Frequency Compensation and Power Stage Design for Buck Converters to Meet Load Transient Specifications

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***Abstract*—The output voltage transient of a buck regulator during a load current step is often a key performance specification. However, many practical design approaches are based on frequency domain specifications like bandwidth and phase margin, without explicitly considering the constraints of the output filter. This paper derives an analytical expression for the peak transient output voltage due to a load step in a buck converter considering bandwidth of its control loop. Utilizing this, a simple design method is developed for a current-mode controlled buck converter with type II compensator that meets the time domain voltage transient specification. The compensator design is illustrated using a critically damped pole/zero cancellation method. The approach is extended to include a design method for voltage-mode buck converters. The critical bandwidth and critical inductance concepts are presented for design in this context. The results are verified using time and frequency domain simulations as well as experimental data.**

I. INTRODUCTION

In the recent past, few attempts have been made to characterize and relate the time domain specifications for load transient with the frequency domain design of the compensator. As such, for dynamic voltage regulation of a current-mode buck converter, its step load response is analyzed using an average state equation in [1]. References [2] and [3] analyze the output impedance of the converter to characterize the step load response. In [4], the analytical expressions are derived for peak voltages in terms of power stage and feedback compensation parameters, which provide insight to obtain a good step load response. Nevertheless, [4] neither addresses the critical bandwidth concept nor provides an expression for peak voltage in terms of bandwidth to develop an easy design method. The relation of bandwidth and peak voltage is derived in [5] for both voltage- and current-mode buck converters. In [5], the analysis for voltage-mode control is quite detailed and the results enjoy good accuracy. However, the analysis for current-mode control is over-simplified, resulting in decreased accuracy when the transient response is bandwidth limited by the control loop. In this paper, the analytical expressions for peak transient voltages are derived using the closed loop output impedance which, under reasonable assumptions, leads to closed form expressions for peak voltage and peak time in terms of bandwidth. The power stage and compensation parameters can then be found using the derived expressions to ensure the target output voltage transient requirement is met for the specified load step.

II. STEP LOAD REPONSE ANALYSIS

A closed loop current-mode (CM) synchronous buck converter circuit is shown in Fig. 1. The corresponding small signal block diagram of the closed loop is given in Fig. 2. The step load response of the converter [4] is given by

$$v_o(t) = L^{-1}\left[Z_{ocl}(s)\Delta I_o / s\right] \tag{1}$$

where $Z_{ocl}(s)$ is the closed loop output impedance and ΔI_o is the load step. From the small-signal model of a CM buck converter, the closed loop output impedance is obtained in (2) where T_i and T_v are the current loop and voltage loop gains respectively.

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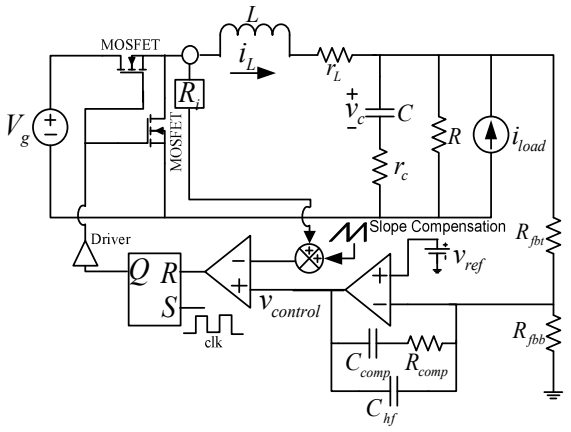

Figure 1. CM synchronous buck converter in closed loop.

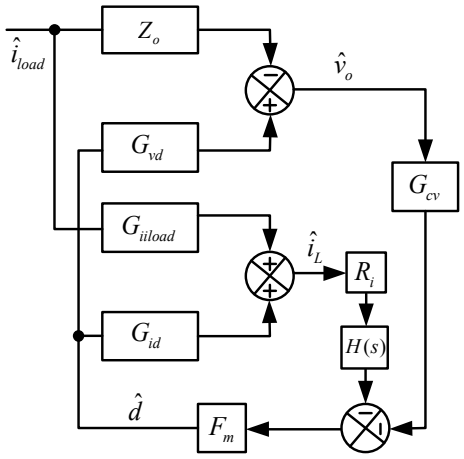

Figure 2. Small signal model of a CM buck converter.

$$Z_{ocl}(s)=\frac{Z_o+T_i\left\{Z_o+G_{vd}G_{iiload}/G_{id}\right\}}{\left(1+T_i+T_v\right)} \tag{2}$$

Since $|T_i|\gg 1$, so $Z_{ocl}(s)$ is approximated as in (3), where T_2 is the overall loop gain given in (4).

$$Z_{ocl}(s)\approx\frac{Z_o+G_{vd}G_{iiload}/G_{id}}{\left(1+T_2\right)},\quad T_2=\frac{T_v}{1+T_i} \tag{3), (4}$$

Substituting the power stage transfer functions into (3), $Z_{ocl}(s)$ is obtained in (5).

$$Z_{ocl}(s)=\frac{Z_{oi}}{1+T_2},\quad Z_{oi}=\frac{R\left(1+s/\omega_z\right)}{\left(1+s/\omega_o\right)} \tag{5), (6}$$

Z_{oi} in (6) is the open loop output impedance with current loop closed, which is equivalent to the impedance of the output filter and load resistance where $\omega_z=1/\left(Cr_c\right)$ and $\omega_o=1/\left(C\left(R+r_c\right)\right)$. Equation (7) defines the overall control loop where $\left(A_{VM}/K_{HF}\right),\omega_{ZEA}$ and ω_{HF} are the type II compensator mid-band gain, zero and pole respectively.

$$T_2=\frac{A_{VM}}{K_{HF}}\cdot\frac{\left(1+\omega_{ZEA}/s\right)}{\left(1+s/\omega_{HF}\right)}\cdot\frac{R\left(1+s/\omega_z\right)}{R_i\left(1+s/\omega_o\right)} \tag{7}$$

Referencing Fig. 1 $A_{VM}=R_{comp}/R_{fbt}$, $K_{HF}=1+C_{hf}/C_{comp}$, $\omega_{ZEA}=1/(R_{comp}C_{comp})$ and $\omega_{HF}=\left(C_{hf}+C_{comp}\right)/\left(C_{hf}C_{comp}R_{comp}\right)$.

Fig. 3 shows a simplified model of the CM buck converter. This model is valid in the vicinity of the control loop crossover frequency, which generally determines the peak of the closed loop output impedance. Equation (5) can be written as

$$Z_{ocl}(s)=\frac{\dfrac{R\left(1+s/\omega_z\right)}{\left(1+s/\omega_o\right)}}{1+\dfrac{A_{VM}}{K_{HF}}\cdot\dfrac{\left(1+\omega_{ZEA}/s\right)}{\left(1+s/\omega_{HF}\right)}\cdot\dfrac{R\left(1+s/\omega_z\right)}{R_i\left(1+s/\omega_o\right)}}. \tag{8}$$

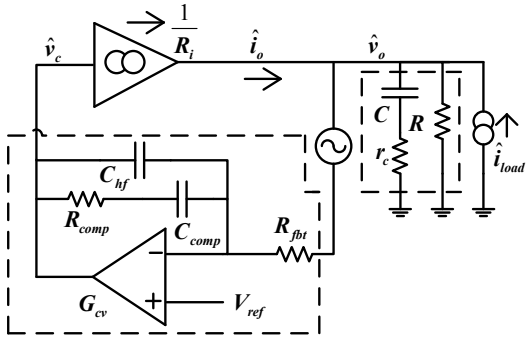

Figure 3. Simplified model of a CM buck converter.

III. Compensation Parameters Design and Peak Transient Voltage

A critically damped pole/zero cancellation method is used to find the type II compensation parameters for the current-mode buck. The high frequency compensator pole is chosen as $\omega_{HF}=\omega_z=1/\left(Cr_c\right)$ to cancel the ESR zero. Equation (8) can be written as

$$Z_{ocl}(s)=\frac{\frac{R(1+s/\omega_z)}{(1+s/\omega_o)}}{1+\frac{A_{VM}\omega_{ZEA}R}{sK_{HF}R_i}.\frac{(1+s/\omega_{ZEA})}{(1+s/\omega_o)}}. \quad (9)$$

Equation (9) can be modified as

$$Z_{ocl}(s)=\frac{R(1+s/\omega_z)}{(1+s/\omega_o)+\frac{K_c\omega_{ZEA}R}{s}(1+s/\omega_{ZEA})} \quad (10)$$

where $K_c=\frac{A_{VM}}{K_{HF}R_i}$.

Equation (10) can be simplified as

$$Z_{ocl}(s)=\frac{sR\omega_o(s+\omega_z)}{\omega_z\left(s^2+s(\omega_o+K_cR\omega_o)+K_c\omega_{ZEA}R\omega_o\right)} \quad (11)$$

since $\frac{R\omega_o}{\omega_z}=\frac{Rr_c}{(R+r_c)}$ and $K_cR\omega_o=\omega_c\frac{R}{R+r_c}$

where control loop bandwidth

$$\omega_c=\frac{A_{VM}}{K_{HF}CR_i}. \quad (12)$$

Then (11) can be modified as

$$Z_{ocl}(s)=\frac{\frac{Rr_c}{R+r_c}s(s+\omega_z)}{\left(s^2+s\left(\omega_o+\omega_c\frac{R}{R+r_c}\right)+\omega_{ZEA}\omega_c\frac{R}{R+r_c}\right)}. \quad (13)$$

Assuming $R\gg r_c$

$$Z_{ocl}(s)=r_c\left(\frac{s(s+\omega_z)}{s^2+s(\omega_o+\omega_c)+\omega_c\omega_{ZEA}}\right). \quad (14)$$

Peak voltage (V_p) and peak time (T_p) can be derived in terms of ω_c, power stage components and parameters as given in Table 1. For a constant current load R→∞ so that the critically damped condition is found when $\omega_{ZEA}=\omega_c/4$. Compensation parameters are shown for the critically damped condition where $\xi=1$.

TABLE I. PEAK VOLTAGES AND TIMES FOR VARIOUS CONDITIONS.

Notations	$\omega_n^2=\omega_c\omega_{ZEA}$, $2\xi\omega_n=(\omega_o+\omega_c)$, $\omega_{d1}=\omega_n\sqrt{1-\xi^2}$, $\omega_{d2}=\omega_n\sqrt{\xi^2-1}$			
Case	$\omega_c\ll 1/(Cr_c)$			$\omega_c\geq 1/(Cr_c)$
	$\xi<1$	$\xi=1$	$\xi>1$	
(T_p)	$\frac{1}{\omega_{d1}}\tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)$	$\frac{1}{\omega_n}$	$\frac{1}{\omega_{d2}}\tanh^{-1}\left(\frac{\sqrt{\xi^2-1}}{\xi}\right)$	0
(V_p)	$\frac{\Delta I_o e^{-\xi\omega_n T_p}}{C\sqrt{\omega_c\omega_{ZEA}}}$	$\frac{\Delta I_o e^{-1}}{C\sqrt{\omega_c\omega_{ZEA}}}$	$\frac{\Delta I_o e^{-\xi\omega_n T_p}}{C\sqrt{\omega_c\omega_{ZEA}}}$	$\left(\frac{Rr_c}{R+r_c}\right)\Delta I_o$
Compensation Parameters	$R_{comp}=4/(2\pi f_c C_{comp})$, $C_{comp}=4/((2\pi f_c)^2R_{fbt}CR_i)-C_{hf}$, $C_{hf}=r_c/(2\pi f_c R_{fbt}R_i)$			

Specifications:

$f_{sw}=300kHz, V_g=12V, V_o=1.2V, R=0.06\Omega,$

$\Delta I_o=5A, C=440\mu F, r_c=2.5m\Omega, L=1.2\mu H, R_i=86m\Omega$

Peak voltages and peak times are compared for two bandwidths of 10 kHz and 20 kHz as listed in Table 2.

"Eq. (2)" is computed using the precise form of (2). "Table 1" is the approximate result from Table 1. "SIMPLIS" is the simulation result using the SIMPLIS circuit simulator. "Ref. [5]" is the result using the equations in [5].

TABLE II. COMPARISON OF PEAK VOLTAGES AT DIFFERENT BANDWIDTHS USING COMPENSATION PARAMETERS FROM TABLE 1.

f_c (*kHz*)	PM (deg)	Eq. (2) $V_{pv}(mV)$ $T_p(\mu s)$	Table 1 $V_{pv}(mV)$ $T_p(\mu s)$	SIMPLIS $V_{pv}(mV)$ $T_p(\mu s)$	Ref. [5] $V_{pv}(mV)$ $T_p(\mu s)$
10	77.3	130	129	131	181
		28	32	28	-
20	67.3	71	67	75	90
		13	15	12	-

IV. Power Stage Design for the Current-Mode Buck Converter

From the small-signal model, closed loop current transfer function $G_{ii\_ci}(s)$ is obtained in (15).

$$G_{ii\_ci} = \frac{G_{ii}(1+T_v) + F_m G_{id} G_{cv} Z_o}{1+T_i+T_v} \quad (15)$$

Since $|T_i| \gg 1$, $G_{ii\_ci}(s)$ is approximated by (16).

$$G_{ii\_ci} \approx \frac{G_{ii}T_2 + G_{cv}Z_o/R_i}{1+T_2} = \frac{\omega_c(s+\omega_{ZEA})}{(s^2+2\xi\omega_n s+\omega_n^2)} \quad (16)$$

The inductor current due to a step change in load current is given by (17) for $\xi < 1$.

$$i_L(t) = \Delta I_o \left[1 - \frac{e^{-\xi\omega_n t}}{\sqrt{1-\xi^2}} \left\{ \sqrt{1-\xi^2}\cos\omega_{d1}t + \left(\xi - \frac{\omega_n}{\omega_{ZEA}}\right)\sin\omega_{d1}t \right\} \right] \quad (17)$$

The maximum rate of change of the inductor current is found by differentiating (17) and is given by (18).

$$\left.\frac{di_L(t)}{dt}\right|_{\max} = \Delta I_o.\omega_c \quad (18)$$

The rate of change of inductor current cannot exceed this value without slew rate limiting. The inductor current slew rate during step-up and step-down are given by (19) and (20) respectively.

$$\frac{di_L(t)}{dt}|_{up} = \frac{V_{in}-V_o}{L} \quad , \quad \frac{di_L(t)}{dt}|_{down} = \frac{V_o}{L} \quad (19), (20)$$

The inductance value is obtained from (21).

$$L = \frac{V_{in}MIN(D,D')}{\Delta I_o \omega_c} \quad (21)$$

The peak voltage for the critically damped case is given by (22) with the compensator zero at $\omega_{ZEA} = \omega_c / 4$.

$$V_p = \frac{2\Delta I_o e^{-1}}{C\omega_c} \quad (22)$$

The critical bandwidth as defined in [5] is given by (23).

$$f_{ct\_i} = \frac{1}{2\pi C r_c} \quad (23)$$

In order to keep the output capacitor's series resistance from determining the output transient voltage, the critical bandwidth must be higher than the control loop bandwidth.

The critical inductance from [7] is given by (24).

$$L_{ct} = \frac{V_{in}MIN(D,D')Cr_c}{\Delta I_o} \quad (24)$$

In a closed loop system, the critical inductance indicates the point beyond which the duty cycle saturates at its maximum value. The peak transient voltage is then determined by the large signal limiting of the inductor current into the output capacitor. This is validated experimentally using the LM5117 synchronous buck controller with 12V output. Fig. 4 shows the variation of output voltage at different duty cycles with 15 kHz bandwidth and a 5A load current step. As can be seen for duty cycle exceeding 0.5 the transient voltage droop is large signal limited by the characteristic of the output filter.

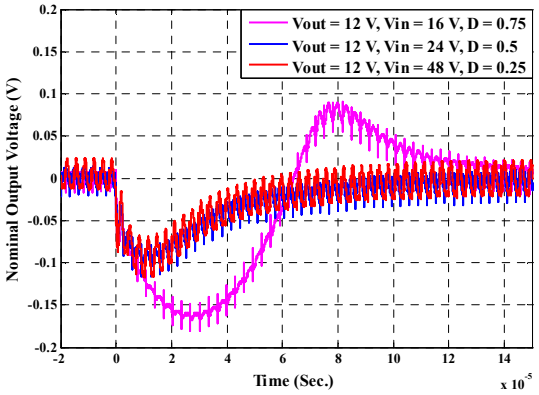

Figure 4. Comparison of output voltage with different input voltages at 5A load step.

V. Current-Mode Power Stage and Compensation Design

For practical design, the inductor ripple current is generally chosen to be a significant percentage of the average current, with associated loss being a limiting factor. The capacitor series resistance is then chosen to be less than that required to produce the transient voltage limit by the load current step. The output capacitor value is found taking into account the critical inductance limit. The control loop bandwidth is then identified based on the value of output capacitance. This is illustrated by the following design example.

Given $f_{sw} = 300kHz, V_{in} = 12V, V_o = 1.2V, V_p = 80mV$

$R = 1.2V/10A = 0.12\Omega$, $R_i = 86m\Omega$, $\Delta I_o = 5A$

$$L = \frac{V_O D'}{I_{PP} f_{SW}}, \qquad r_c \le \frac{V_p}{\Delta I_o} \qquad (25), (26)$$

$$C \ge \frac{2e^{-1}\Delta I_o{}^2 L}{V_{in} MIN(D, D') V_p}, \qquad f_c \ge \frac{2e^{-1}\Delta I_o}{2\pi V_p C} \qquad (27), (28)$$

From (25) assuming 30% ripple current, $I_{pp} = 3A$, $L = 1.2\mu H$. From (26) the maximum ESR of the output capacitor is $r_c \le 16m\Omega$. From (27) the minimum value of output capacitance is $C \ge 230\mu F$. Choose two 220µF, 5mΩ capacitors in parallel for C = 440µF, r_c = 2.5mΩ. From (28) the minimum value of the control loop bandwidth is $f_c \ge 16.7kHz$. Choose $f_c = 20kHz$ and find compensation components using standard values of $R_{comp} = 25.5k\Omega$, $C_{comp} = 1.5nF$, $C_{hf} = 56pF$. For comparison choose a second design at $f_c = 10kHz$ using standard values of $R_{comp} = 12.1k\Omega$, $C_{comp} = 5.6nF$, $C_{hf} = 100pF$.

VI. Current-Mode Experimental Verification

The LM5117 current-mode synchronous buck controller is used for experimental verification with component specifications given in the design examples as shown in Fig. 5. The experimental results for transient and frequency responses are shown in Fig. 6 through Fig. 9. The transient response and frequency response are compared to simulated and calculated results in Fig. 10 through Fig. 13. As can be seen from Fig. 10 the 10 kHz design exhibits greater than the 80mV transient target while in Fig. 11 the 20 kHz design is within specification.

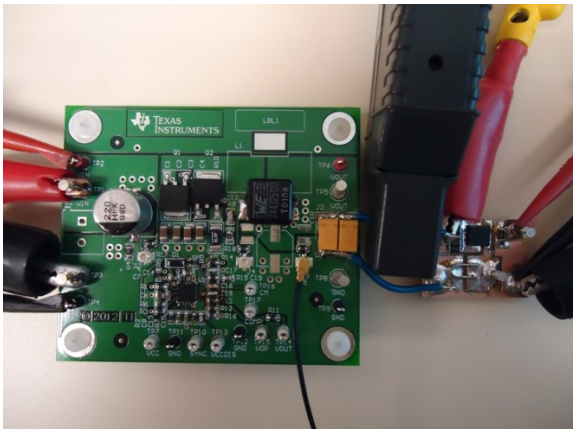

Figure 5. Experimental set-up for transient response test.

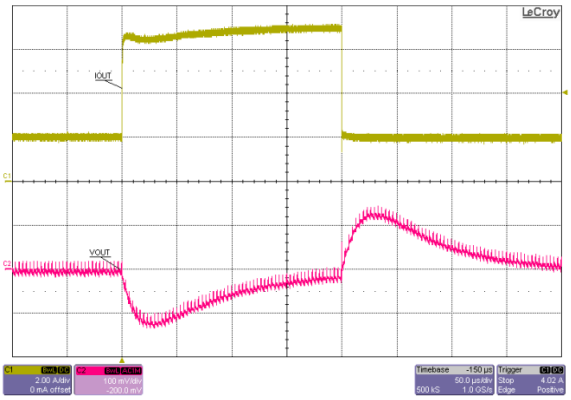

Figure 6. Output voltage with 5A load step for 10 kHz BW.

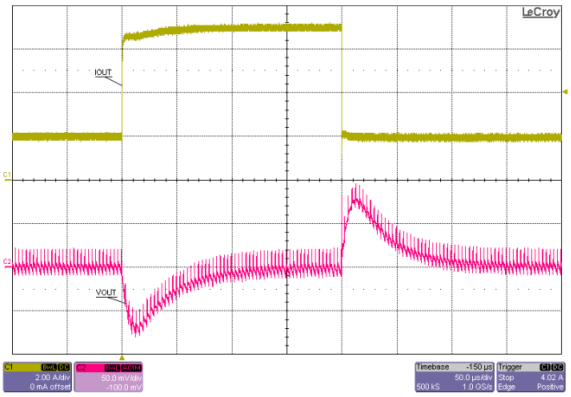

Figure 7. Output voltage with 5A load step for 20 kHz BW.

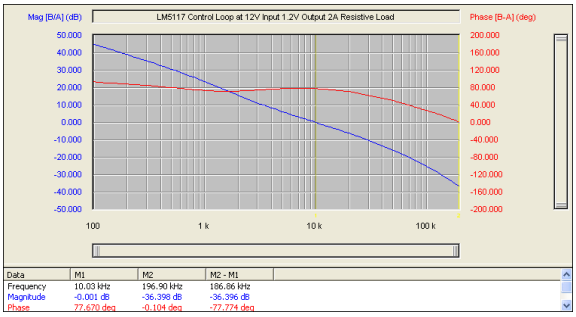

Figure 8. Control loop gain/phase plot for 10 kHz BW.

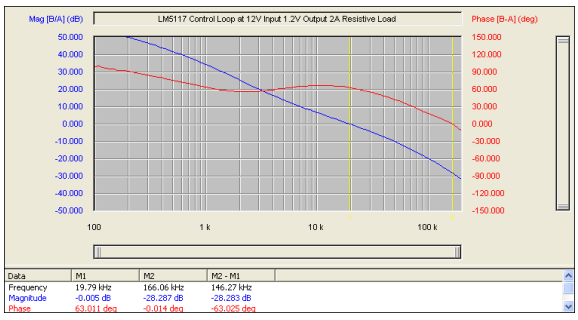

Figure 9. Control loop gain/phase plot for 20 kHz BW.

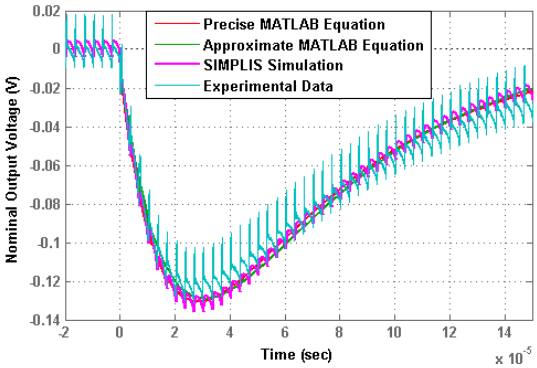

Figure 10. Comparison of output voltages for 10 kHz BW.

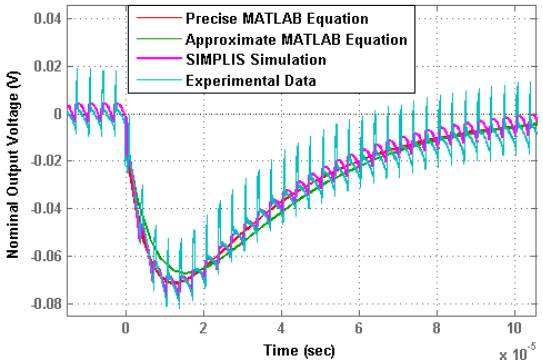

Figure 11. Comparison of output voltages for 20 kHz BW.

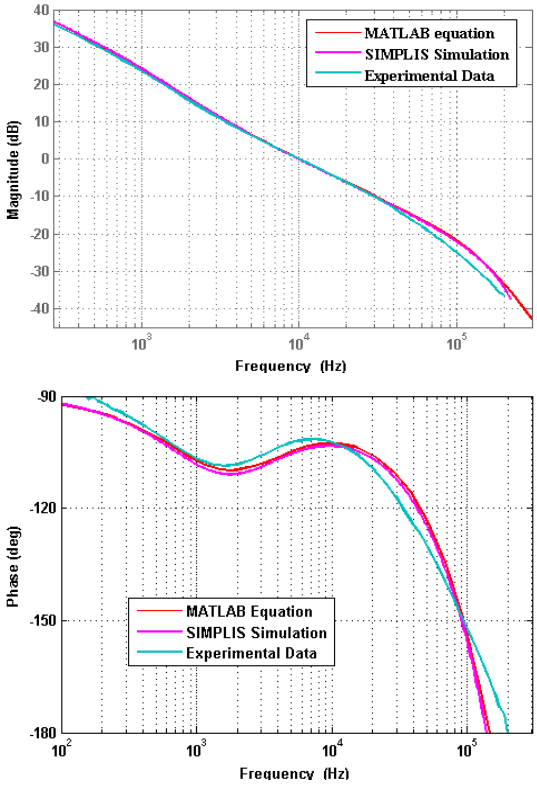

Figure 12. Comparison of gain/phase plots at 10 kHz BW.

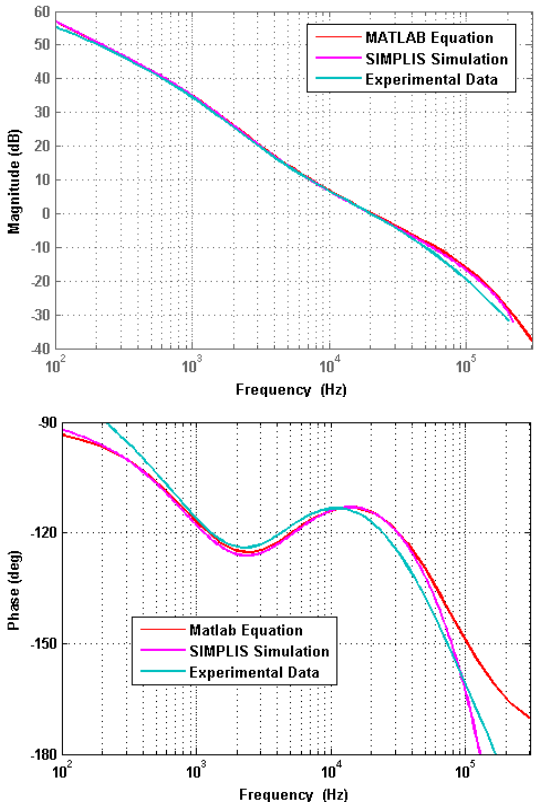

Figure 13. Comparison of gain/phase plots at 20 kHz BW.

VII. Voltage-Mode Power Satge Design and Compensator Design

A synchronous voltage-mode (VM) buck converter shown in Fig. 14 is analyzed in [5] based on closed-loop inductor to load current transfer function and the peak transient voltage is related to control bandwidth in (29) and (30).

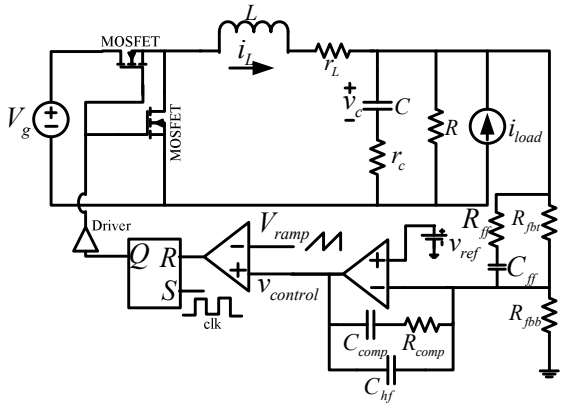

Figure 14. VM synchronous buck converter in close loop.

$$V_p = \frac{1+(4r_cCf_c)^2}{8Cf_c}\Delta I_o \quad \text{when} \quad f_c < f_{ct\_v} \qquad (29)$$

$$V_p = r_c \Delta I_o \quad \text{when} \quad f_c \geq f_{ct\_v} \tag{30}$$

where $f_{ct\_v} = 1/4Cr_c$ is the critical bandwidth.

The small-signal model of the VM buck converter is shown in Fig. 15.

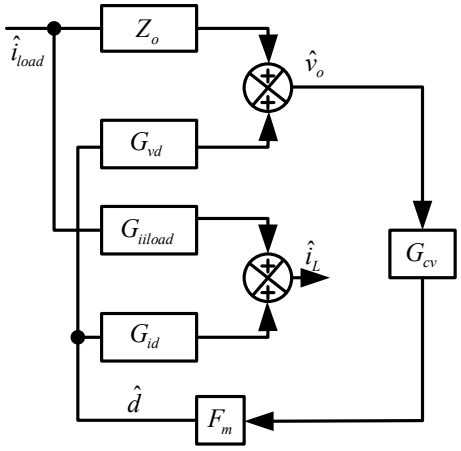

Figure 15. Small-signal model of a VM buck converter.

The VM buck converter is analyzed based on closed-loop output impedance transfer function. The closed-loop output impedance is given by

$$Z_{ocl} = \frac{Z_o}{1 + G_{cv} F_m G_{vd}} \tag{31}$$

and the control loop,

$$T_v = G_{cv} F_m G_{vd}\,. \tag{32}$$

A type III compensator is designed based on pole/zero placement method in which two zeros are placed at the power stage poles, one pole is placed at ESR zero and another pole at switching frequency. Referring to Fig. 14,

$$G_c = \frac{V_{ramp}\omega_c}{V_g \omega_p},\ C_{hf} = \frac{1}{\omega_{sw} G_c R_{fbt}},\ C_{comp} = C_{hf}\left(\frac{\omega_{sw} - \omega_p}{\omega_p}\right)$$

$$R_{comp} = \frac{1}{\omega_p C_{comp}},\ R_{ff} = \frac{R_{fbt}\omega_p}{\omega_z - \omega_p},\ C_{ff} = \frac{1}{\omega_z R_{ff}} \tag{33}$$

The closed-loop output impedance is approximated as

$$Z_{ocl}(s) = \frac{s r_c \left(s + \omega_z\right)}{\left(s^2 + s\omega_c + 2\omega_c\omega_p\right)} \tag{34}$$

where $\omega_p = \frac{1}{\sqrt{LC}}$, $\omega_z = \frac{1}{Cr_c}$ and damping factor

$$\xi = \sqrt{\frac{\omega_c}{8\omega_p}}\,. \tag{35}$$

Equations (29) through (30) from [5] are valid for the under damped case where $\omega_c < 8\omega_p$.

A similar design method is presented for the power stage and compensation design of a VM buck converter. The design constraints can be found in (36) through (39). A design example is shown with the following specifications.

$$f_{sw} = 300kHz, V_{in} = 12V, V_o = 1.2V, V_p = 80mV$$
$$R = 1.2V/10A = 0.12\Omega, \Delta I_o = 5A$$

$$L = \frac{V_O D'}{I_{PP} f_{SW}}, \qquad r_c \leq \frac{V_p}{\Delta I_o} \tag{36), (37}$$

$$C \geq \frac{\Delta I_o{}^2 L}{V_{in} MIN(D, D') V_p} \cdot \frac{1}{1 + \sqrt{1 - \left(\Delta I_o r_c / V_p\right)^2}} \tag{38}$$

$$f_c \geq \frac{\Delta I_o}{4 V_p C} \cdot \frac{1}{1 + \sqrt{1 - \left(\Delta I_o r_c / V_p\right)^2}} \tag{39}$$

For practical design, assuming 30% current ripple, $I_{pp} = 3A$, the inductance value is obtained from (36) as $L = 1.2\mu H$. From (37) the maximum ESR of the output capacitor is $r_c \leq 16m\Omega$. From (38) the minimum value of output capacitance is $C \geq 312.5\mu F$. Choose two 220µF, 5mΩ capacitors in parallel for C = 440µF, r_c = 2.5mΩ. From (39) the minimum value of the control loop bandwidth is $f_c \geq 17.76kHz$. Choose $f_c = 20kHz$ and find compensation components using pole/zero placement method. The obtained parameters are $R_{comp} = 2.2k\Omega$, $C_{comp} = 10nF$, $C_{hf} = 220pF$, $R_{ff} = 300\Omega$, $C_{ff} = 3.3nF$. The design is verified by large-signal simulations with SIMPLIS simulator as well as with experiments using the LM27403 synchronous buck controller. Fig. 16 and Fig. 17 show the experimental data for 20 kHz bandwidth. Fig. 18 shows that the experimental gain/phase plots match with simulation results. Fig. 19 shows the comparison of output voltages at 20 kHz bandwidth which meets the target peak transient voltage of 80 mV.

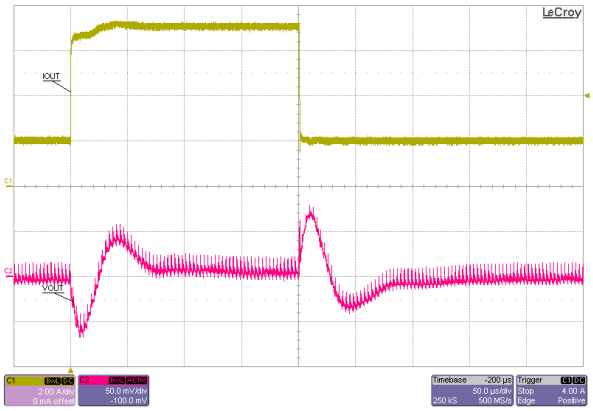

Figure 16. Output voltage with 5A load step for 20 kHz BW.

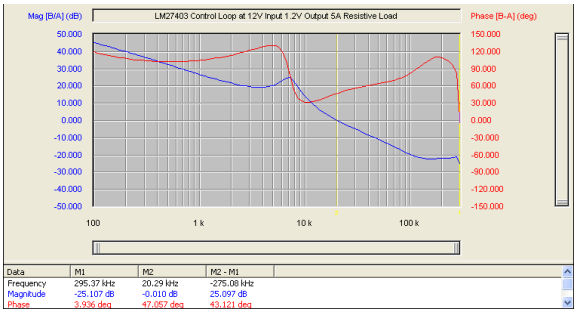

Figure 17. Control loop gain/phase plot for 20 kHz BW.

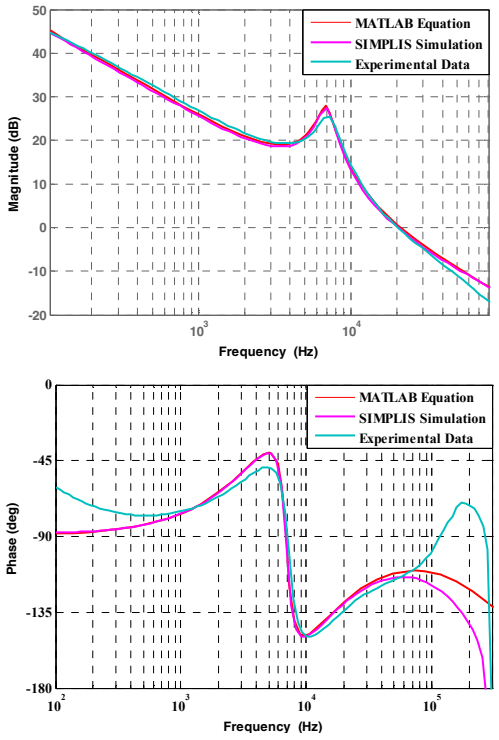

Figure 18. Comparison of gain/phase plots at 20 kHz BW.

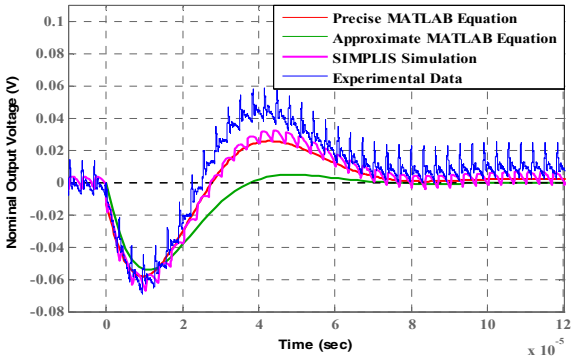

Figure 19. Comparison of output voltage at 20 kHz BW.

VIII. Conclusion

Analytical expressions for peak transient voltage and peak time have been derived in terms of bandwidth for the buck converter. This allows for a simplified design method by which the target output voltage transient is met for the specified load step. The results are verified using large-signal SIMPLIS simulations as well as by experiments using LM5117 and LM27403 synchronous buck controllers.

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