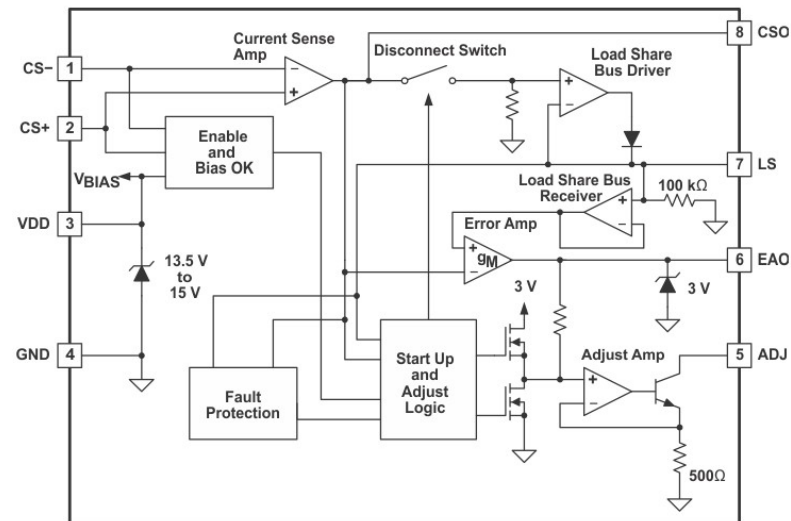# Reference Guide to the
UCC29002

Advanced 8 pin Load Share Controller

TEXAS INSTRUMENTS
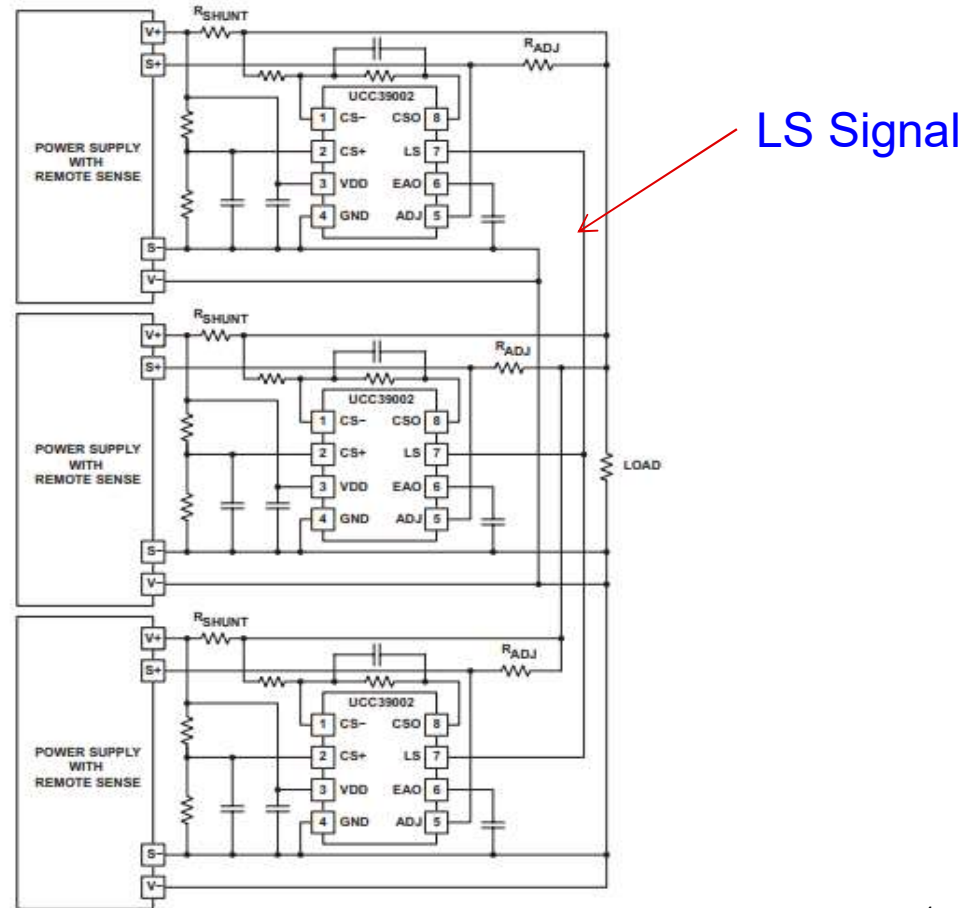
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UCC29002 Controller

- The UCC29002 utilizes a shared bus LS signal.
- LS represents the current output of the power module with the highest output current
- This common LS signal forces the lower current power modules to provide a higher output current.
- In steady state all power modules provide an equal contribution of output current.
- This method of equal current sharing is normally called :
- MASTER SLAVE Automatic Selection

LS Signal

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Power Module With Remote Sensing

- V+ Output Power Rail

- V- Output Power Return

- S+ is the load sense voltage

- S- is the return voltage at the load

RSENSE is an internal voltage to the Power Module.
If unknown then it can easily be measured.

Power Modules with Output Voltage Trim

- The ADJ pin is configured as a current follower and applies a error signal to the TRIM resistor on the power module
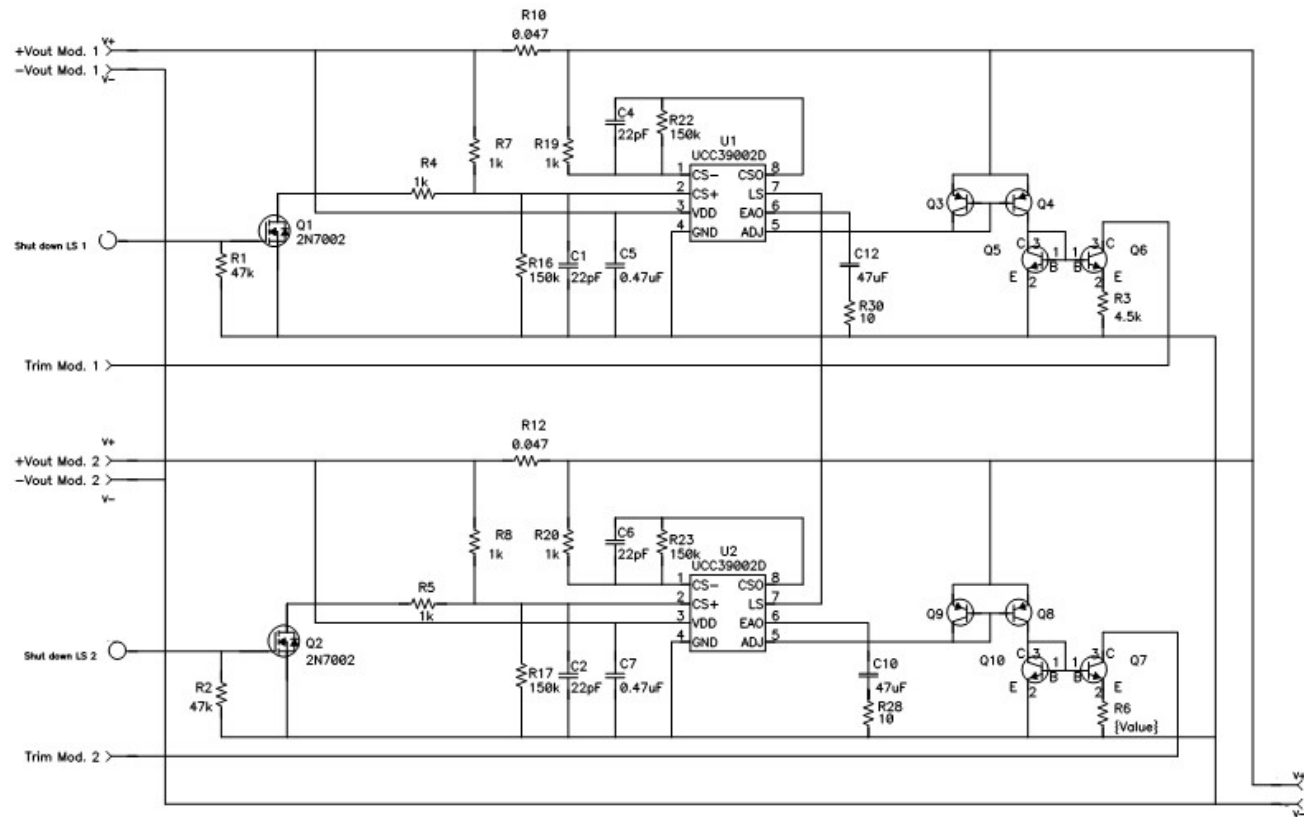
- Power modules with fixed output voltage cannot be used with the UCC29002.

- LED drivers with fixed load current cannot be used with the UCC29002.

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Power Modules with High Voltage Output

- The max voltage rating on the VDD and ADJ pins is 15V

- For output voltages greater than12V it is recommended that this application be used

- Resistive dividers RBIAS1 and RBIAS2 set the voltage on VDD at 12V

- The NPN transistor sets the max voltage on ADJ to (VDD-0.7) V

- Example shown for low side current sensing

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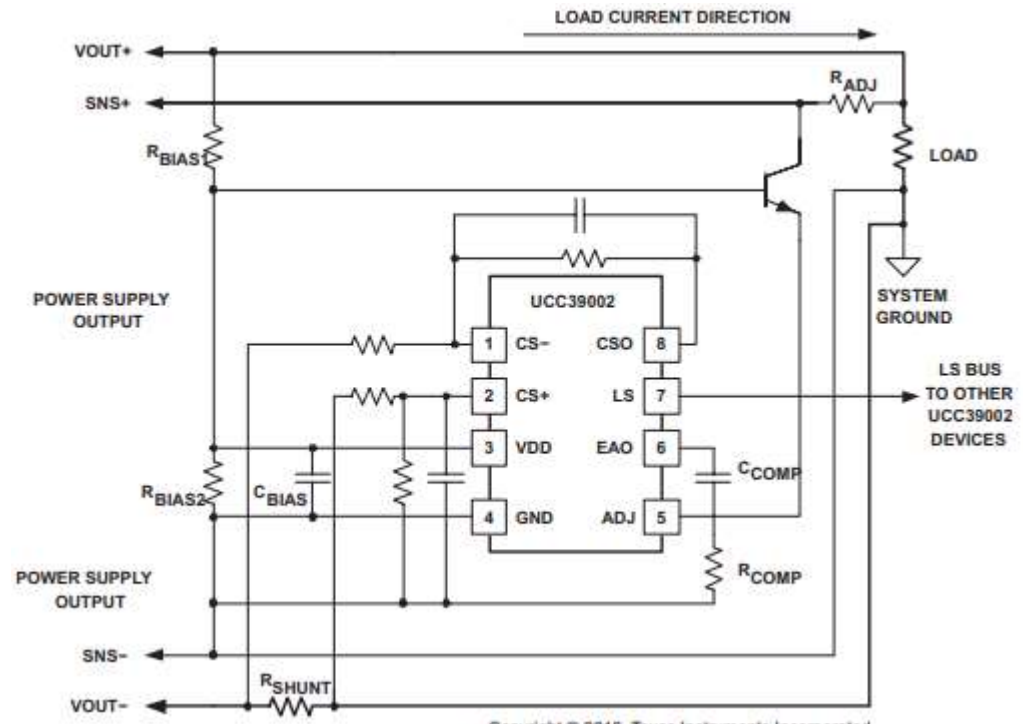
High Output Voltage with High Side Current Sensing

- In some applications low side current sensing is not possible because of the pcb layout. High side sensing is only viable option

- As in previous example VDD and ADJ are limited to 12V

- CS amplifier is not unity gain stable and must have a minimum gain of three.

- This means DIVIDER1 and DIVIDER2 set the voltages
  CS+(max) and CS-(max) not to exceed 4 V
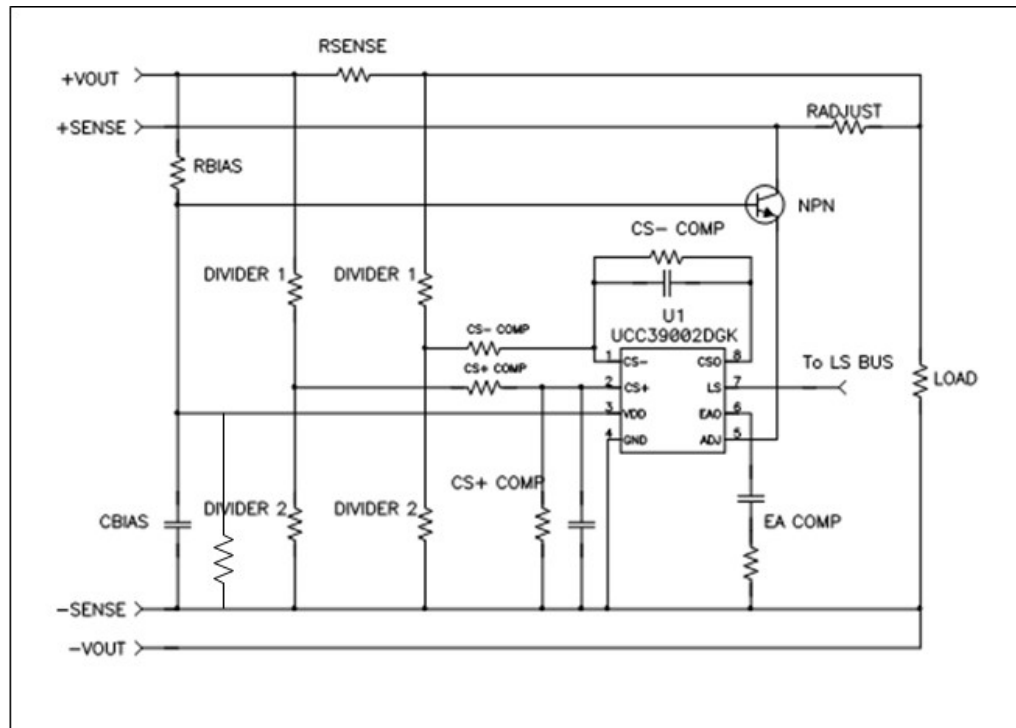
Power Modules with Low Voltage Output

- There are two limitations on the minimum output voltage

- $VDD_{MIN} = 4.5V$

- $ADJ_{MIN} = EAO + 1 = 4V$

- These limitations can be resolved by applying an external 8V to VDD and -5V to ADJ relative to the GND return of the power module

- The example shown has a 1V output

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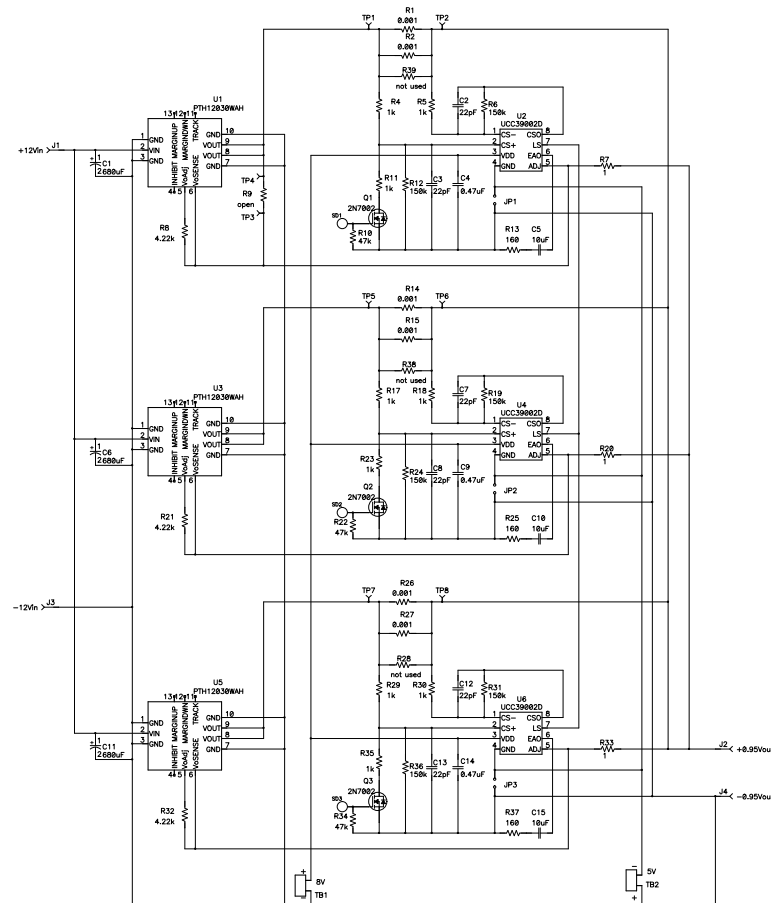
Power Module Startup Requirement

Power Module must source but not sink current

This means that if SR FETs are used they should disabled at startup
or the module should have a pre bias load startup capability.

Without this feature one module may source current into another module.
This will pump energy from the secondary to the primary
of the module sinking current.
This results in startup oscillations, voltage glitching and transients.

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UCC29002 Startup Behaviour

- The UCC29002 and the UCC39002 both disable load sharing at startup.

- ADJ is forced to sink maximum current.

- The controller returns to normal operation when the
value of CSO exceeds 80% of the average per module current.

  This forces a know state for each load share module
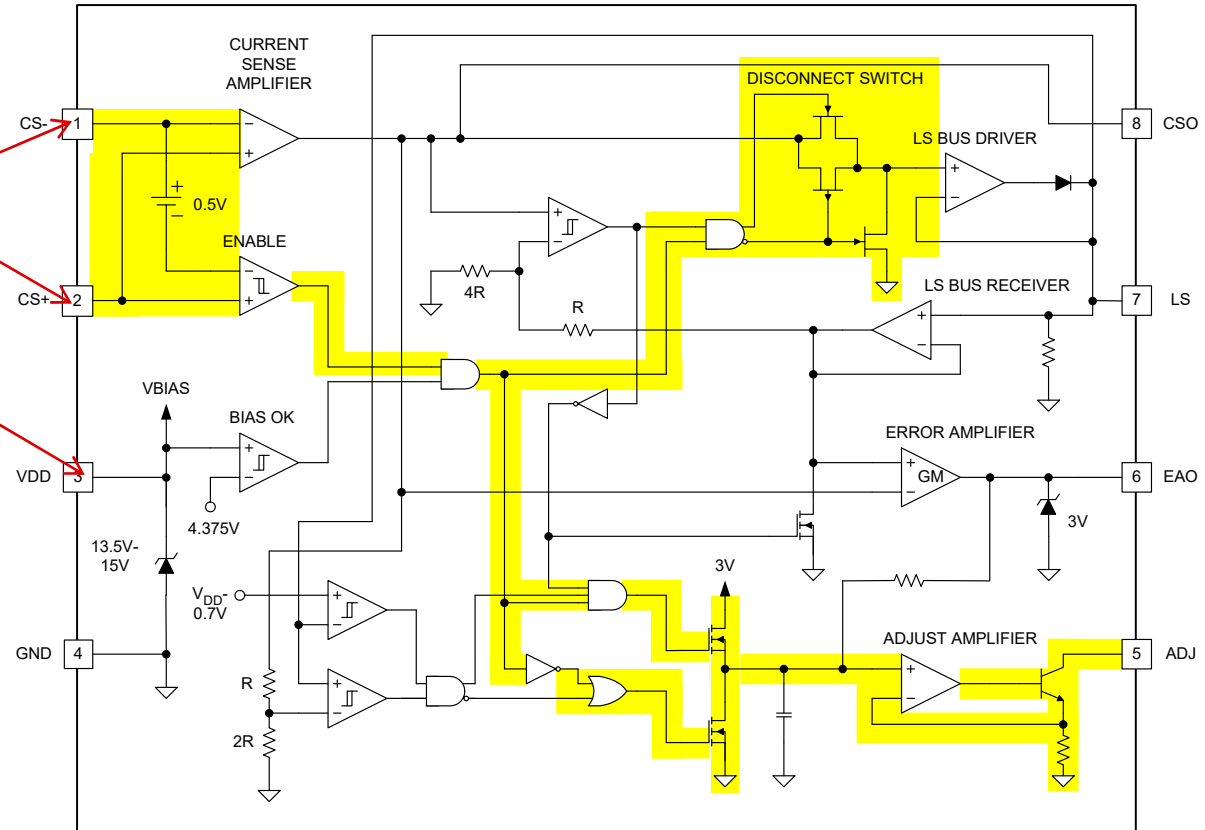 and helps prevent large load transients oscillations
  at startup

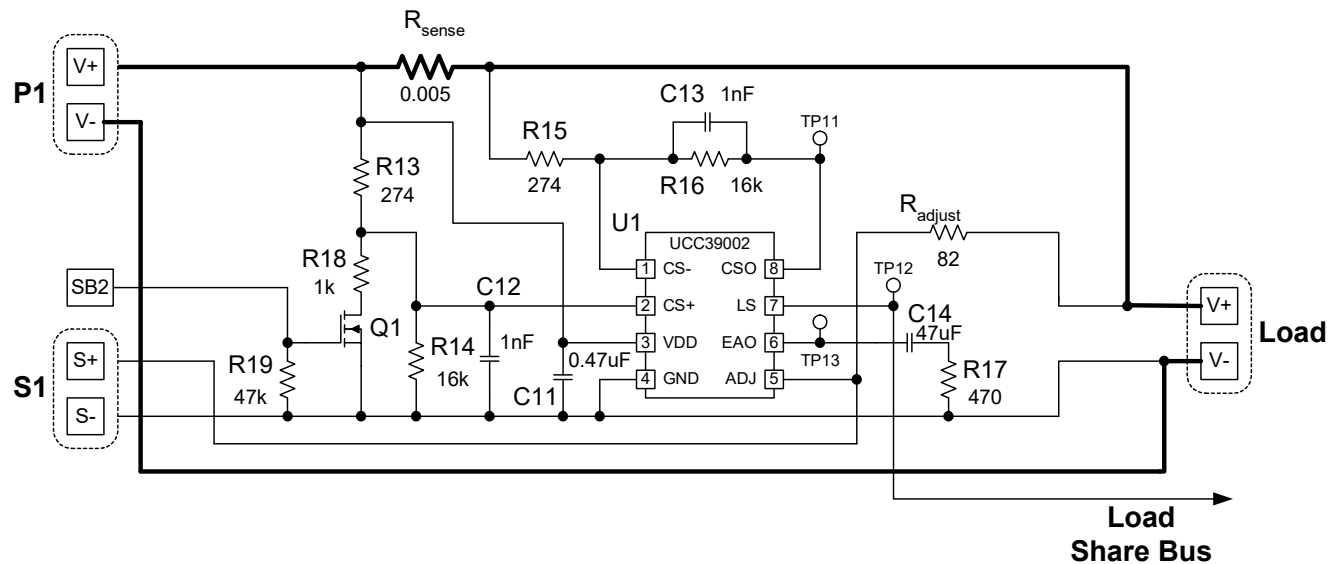- The UCC29002-1 does not have this startup feature.

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Disabling the UCC29002

UCC29002 is disabled when VDD is less than 4.375 V or when CS- is 0.5V greater than CS+

CS- >0.5+CS+

VDD less than 4.375V

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UCC29002 Startup and Shutdown

UCC29002 is enabled when
VDD is greater than 4.375 V
and CS- is not greater than 0.5V relative to CS+

This feature can be used as a reliable method of enabling and disabling the load
sharing function

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Requirements :Loop Response

- The crossover frequency for the load share loop needs to be set at one decade below the unity gain crossover frequency of the Power Modules.

- This important design requirement is used to calculate the compensation component values on the error amplifier output EAO.

- The UCC290002 control loop is slow and current sharing is not accurate during transients

- Startup into a full load may trigger over current protection because of the slow loop response

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Requirements : Load Share Accuracy

- Current sharing accuracy is largely determined by the noise immunity associated with measuring the load module current.

- A good pcb layout is very important in minimizing noise measurement errors
    - Use separate power returns and control signal returns paths
    - Use the largest acceptable current shunt value
    - LS is a DC control signal and should not have any switching noise. Do not add a capacitor filter on LS

- Possible full load accuracy of up to 1%.

- Accuracy degrades at light loads and with lower output voltages.

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PCB Layout Example
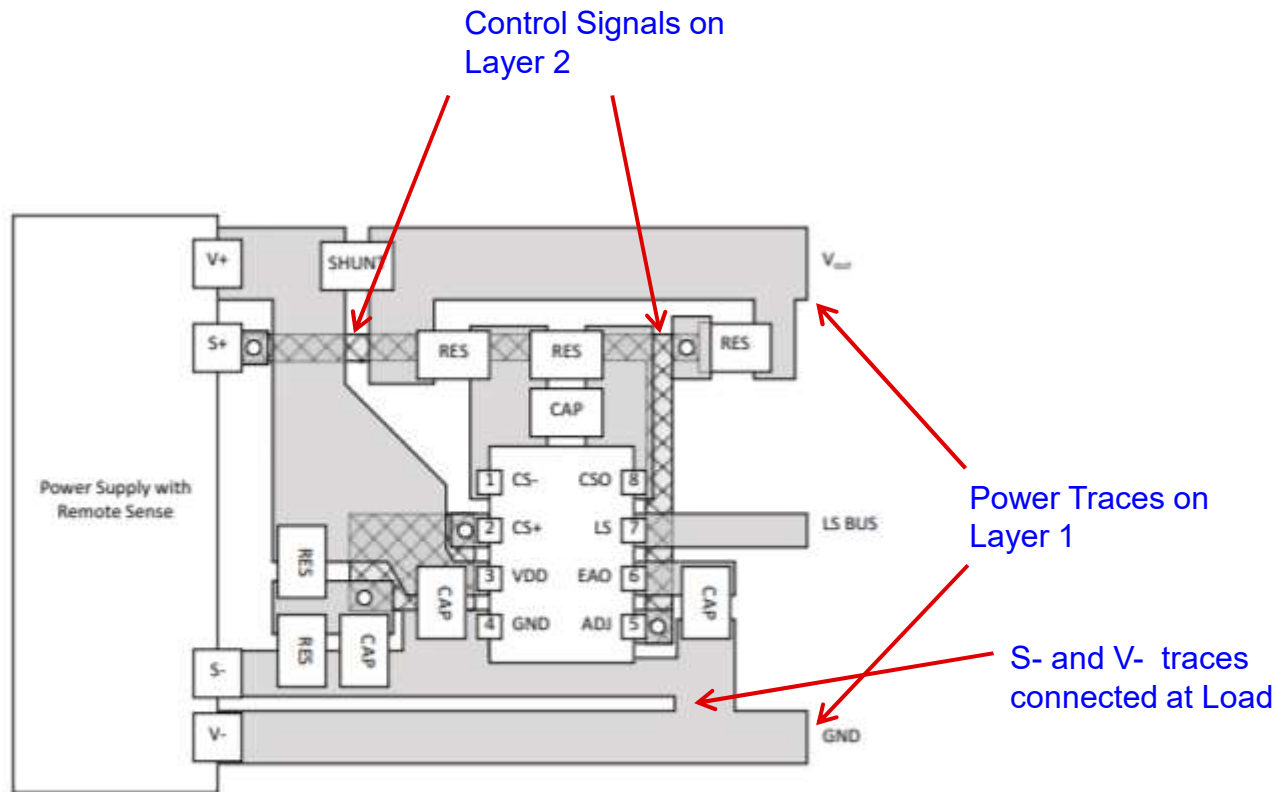
UC29002 and UC2902 Comparison

	UC2902	UCC29002
Supply Current (max)	6mA	3.5mA
Supply Voltage (max)	20V	15V
Start Up Voltage	UVLO 2.5V	Bias OK 4.375V
Current Sense Amplifier Gain	40 V/V internally set	User programmable differential amplifier
High-Side Current Sense	No	Yes
Low-Side Current Sense	Yes	Yes
CS Input Offset Voltage	1.5mV	350μV
Hot-Swap Capability	No	Yes
Load Share Bus	Differential Line	Single Wire
Package	SOIC-8, DIL-8	SOIC-8, MSOP (DGK), DIL-8
High-Temp Version	No	No

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Additional Resources

- Excel Calculator Tool
  http://www.ti.com/product/UCC29002/technicaldocuments

- Mathcad Calculator Tool
  http://www.ti.com/product/UCC29002/toolssoftware

- SLUA311 Application Report
  http://www.ti.com/lit/an/slua311/slua311.pdf

- SLUU137B Reference Design
  http://www.ti.com/lit/ug/sluu137b/sluu137b.pdf

- SLUU166A User Guide
  http://www.ti.com/lit/ug/sluu166a/sluu166a.pdf

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