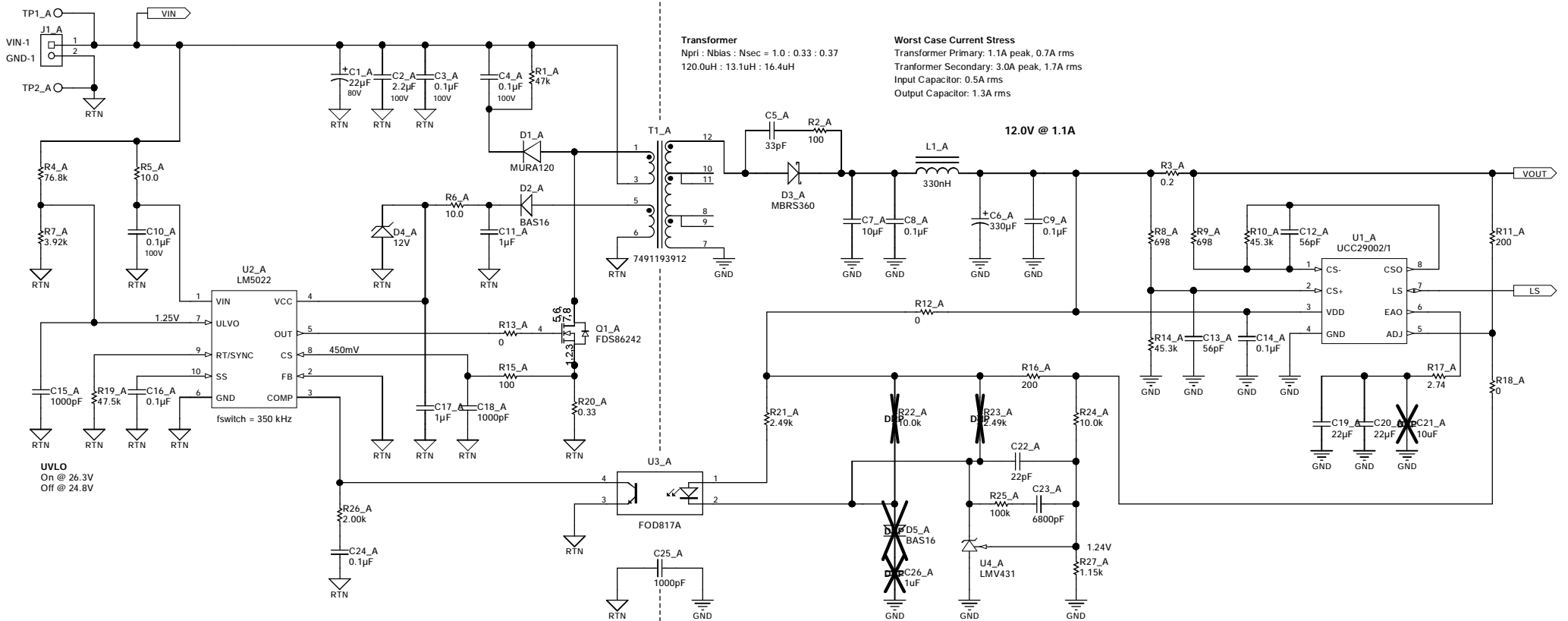


Revision History	
Revision	Notes
A	* First release
B	* Built & Tested

**Design Notes**  
 \* R12, R18 for test purpose only  
 \* C21, C26, D5, R22, R23 not populated  
 \* U1 (SO-8) does not meet footprint (8-VSSOP)

Up to 8 Inputs  
 27 .. 60V DC



**Transformer**  
 Npri : Nbias : Nsec = 1.0 : 0.33 : 0.37  
 120.0uH : 13.1uH : 16.4uH

**Worst Case Current Stress**  
 Transformer Primary: 1.1A peak, 0.7A rms  
 Transformer Secondary: 3.0A peak, 1.7A rms  
 Input Capacitor: 0.5A rms  
 Output Capacitor: 1.3A rms

12.0V @ 1.1A

UVLO  
 On @ 26.3V  
 Off @ 24.8V

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Designed for: Public Release	Mod. Date: 1/30/2015
Project Title: 8x Revers Power	
Number: PMP10099   Rev: B	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Final Version
Drawn By:	File: PMP10099RevB - Circuit.SchDoc
Engineer: Matthias Ulmann	Contact: http://www.ti.com/support

Sheet 2 of 2  
 Size: A3  
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