

NIKO-SEM

**N-Channel Enhancement Mode
Field Effect Transistor**

PK600BA

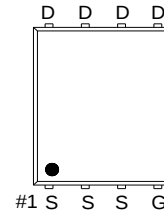
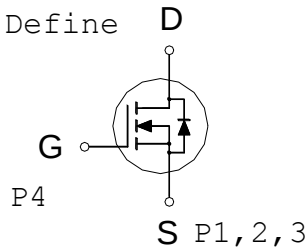
PDFN 5x6P

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
30V	9.5m Ω	40A

Pin Define P5, 6, 7, 8



G. GATE
D. DRAIN
S. SOURCE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ³	$T_C = 25\text{ }^\circ\text{C}$	I_D	40	A
	$T_C = 100\text{ }^\circ\text{C}$		25	
Pulsed Drain Current ¹		I_{DM}	100	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	10.7	
	$T_A = 70\text{ }^\circ\text{C}$		8.6	
Avalanche Current		I_{AS}	18	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	16.2	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	27.8	W
	$T_C = 100\text{ }^\circ\text{C}$		11	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	2	W
	$T_A = 70\text{ }^\circ\text{C}$		1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		63	$^\circ\text{C} / \text{W}$
Junction-to-Case	$R_{\theta JC}$		4.5	

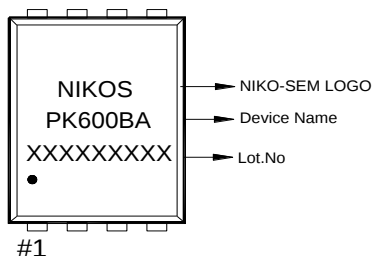
¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25\text{ }^\circ\text{C}$.

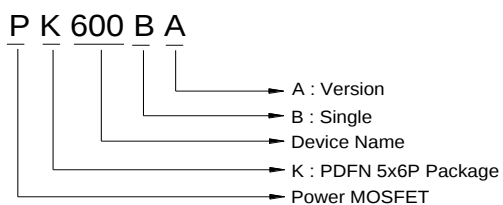
³Package limitation current is 20A.

Marking Information:(Please see the corresponding data sheet)

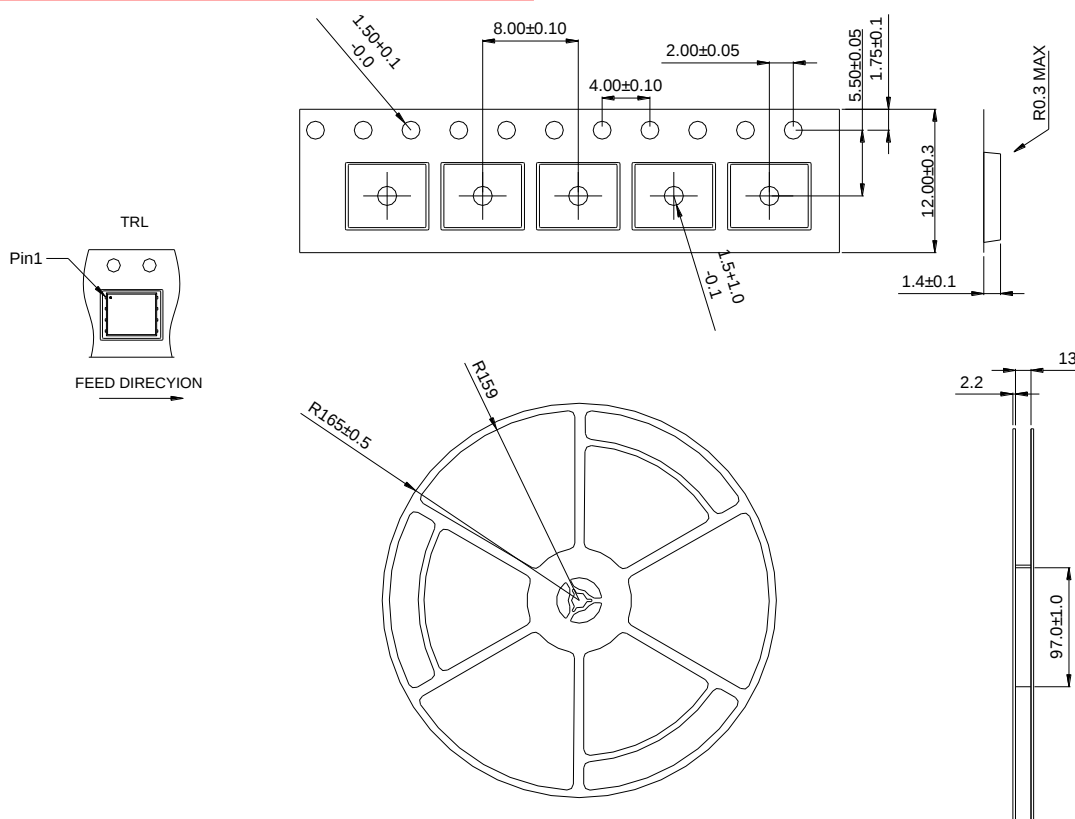
1.Part Marking



2. Part number



Tape&Reel Information:3000pcs/Reel



附註:All Dimension in milimeter

Lot.No. & Date Code rule

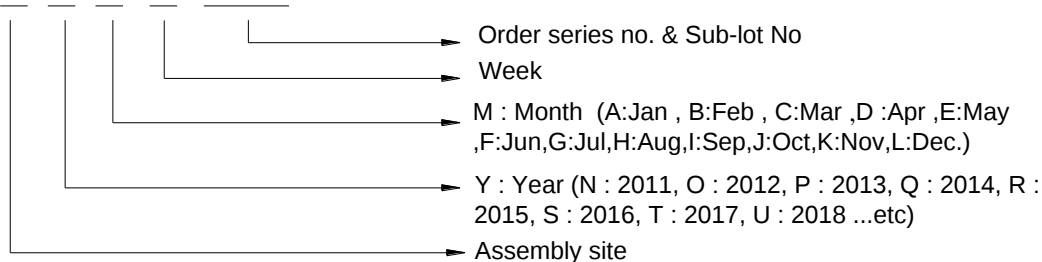
1.LOT.NO.

M N 15M21 03



2.Date Code

D Y M X XXX



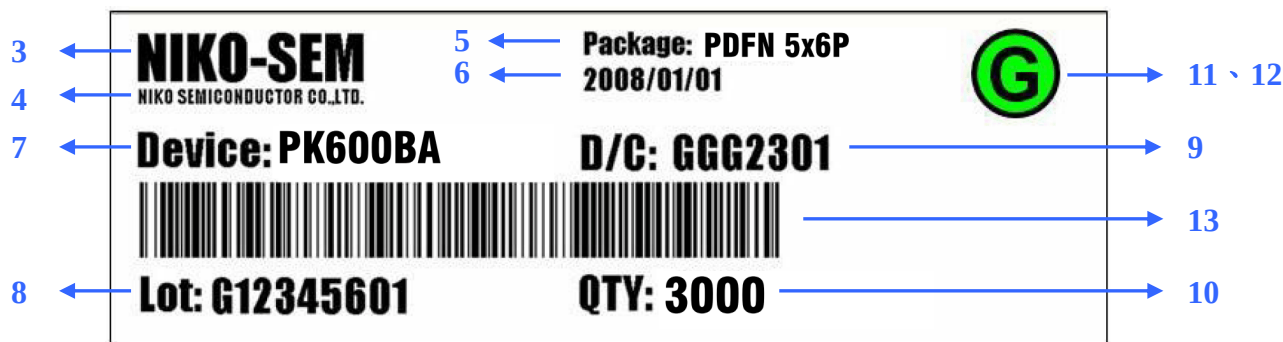
3.Date Code (for Small package)

XX Y WW



Label rule

標籤內容 (Label content)

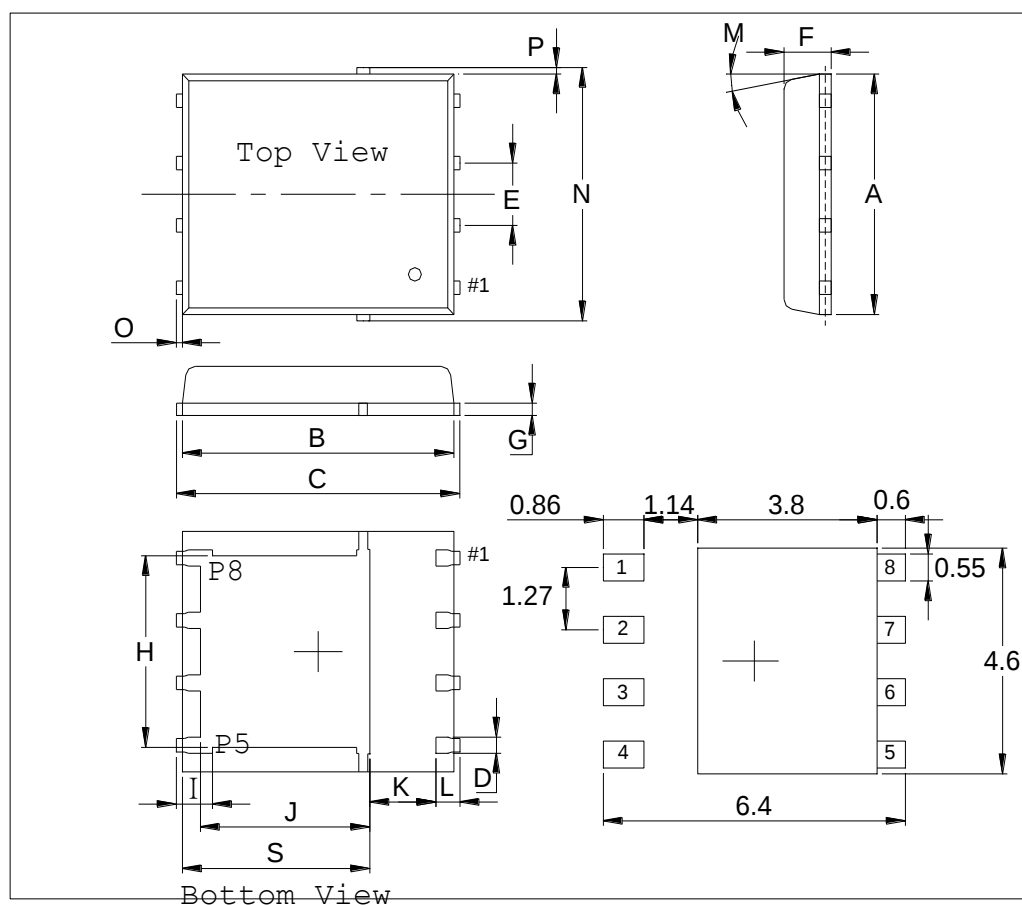


1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可區分英文”O”和數字”0”，”G 和”Q”的字型即可) (Or any font capable of being distinguished for Letter O and digital 0, and for G and Q))
3	NIKO-SEM	Height: 4 mm
4	NIKO SEMICONDUCTOR CO., LTD.	Height: 1 mm
5	Package	Height: 2 mm
6	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
7	Device	Height: 3 mm (Max: 16 Digit) Device Name not including Rev.
8	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
9	D/C	Height: 3 mm (Max: 7 Digit)
10	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
11	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
13	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least

Package Dimension

PDFN 5x6P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.34		3.9
B	5.42		5.9	K	0.9		
C	5.9		6.35	L	0.38		0.711
D	0.3		0.51	M	0°		12°
E	1.17	1.27	1.37	N	4.8		5.4
F	0.8	1	1.2	O	0.05		0.36
G	0.15		0.35	P	0.05		0.25
H	3.67		4.31	S	3.73		4.19
I	0.38		0.71				

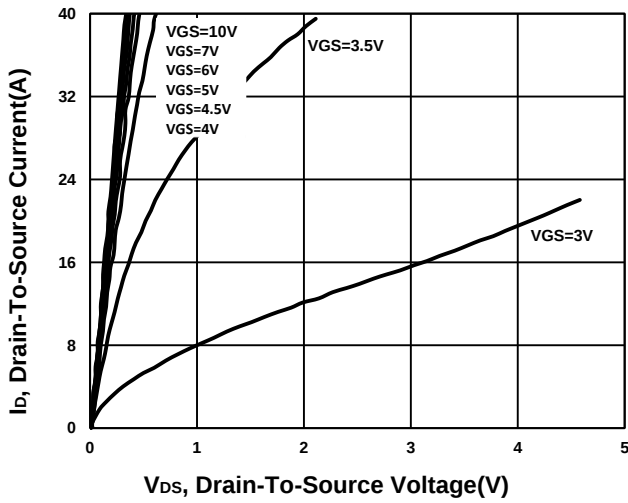


ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

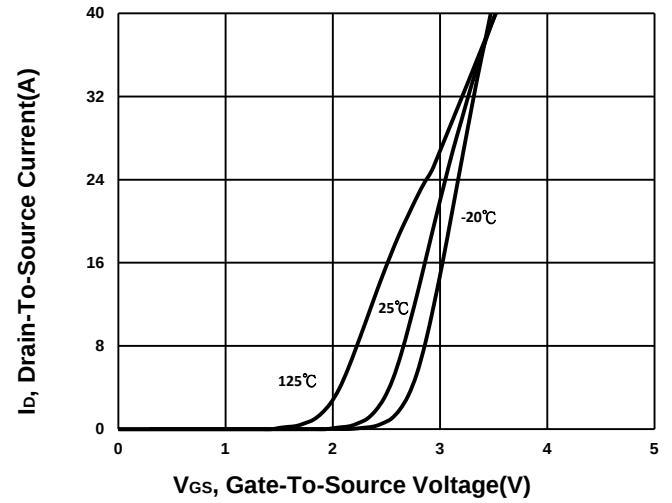
PARAMETER	SYMBOL		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}		V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}		V _{DS} = V _{GS} , I _D = 250μA	1.3	1.75	2.3	
Gate-Body Leakage	I _{GSS}		V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}		V _{DS} = 24V, V _{GS} = 0V			1	μA
			V _{DS} = 20V, V _{GS} = 0V, T _J = 55 °C			10	
Drain-Source On-State Resistance ¹	R _{DS(ON)}		V _{GS} = 4.5V, I _D =9A		9.7	13.5	mΩ
			V _{GS} = 10V, I _D = 9.5A		7.4	9.5	
Forward Transconductance ¹	g _{fs}		V _{DS} = 5V, I _D = 9.5A		62		S
DYNAMIC							
Input Capacitance	C _{iss}		V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		608		pF
Output Capacitance	C _{oss}				112		
Reverse Transfer Capacitance	C _{rss}				74		
Gate Resistance	R _g		V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		2.8		Ω
Total Gate Charge ²	Q _g	V _{GS} = 10V	V _{DS} = 15V, V _{GS} = 10V, I _D = 9.5A		14		nC
		V _{GS} = 4.5V			7.3		
Gate-Source Charge ²	Q _{gs}				2		
Gate-Drain Charge ²	Q _{gd}				3.7		
Turn-On Delay Time ²	t _{d(on)}			V _{DS} = 15V , I _D ≅ 9.5A, V _{GS} = 10V, R _{GEN} =6Ω		13	
Rise Time ²	t _r				37		
Turn-Off Delay Time ²	t _{d(off)}				48		
Fall Time ²	t _f				25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _J = 25 °C)							
Continuous Current ³	I _S					25	A
Forward Voltage ¹	V _{SD}		I _F = 9.5A, V _{GS} = 0V			1.1	V
Reverse Recovery Time	t _{rr}		I _F = 9.5A, dI _F /dt = 100A / μS		11.7		nS
Reverse Recovery Charge	Q _{rr}				3		nC

¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Package limitation current is 20A.

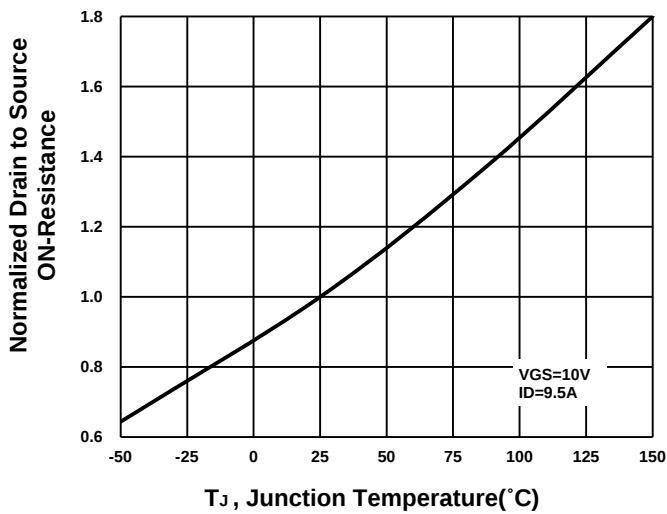
Output Characteristics



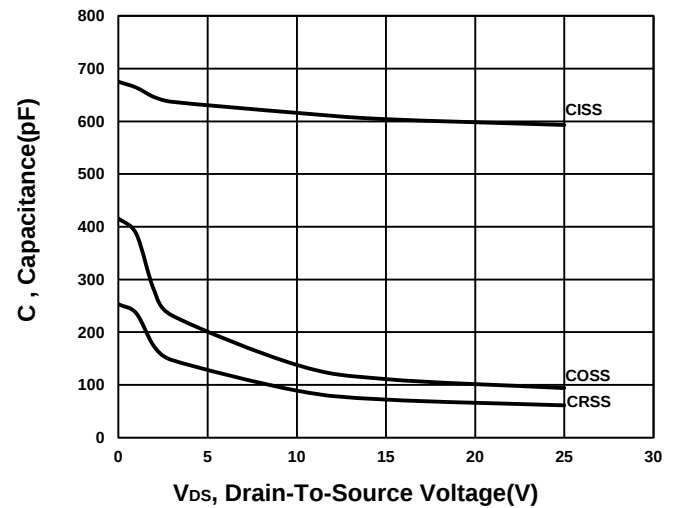
Transfer Characteristics



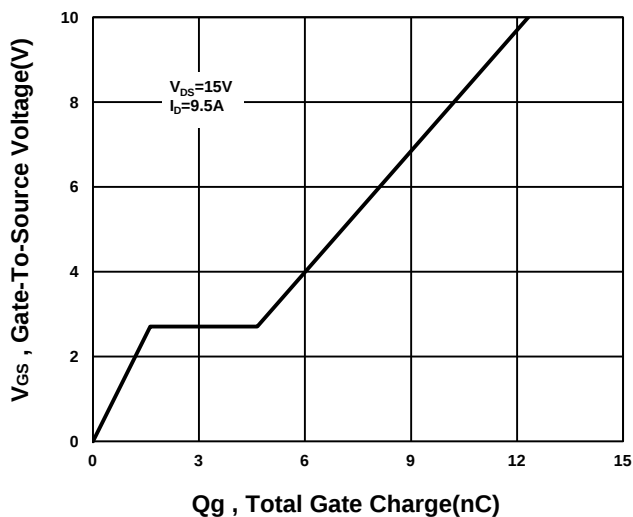
On-Resistance VS Temperature



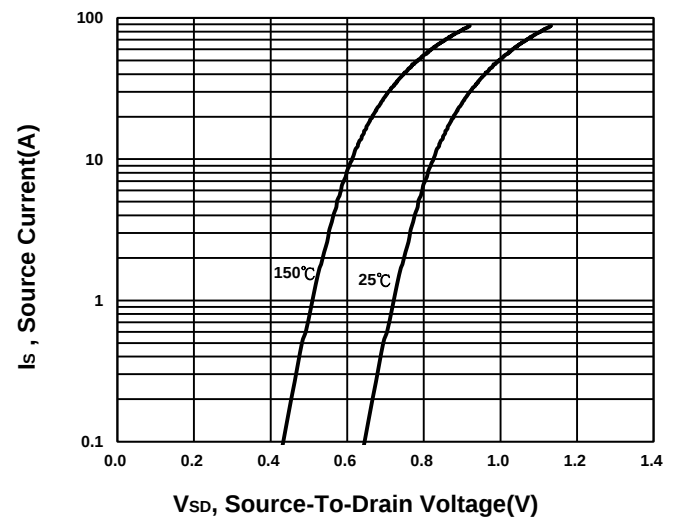
Capacitance Characteristic



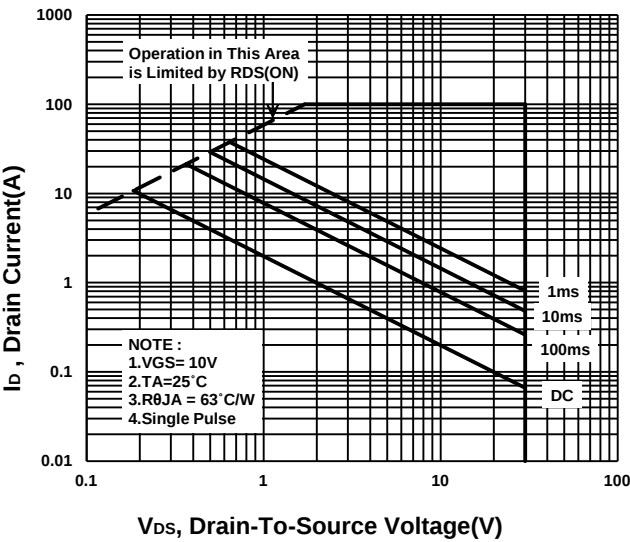
Gate charge Characteristics



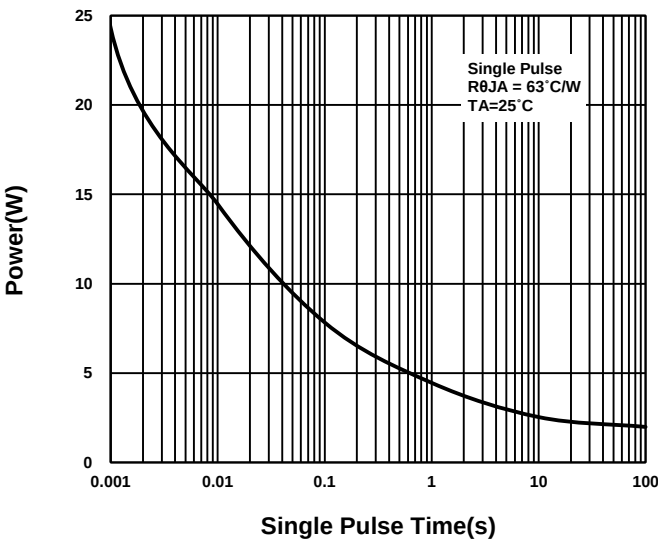
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

