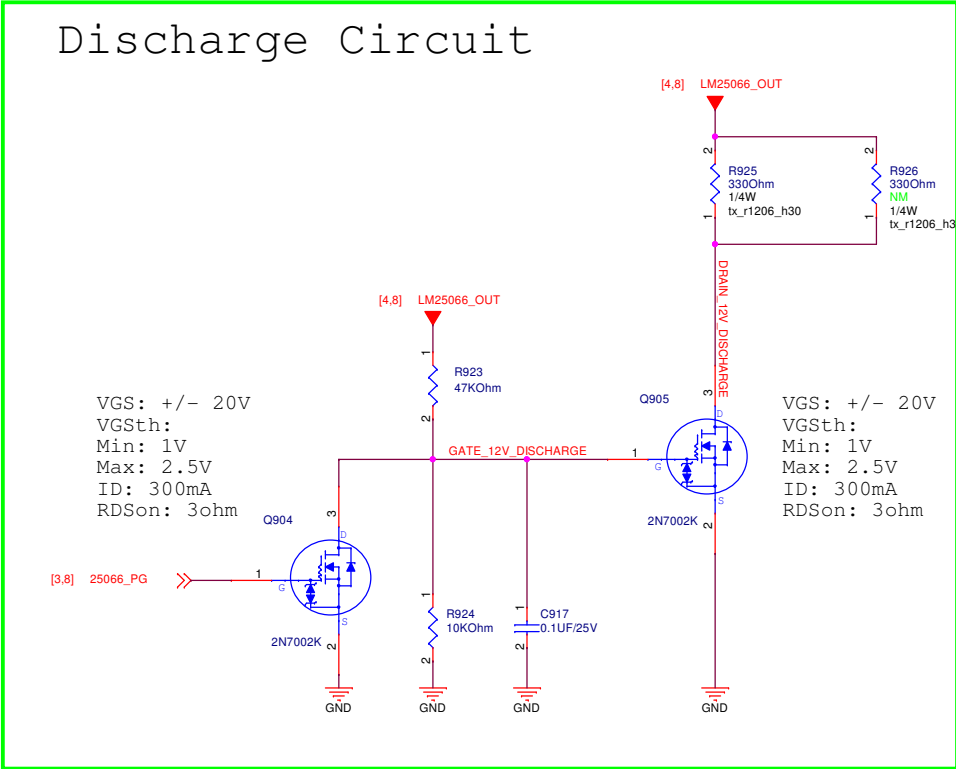
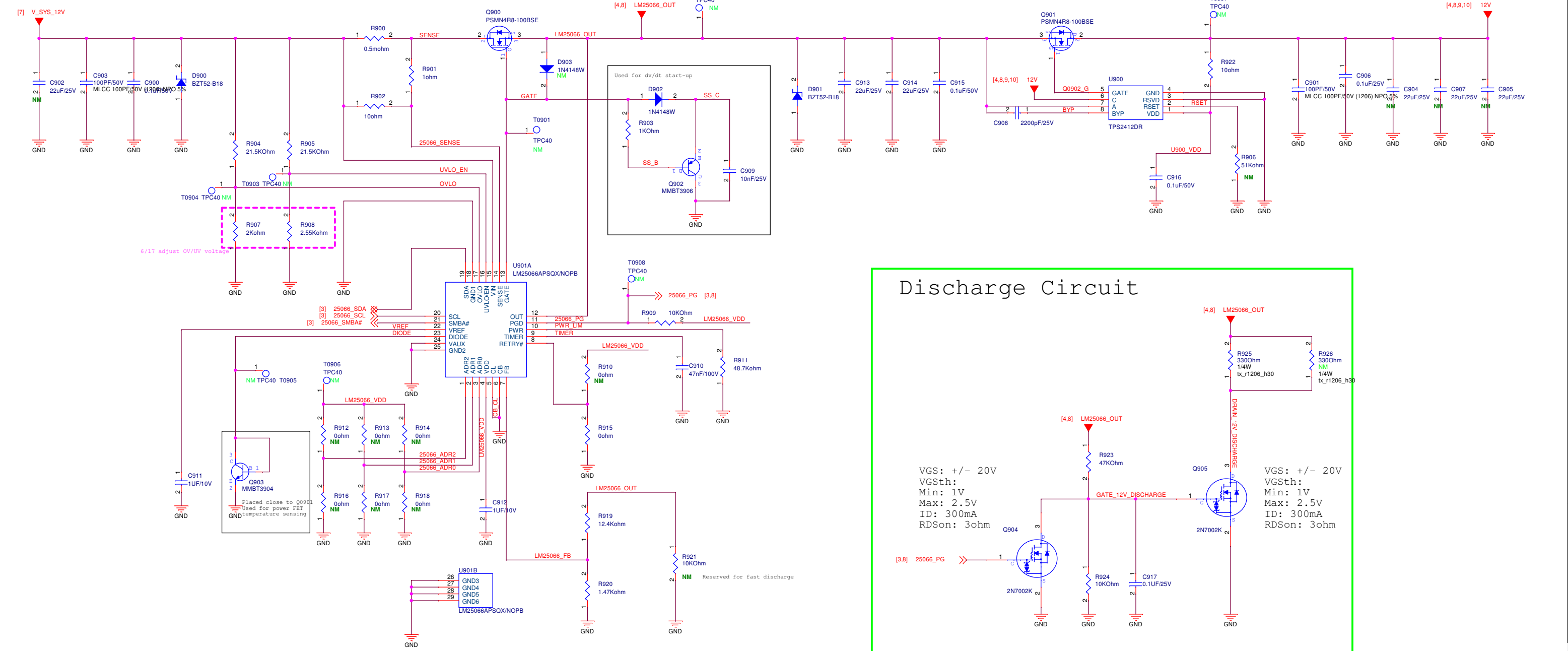




Design Summary		
R_S	0.5	mΩ
R_{CL1}	10	Ω
R_{CL2}	1	Ω
R_{PWR}	48.7	kΩ
C_T	47.00	nF
R_1	21.5	kΩ
R_2	2.87	kΩ
R_3	21.5	kΩ
R_4	1.87	kΩ
R_{FB1}	12.4	kΩ
R_{FB2}	1.5	kΩ
R_{PG}	10	kΩ
C_{IN}	0.01	μF
C_{VDD}	1	μF
C_{VREF}	1	μF
$D1, D3$	1N4148W-7-F	
$D2$	SK153-TP	
$C_{dv/dt}$	10	nF
Connect CL Pin to GND		
Connect CB Pin to GND		
Connect /Retry to GND		
$Q1$	PSMN4R8-100BSE	
#FETs required in parallel		
$Q2$	MMBT3904	
$Q3$	MMBT3906	
$Z1$	5.0SMDJXXX	

Design Results			
	Typical	Units	
Current limit	55.0	A	
Power Limit	617	W	
Circuit Breaker Current	99.0	A	
Startup Time	6.36	ms	
Insertion Delay	14.5	ms	
Fault Timeout	0.888	ms	
Restart Time During Fault	108.309	ms	
Upper UVLO Threshold	10.344	V	
Lower UVLO Threshold	9.850	V	
Upper OVLO Threshold	14.497	V	
Lower OVLO Threshold	14.002	V	
PGD Threshold	11.01108163	V	
PGD Hysteresis	297.6	mV	