TECH DAYS
Texas Instruments

Understanding, measuring, and reducing output noise in DC/DC switching regulators

Practical tips for output noise reduction

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Detailed agenda

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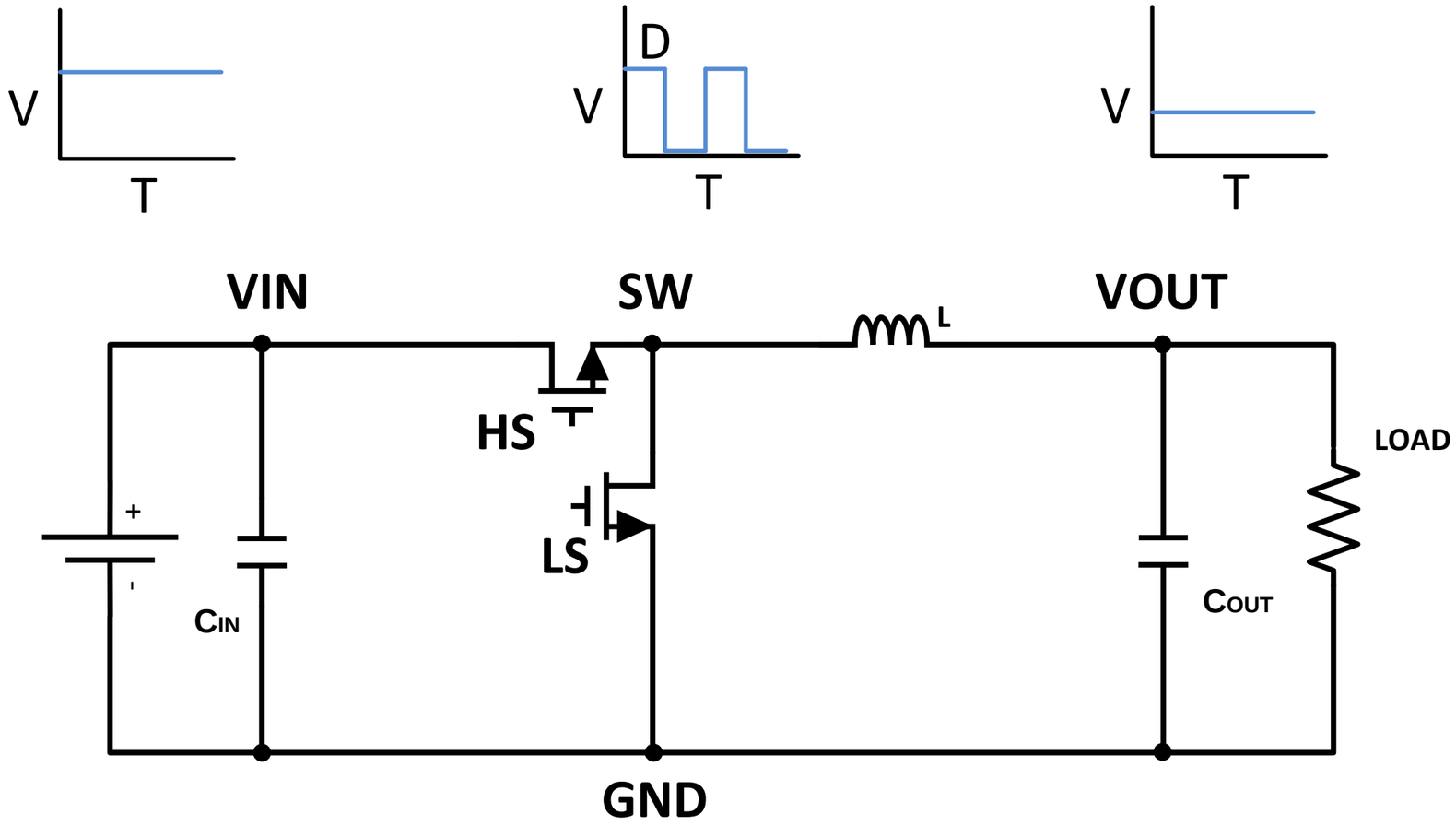
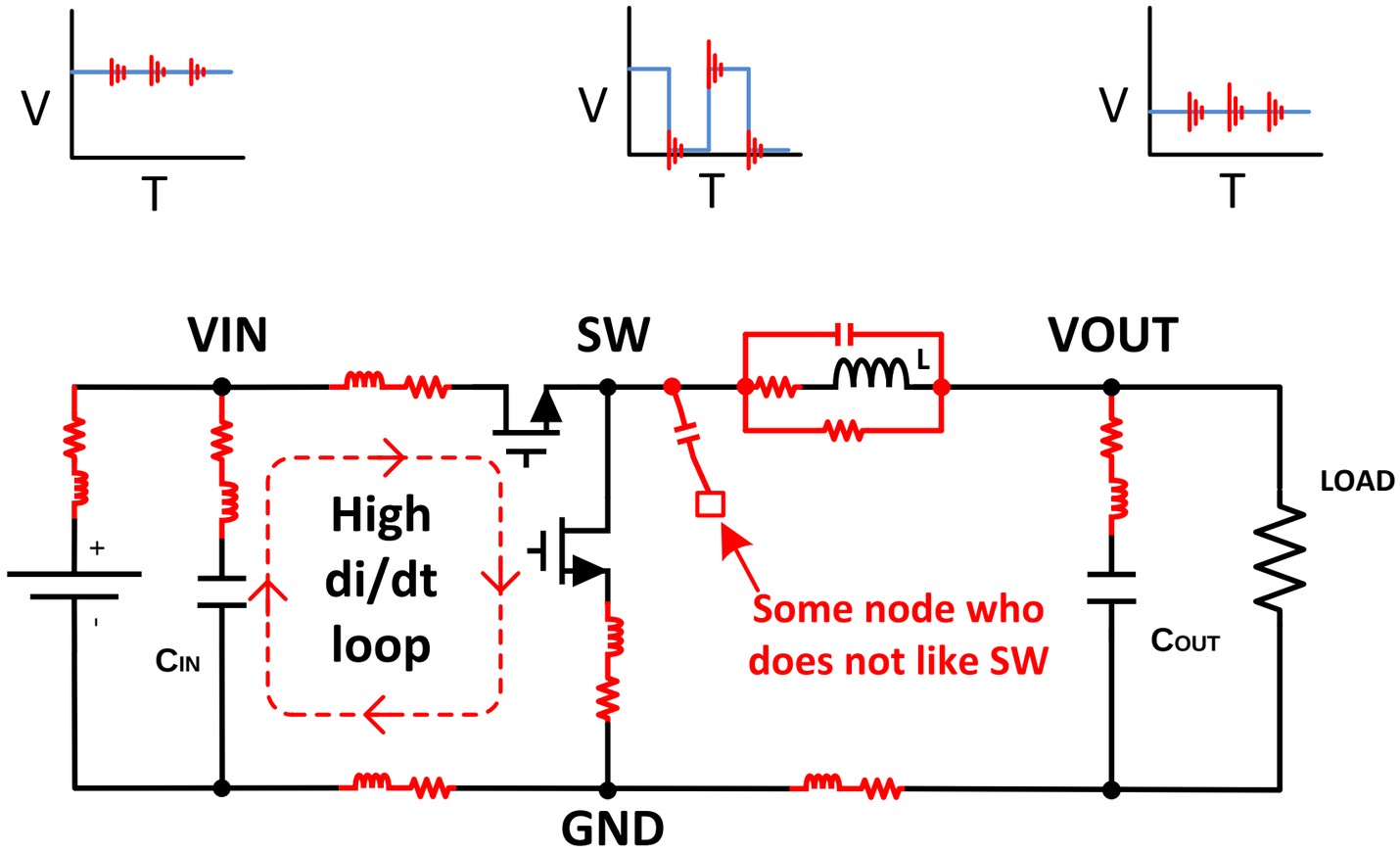
- Understanding the Noise Sources
  - DC/DC converter operation overview
  - Noise components (high frequency vs low frequency)
  - Relevant parasitic elements in the circuit
- Measuring Noise
  - What is “real” vs “fake” noise
  - Examples of measurement techniques (good vs. bad)
- Reducing Noise (high frequency and low frequency)
  - Layout techniques and comparison (good vs. bad)
  - Passive component selection and placement
  - Filtering techniques and examples

Understanding the sources of noise

The buck regulator

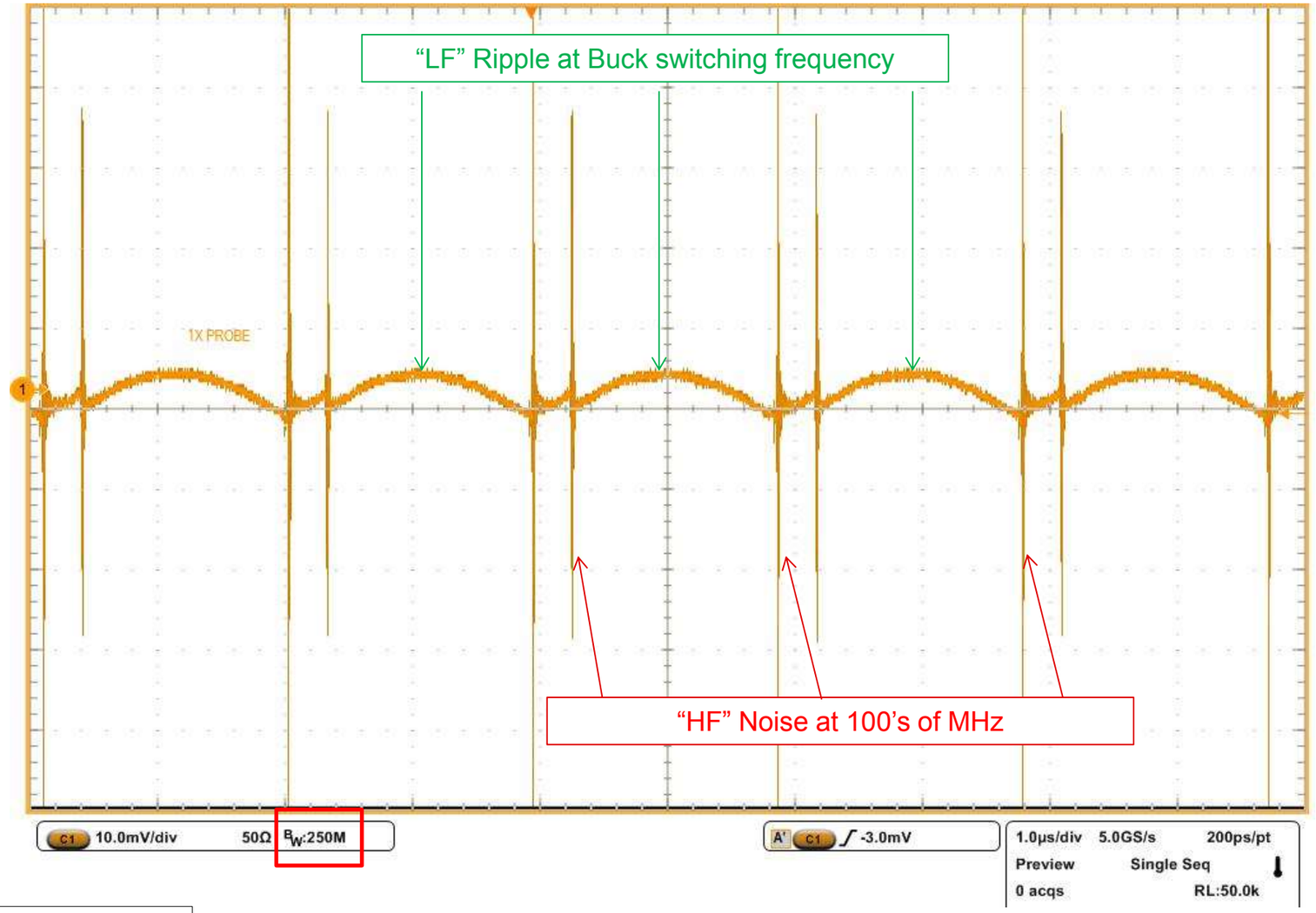


Less ideal buck regulator



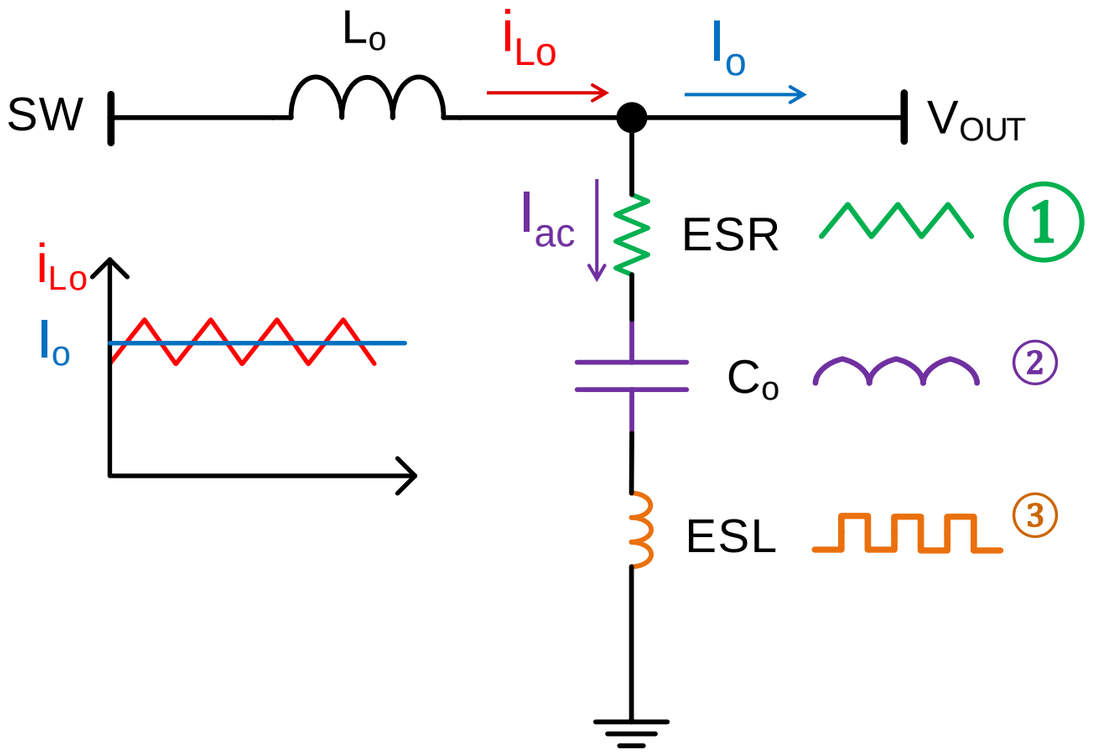
“Free” components in red

Output ripple and noise (example)



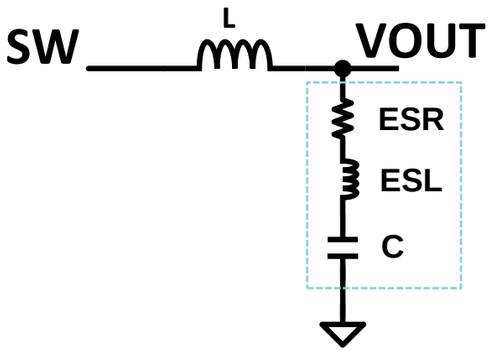
LF ripple origin

- Result of the inductor ripple current and output capacitor impedance



Total LF Ripple = ① + ② + ③

LF ripple with different capacitor types



"47µF" Capacitor

Inductor ripple current

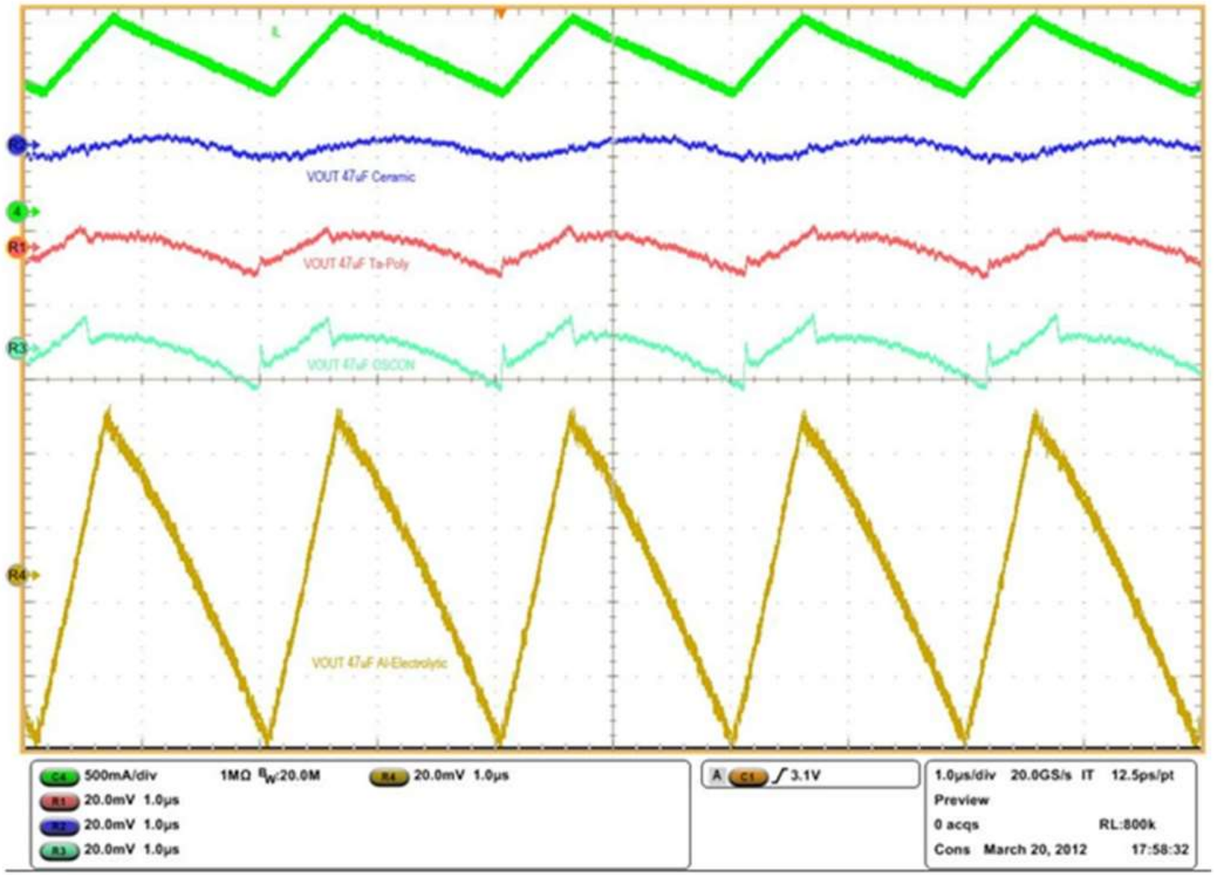
VOUT RIPPLE — Ceramic cap (C dominated, low ESR low ESL)

VOUT RIPPLE — Tantalum cap (medium ESR, some ESL)

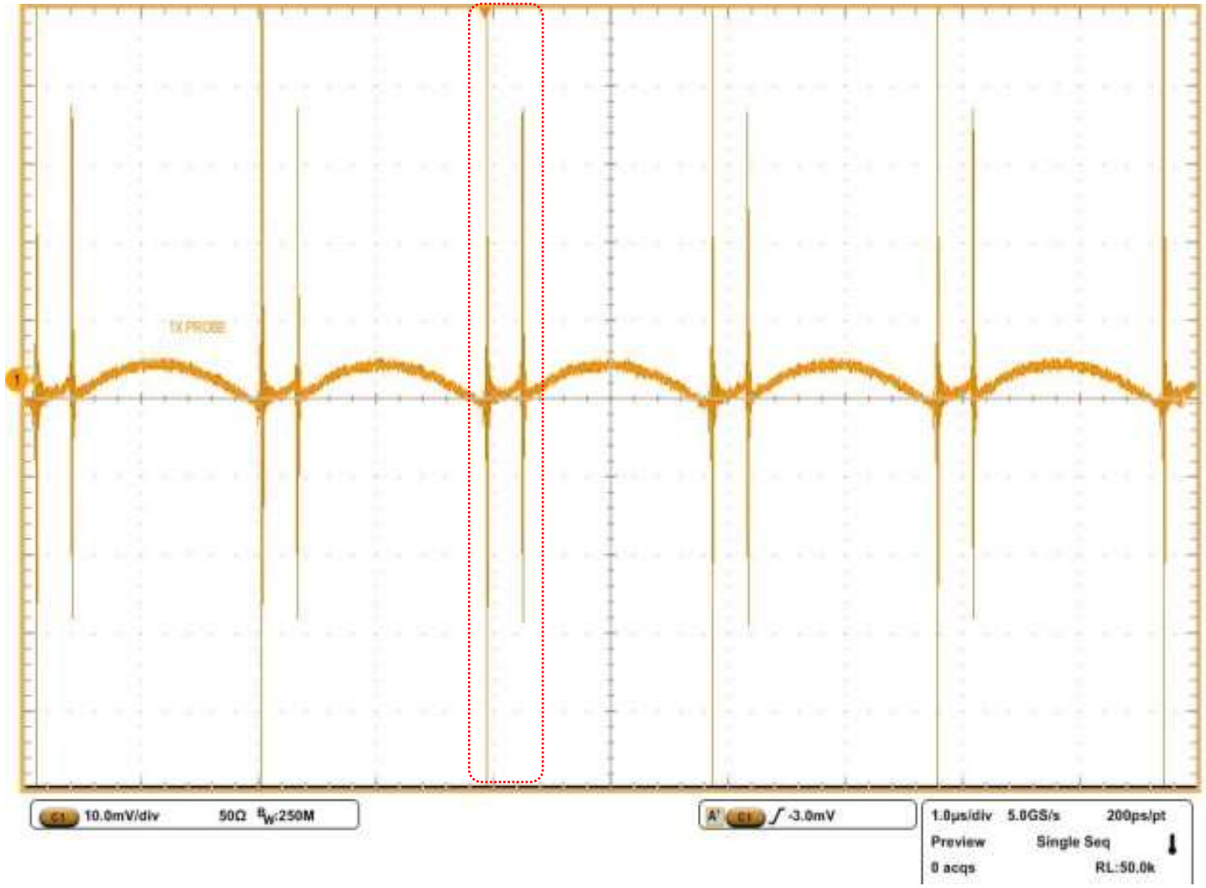
VOUT RIPPLE — OSCON cap (medium ESR, some more ESL)

VOUT RIPPLE — Aluminum Electrolytic cap (ESR dominated)

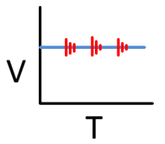
Each capacitor above is 47µF.
The difference is the chemistry

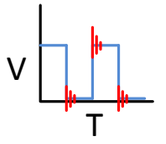


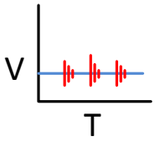
HF noise origin

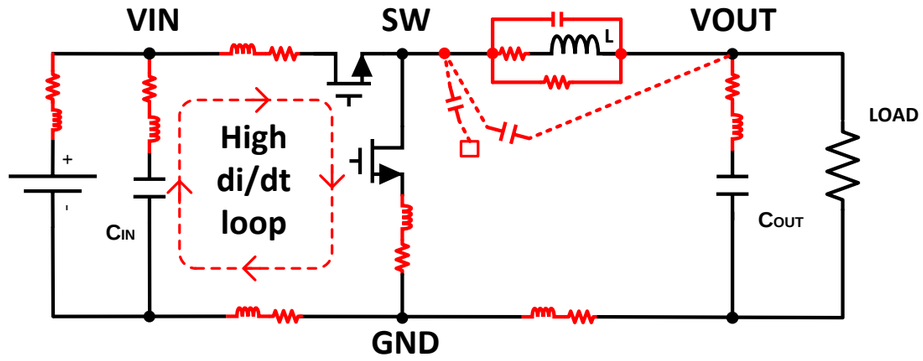


- Who is generating the noise?
  - High di/dt current loop and any inductance in its path
  - Noise appears on the SW node as ringing at each edge





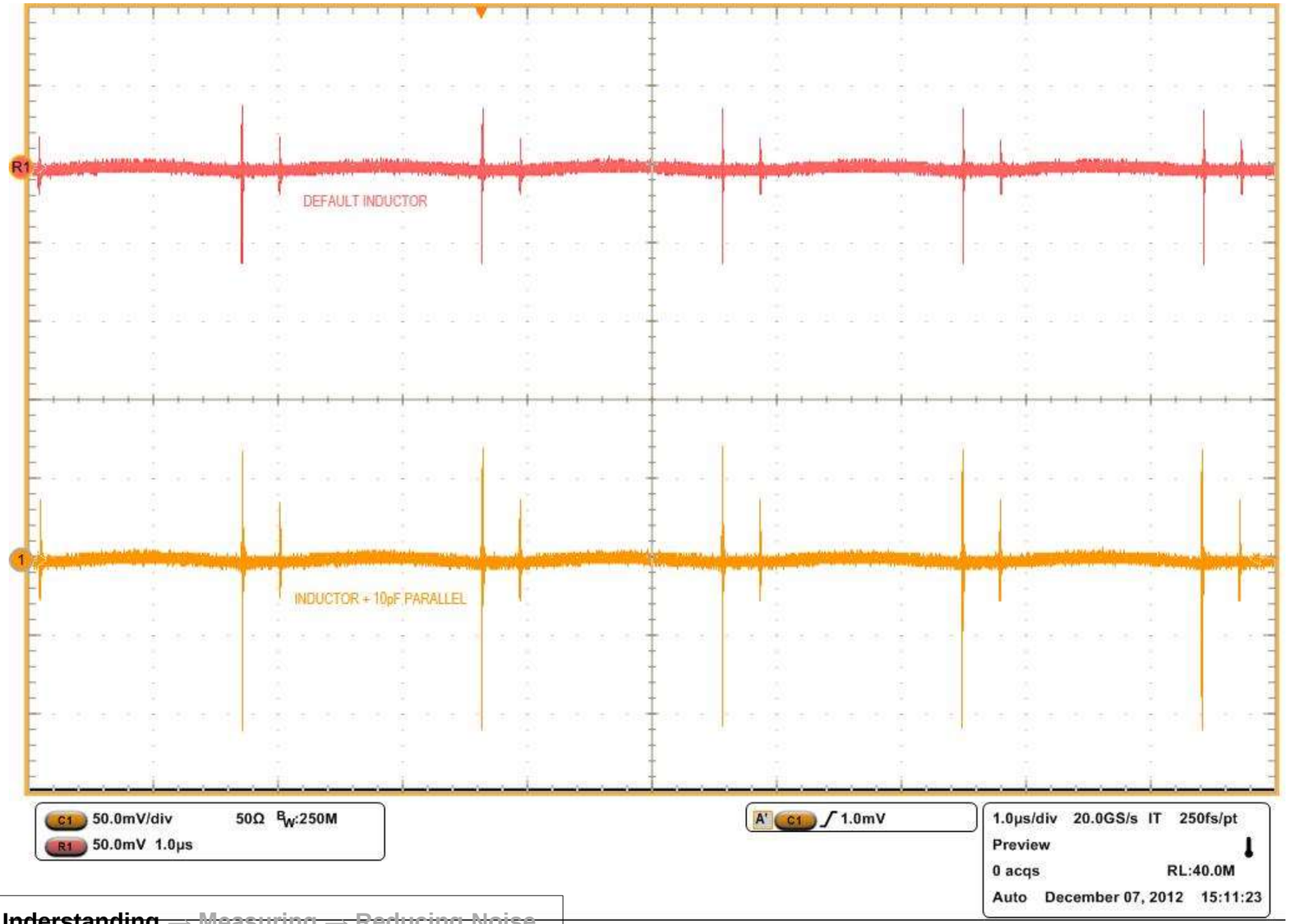




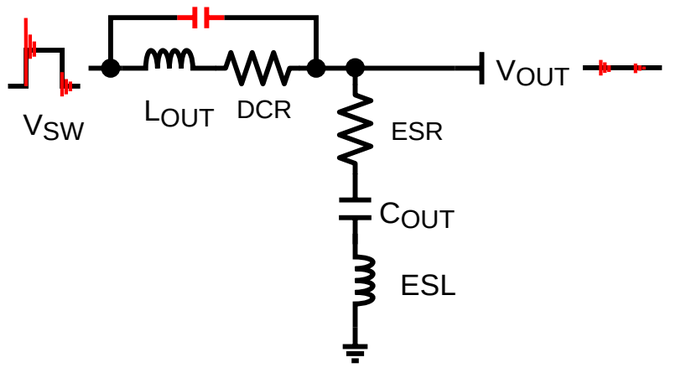
"Free" components in red

- How is the ringing coupled to the output?
  - Parasitic capacitance
    - Across the inductor (could be a few 10's of pF)
    - Between overlapping copper areas on the PCB

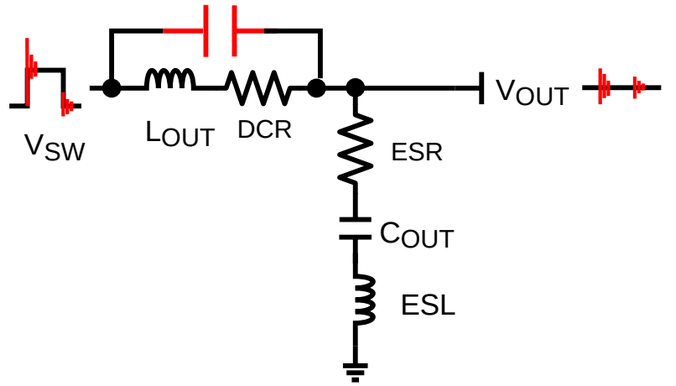
HF noise vs inductor parasitic capacitance



Inductor A



Inductor B

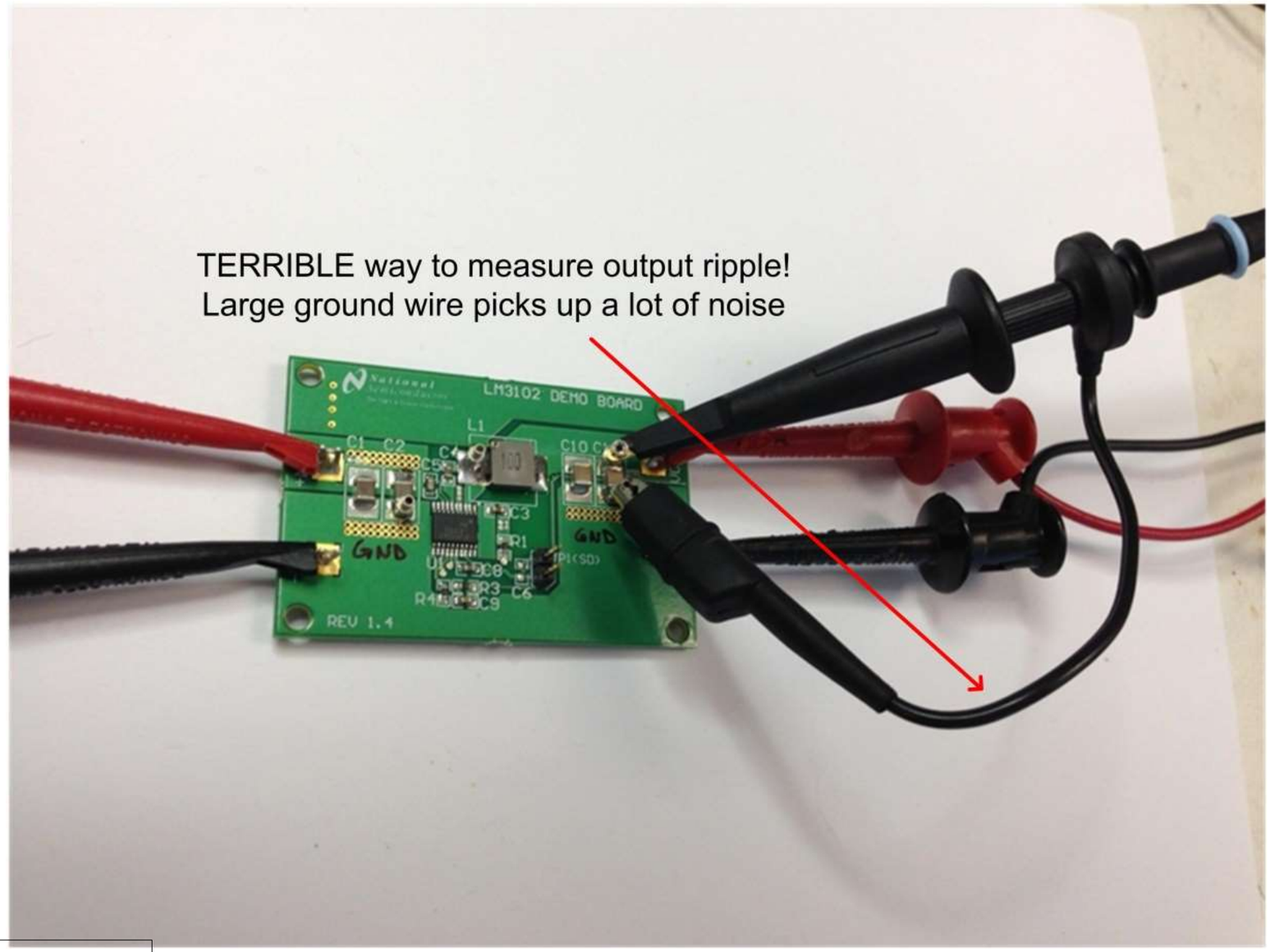


Measuring noise

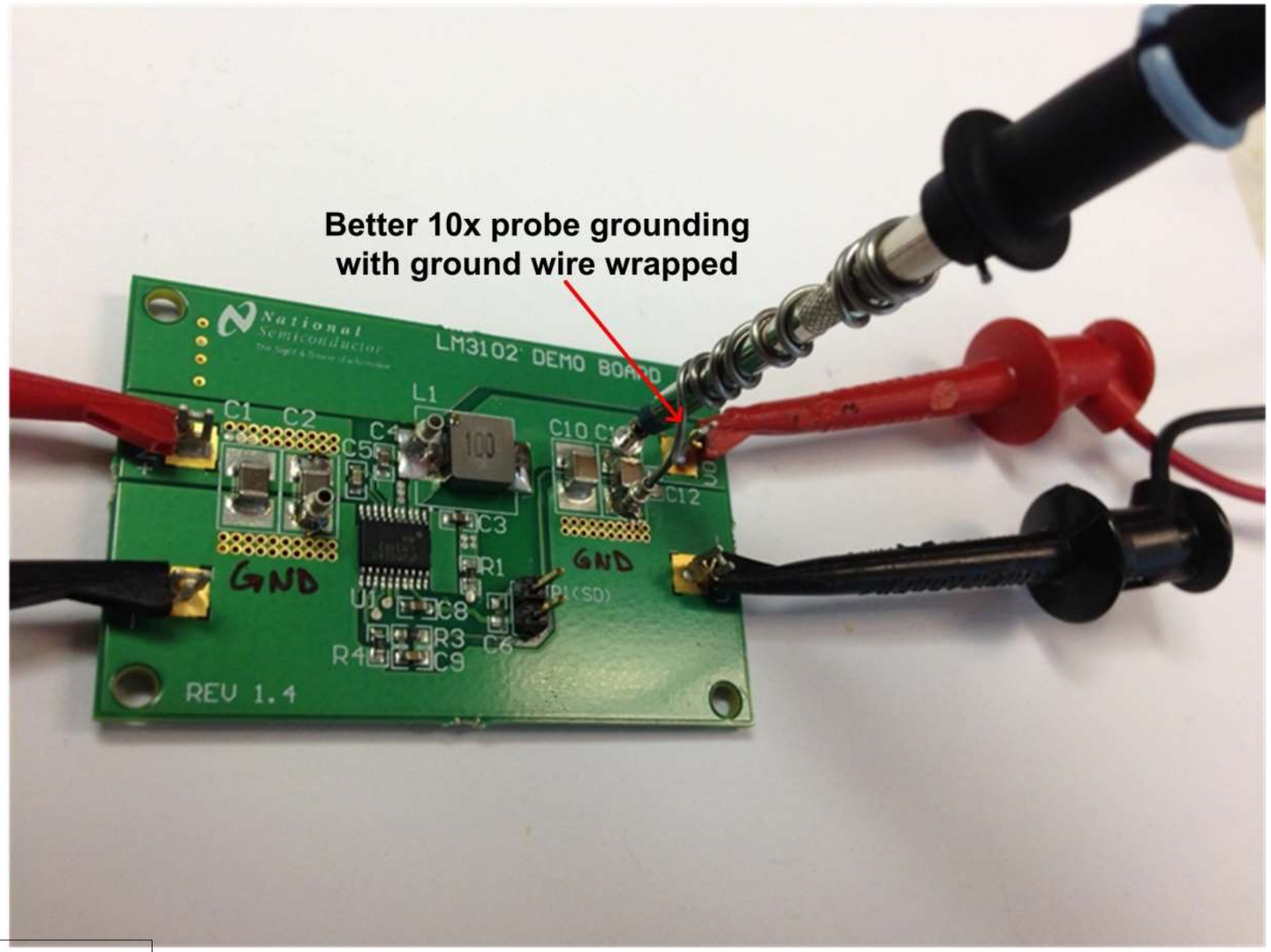
Measuring noise

- Before we explore ways/tools for reducing the output noise, let’s make sure we are measuring it properly.
- Improper measurement techniques can results in exaggerated output noise.
- Exaggerated output noise measurements can result in overly conservative “methods” for fixing it.
- It is important to know the “real” amount of noise before we start reducing it.

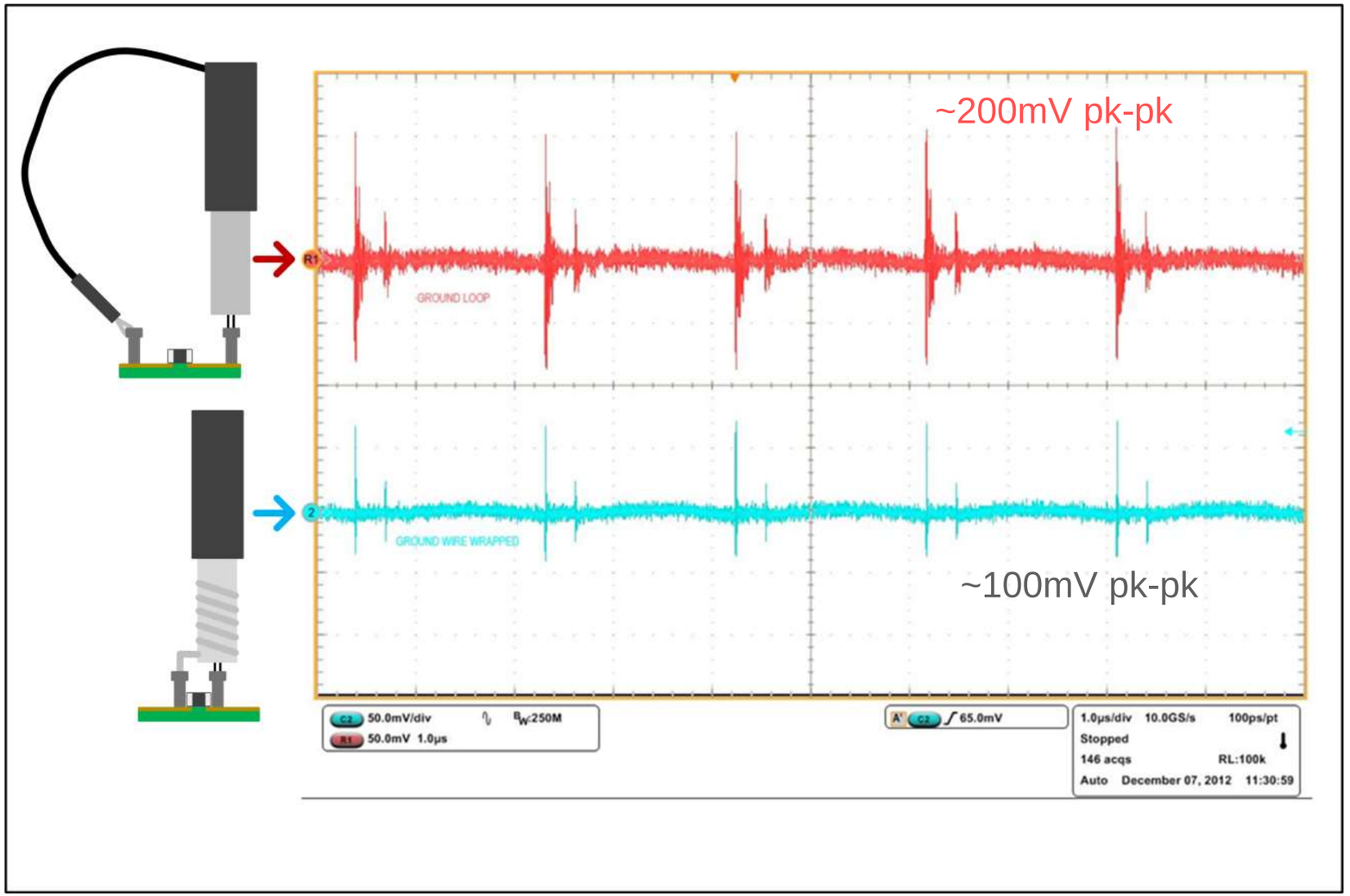
BAD Measurement (example)



Improved measurement (example)



Comparison

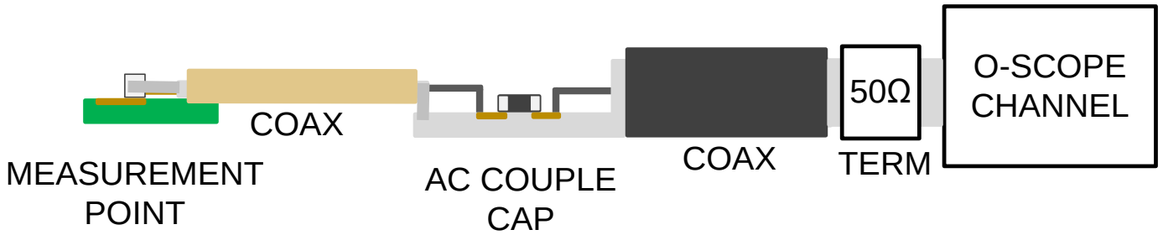


~2x difference in measured noise!

The circuit is exactly the same.
The difference is the measurement technique.

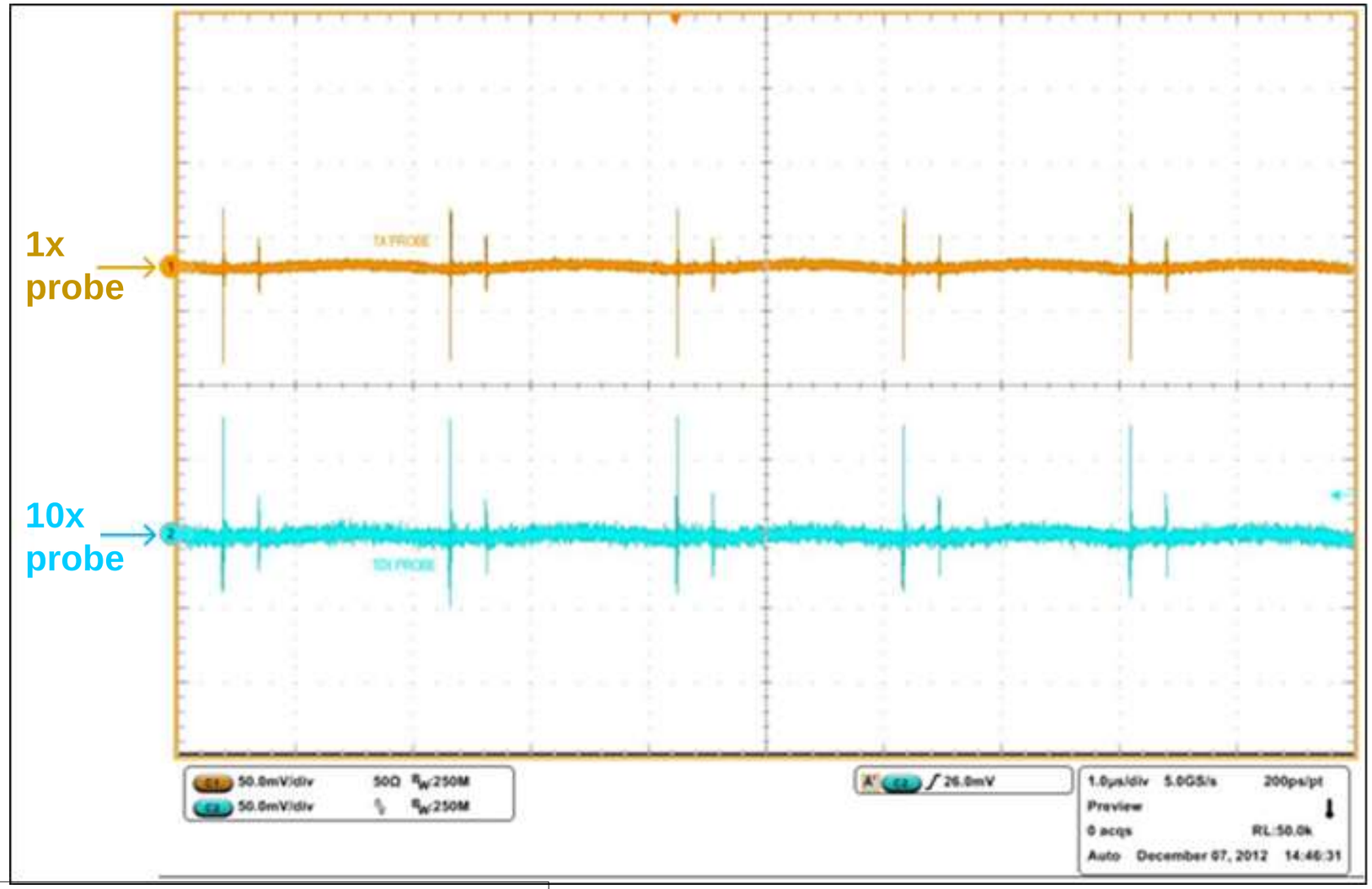
Making a 1x probe (example)

- Short coax cable soldered to the output
- 0.1µF coupling capacitor
- 50Ω termination



- Probe frequency response
- High pass filter with cutoff frequency at 31.8kHz. OK for most modern switchers with loaded output.
- Probe OK for 250MHz scope BW

Advantage of 1x probe



Cleaner reading
Can zoom to 1mV/div for sub 1mV measurements

Fuzzy due to the scope vertical sensitivity limitations of a 10x probe.
Cannot zoom below 10mV/div

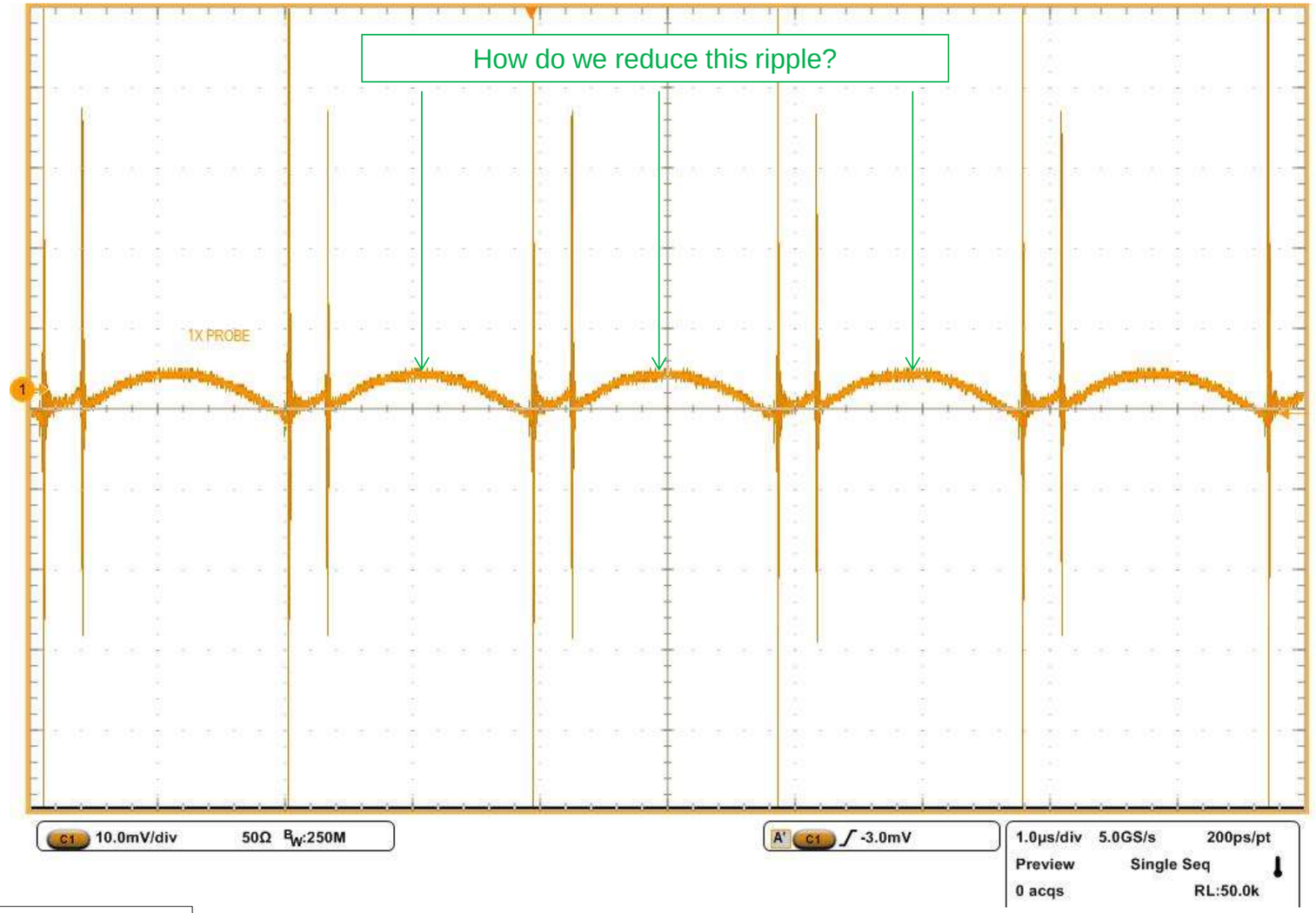
Reducing noise

Reducing noise - toolbox

- LF Ripple
  - Inductor vs Switching Frequency
  - Output capacitor
  - Post filtering
- HF Noise
  - Component placement
  - Component selection (with attention to packaging parasitics)
  - PCB routing and stack-up
  - Filtering
    - Input filters (conducted EMI)
    - Output filters (small HF capacitors)

LF ripple reduction

LF ripple reduction

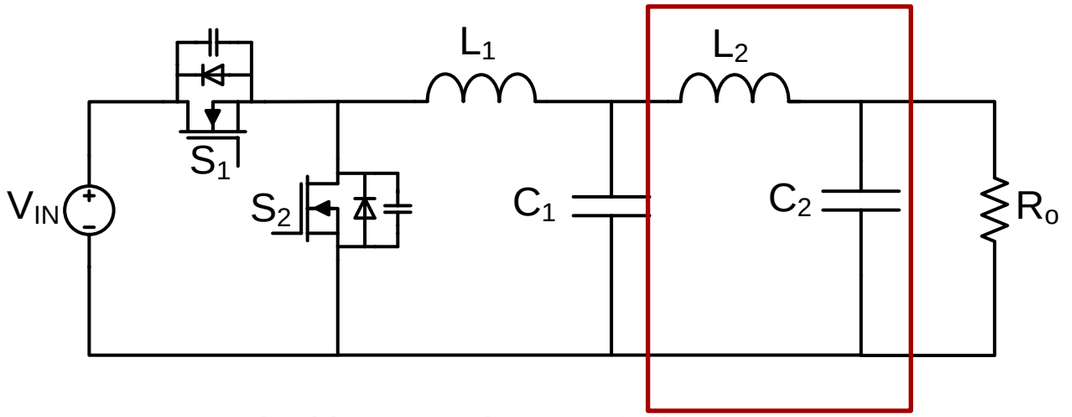


LF ripple – switching frequency and inductance

- We understand that the LF ripple is a function of the inductor ripple current and the output capacitor(s) impedance.
- We can:
  - **Lower the ripple current**
    - For the same inductor, increase the switching frequency
      - Tradeoff: increased switching losses
    - For the same switching frequency, increase the inductance
      - Tradeoff: increased solution size
  - **Lower the capacitor impedance**
    - Use low ESR and low ESL capacitors
      - Tradeoff: perhaps cost
    - Use multiple capacitors in parallel
      - Tradeoff: cost, board space

LF ripple – second stage filter

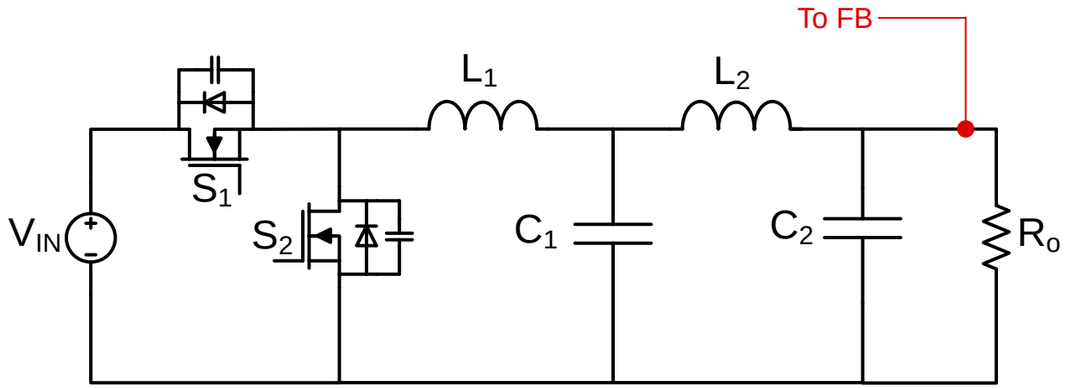
- Certain applications, such as test and measurement, are sensitive to the voltage ripple and routinely require very low output voltage ripple, such as 0.1%.
- To attain this level of attenuation it is required to add another pair of L and C to the output of a buck regulator as shown in the image below.



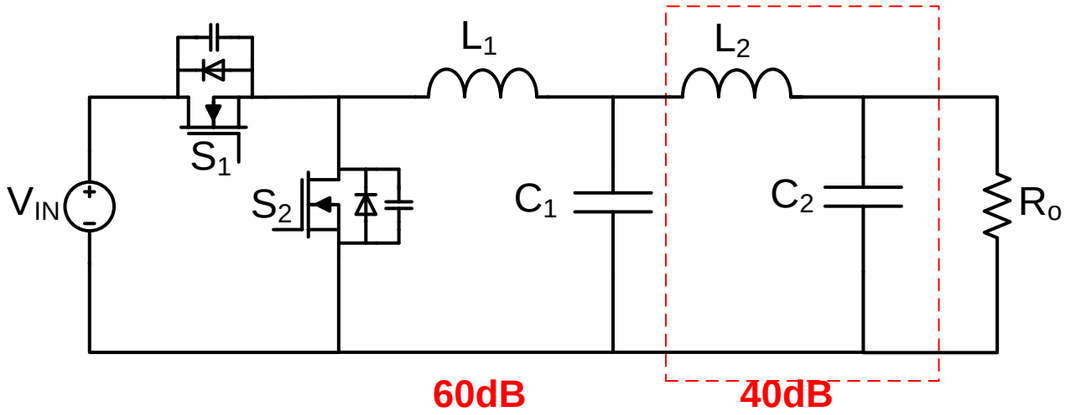
Buck with a second-stage LC filter

Second stage filter and output sense

- Common concern is how to position the 2nd stage filter – before or after the feedback (VOUT) sense point.
- **Assumption**: The second stage filter should be placed after the VOUT sensing point to avoid instabilities.
- **Reality:** Regardless of the connection the filter still interacts with the original output capacitance and there is resonance created.
- Connecting the filter before the VOUT sense:
  - allows us to account for it in the stability review
  - there is no load regulation penalty – resistive drop is compensated by the sense.



Second stage filter – component calculations

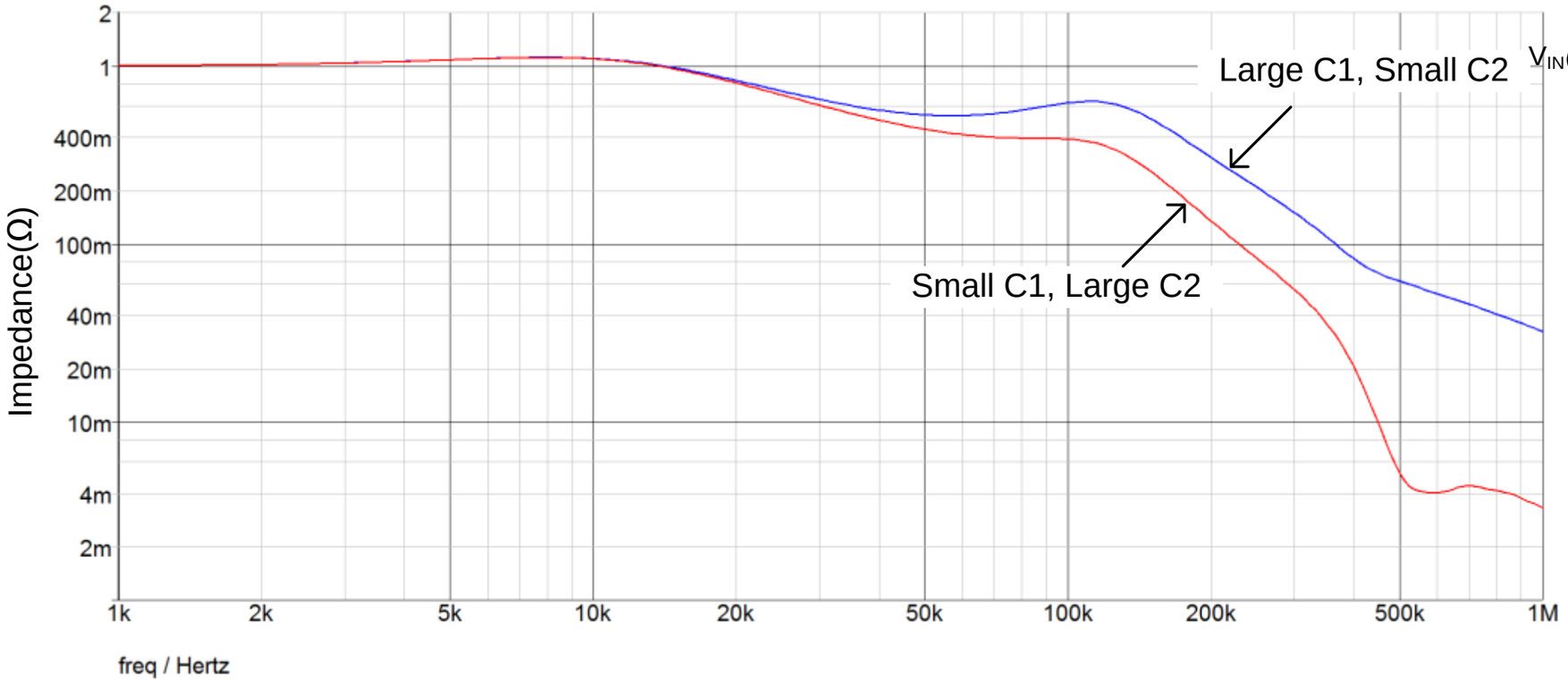


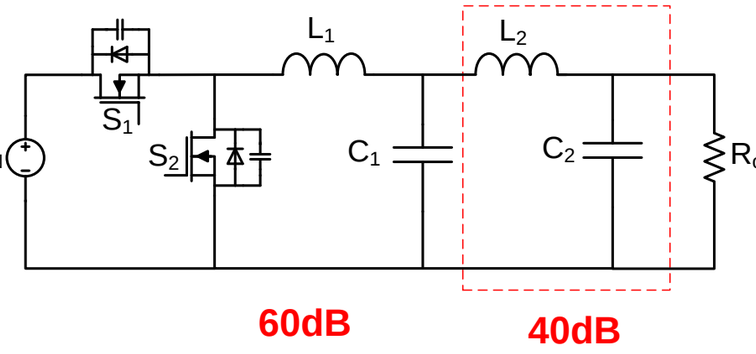
Buck with a second-stage LC filter

- Improper design of the second stage filter could make the converter unstable.
- Two objectives
  1. Attenuation
  2. Loop stability

Second stage filter – component calculations

- To ensure low impedance and to make sure the filter doesn't affect the loop substantially, the ratio of first stage (C1) to second stage capacitance (C2) is set to 1:10
- The value of the secondary inductor is then chosen for the remainder 40dB attenuation.





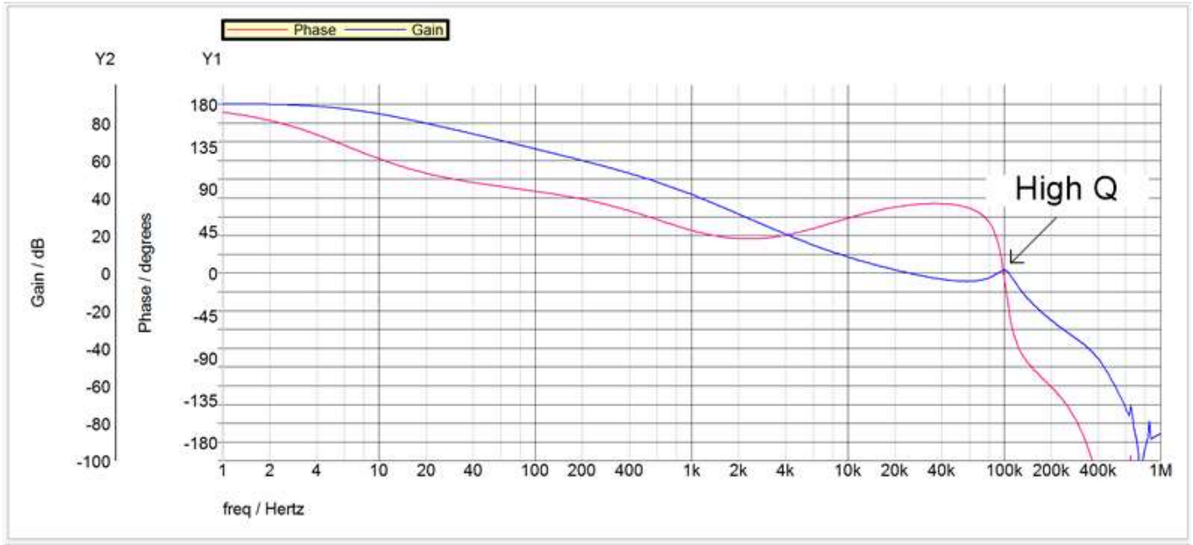
Steps:

1. Calculate L1 (usually based on ripple current)
2. Calculate C1 based on the 1st stage attenuation
3. Set C2 to be 10 x C1
4. Calculate L2 based on the 2nd stage attenuation

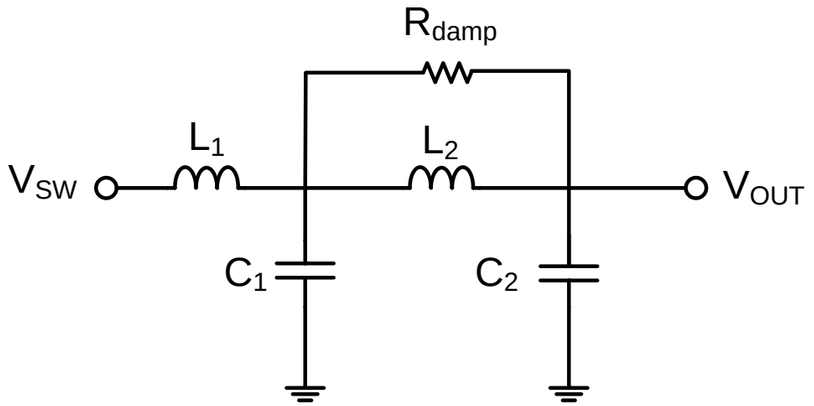
Closed output impedance with different filter designs

Second stage filter – Q and damping

- There may be a need to add a damping resistor in parallel with the inductor



High Q results in low phase margin



Placing the resistor parallel to the inductor damps the Q

Second stage filter – choosing Rdamp and L2

- LMZM23601 with second stage filter.

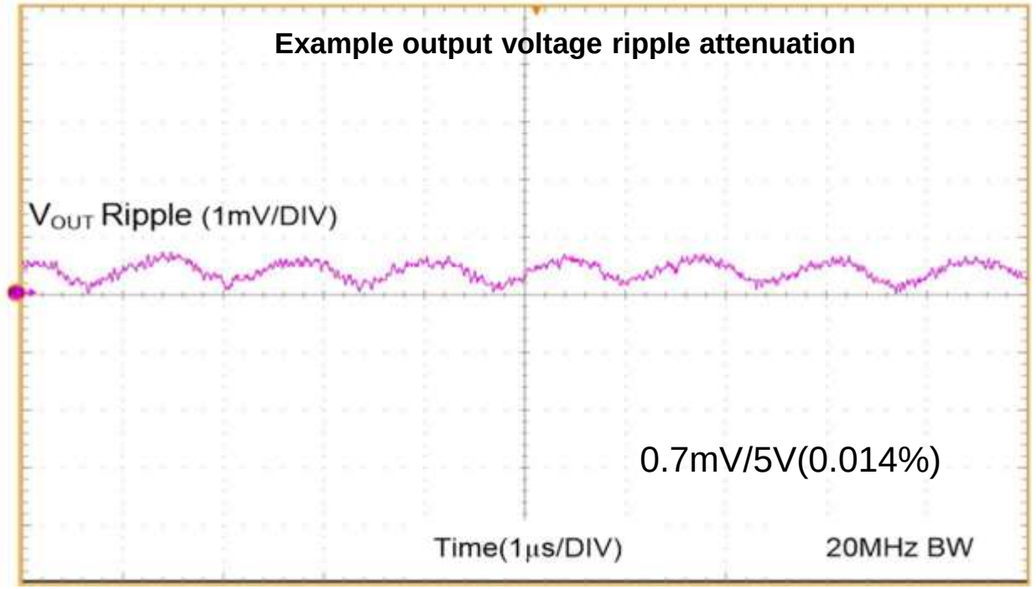
Filter Calculator with Equations

LMZM23601 with a second-stage filter

Second stage filter - results

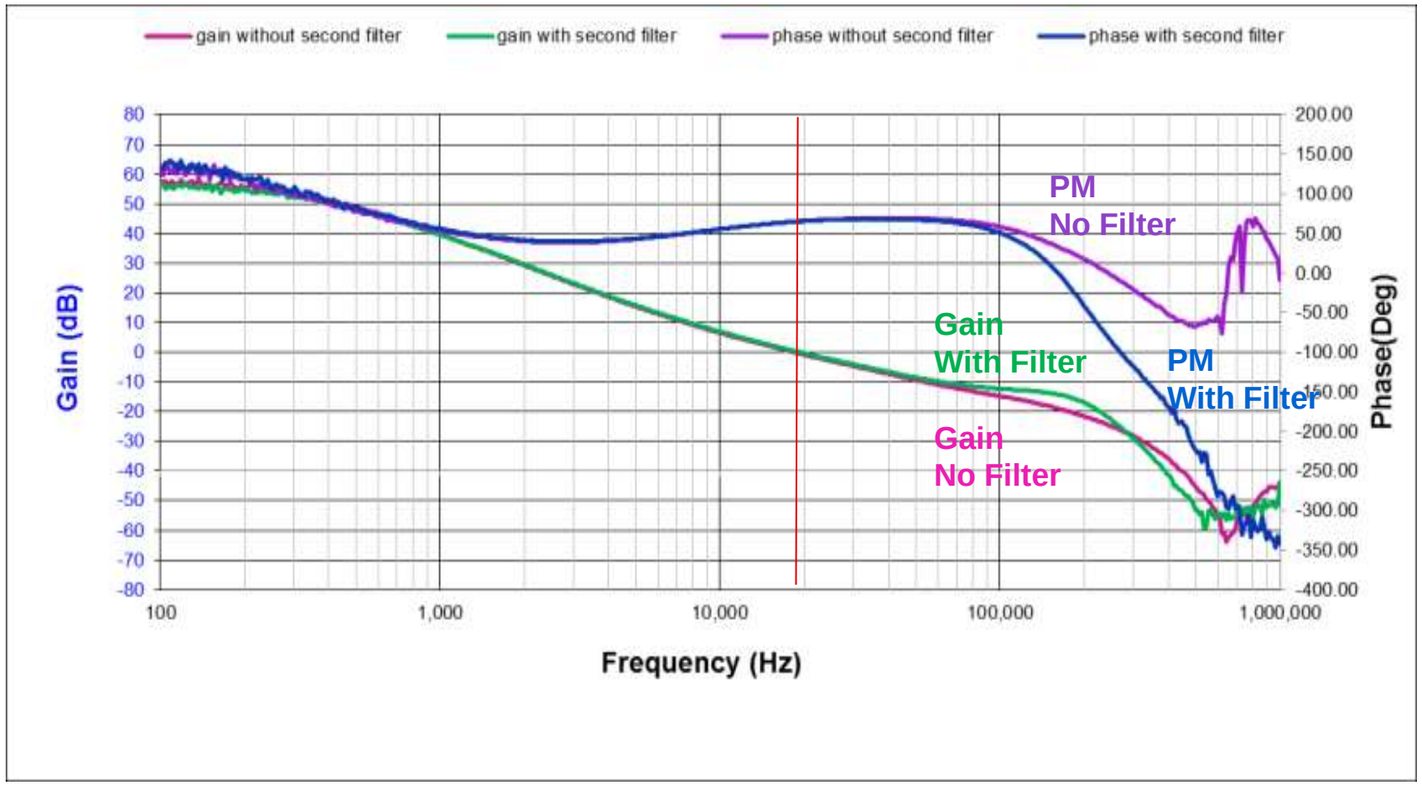
- LMZM23601 with second stage filter.

Attenuation



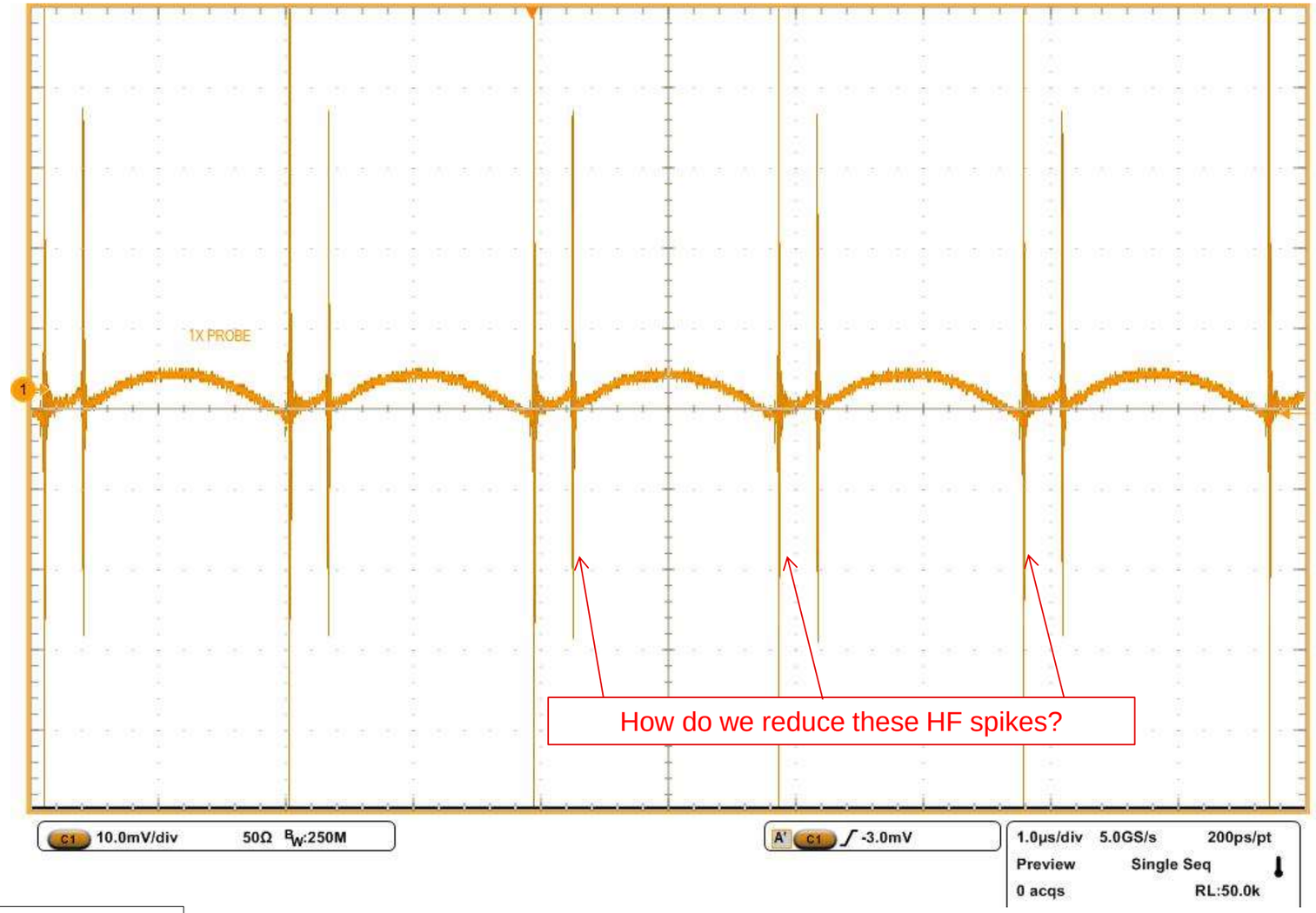
Stability

Bode plot with and without the second-stage filter



HF noise reduction

HF noise reduction



HF noise reduction – component placement

- First step is to optimize (minimize) the area of the **high di/dt loop**.
- For Buck, the high di/dt loop is formed by the input capacitor and the power MOSFETs (switches).
  - Input capacitor as close as possible to IC = Smaller loop area
  - Smaller loop area = Lower ringing on SW node
  - Lower ringing on SW node = Lower output noise
- So first step = optimize input capacitor placement for Buck

HF noise reduction – component placement

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- For a Buck converter…
  - The **INPUT cap** position affects the **OUTPUT noise**!
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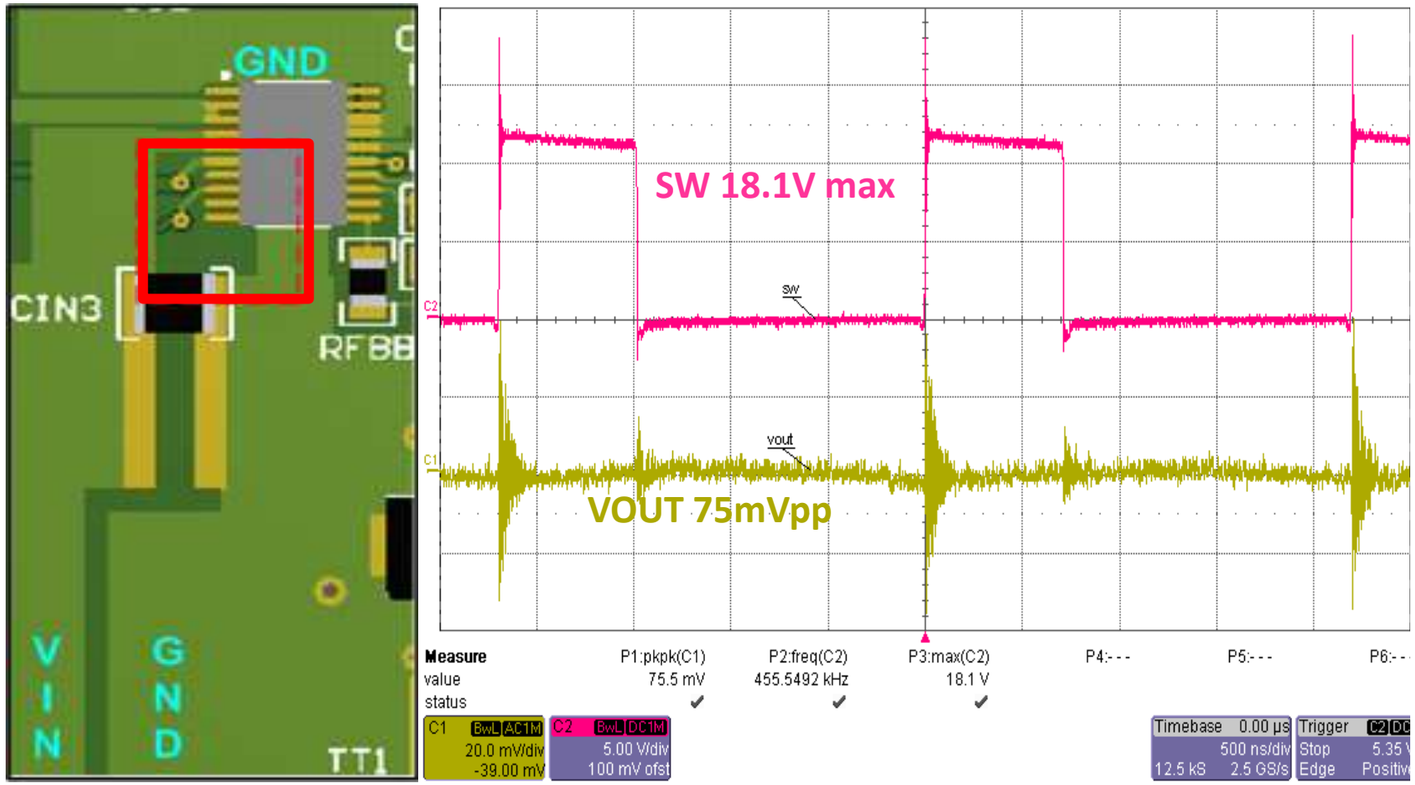
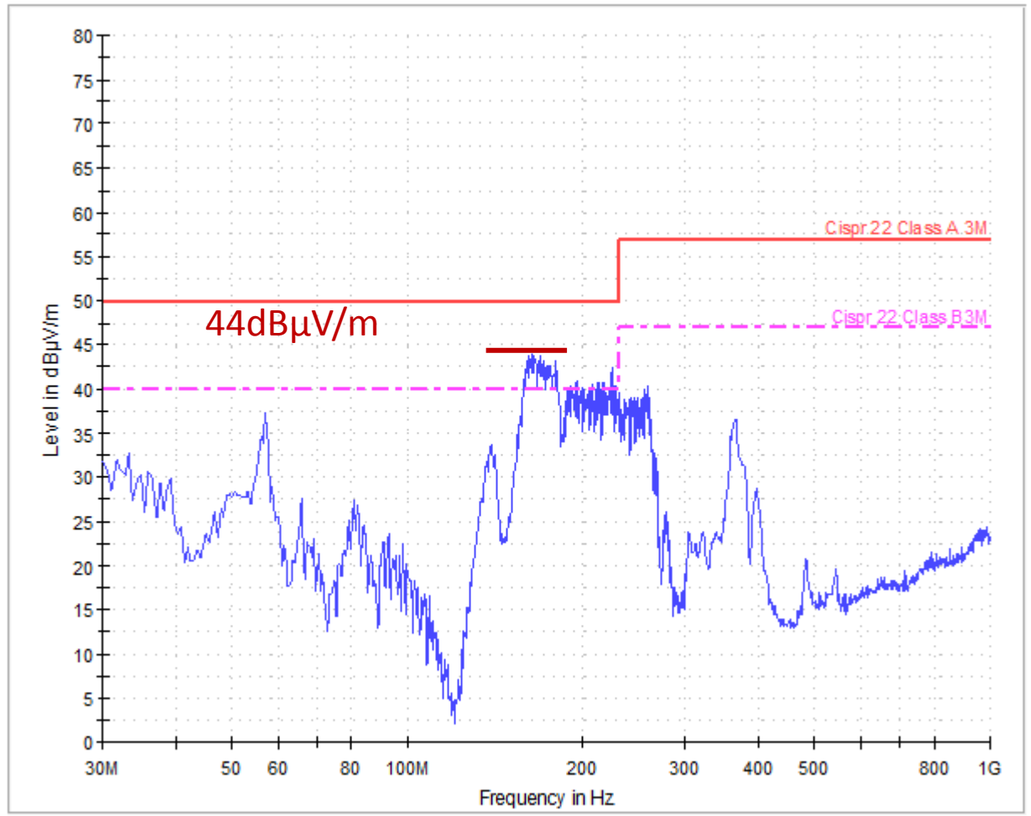
High di/dt capacitor placement - example

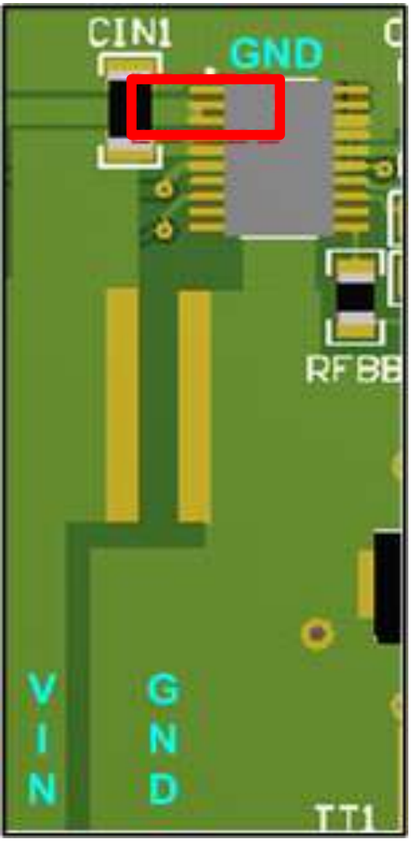
- Buck Regulator comparison with Cin location
- 12V input, 3.3V output, 2A Buck

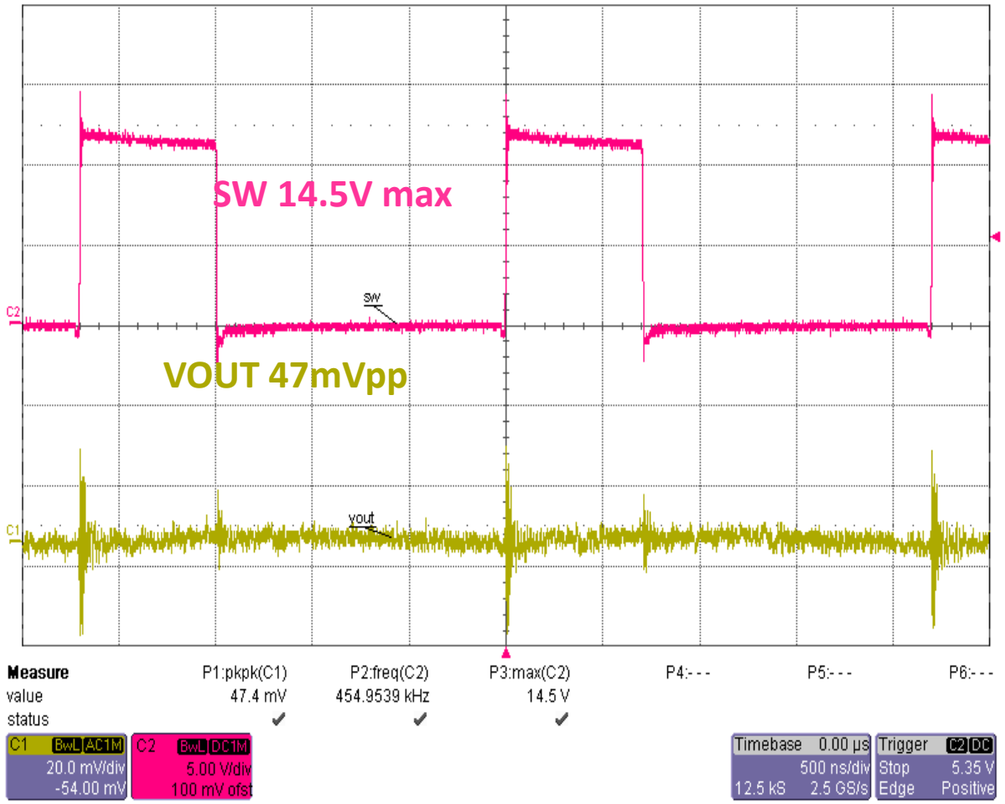


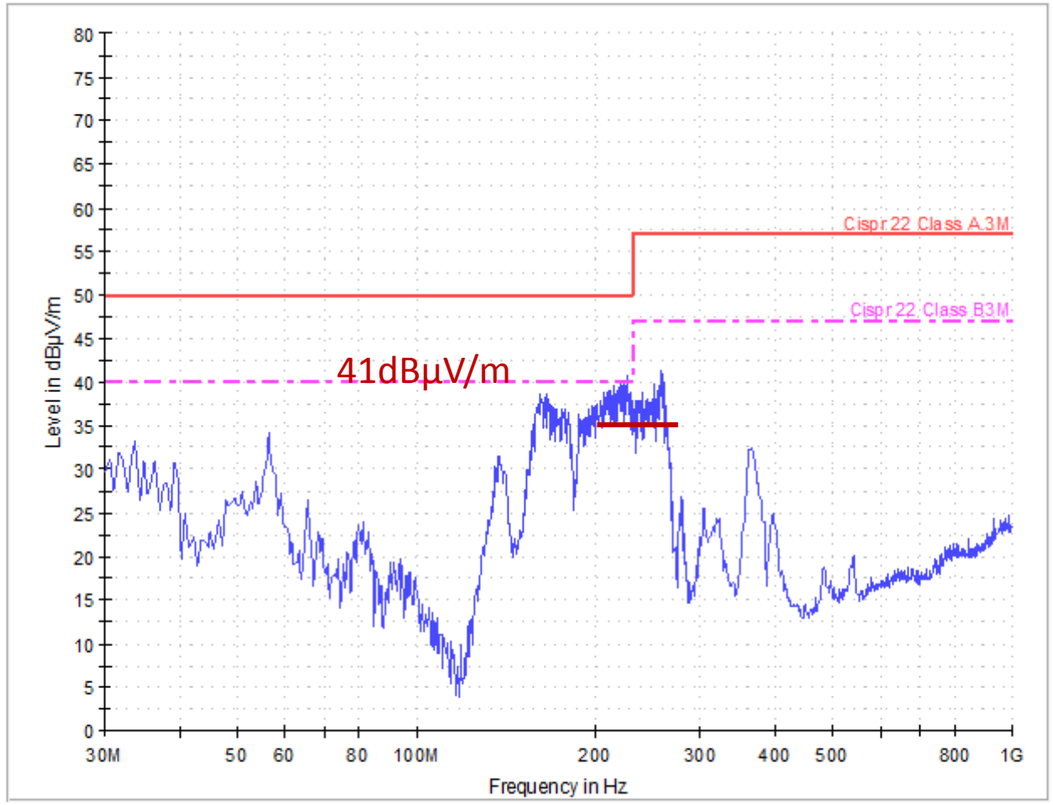


High di/dt capacitor placement - example

- Buck Regulator comparison with Cin location (2 times smaller loop area)
- 12V input, 3.3V output, 2A Buck

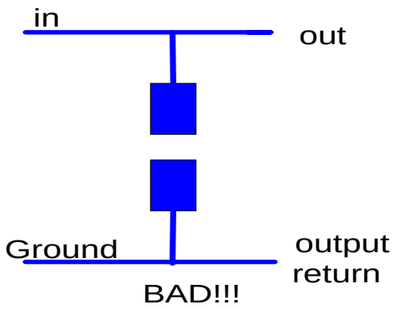


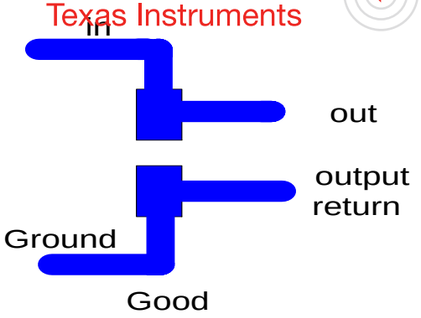


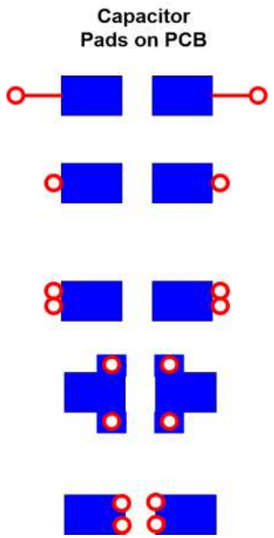


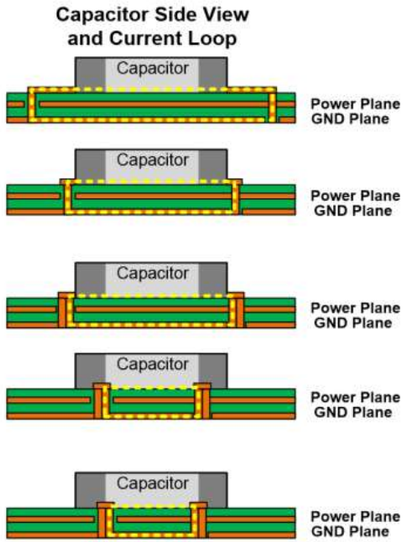
Bypass capacitor routing - example

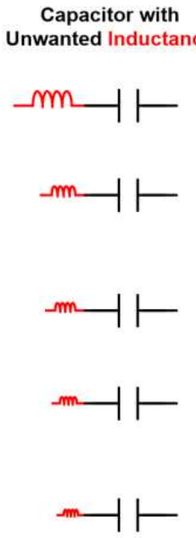
- **Place bypass capacitors on same side of board as component being decoupled**
- **Locate as close to pin as possible**
- **Keep trace width thick and short**

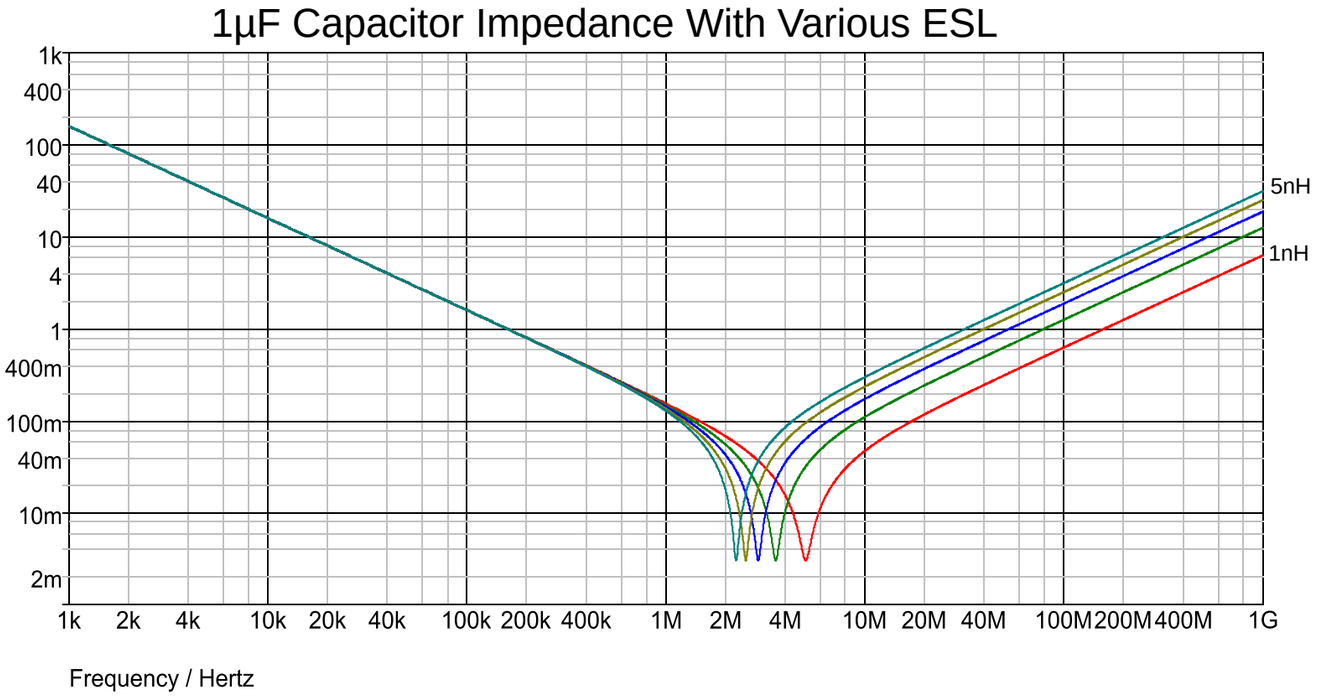






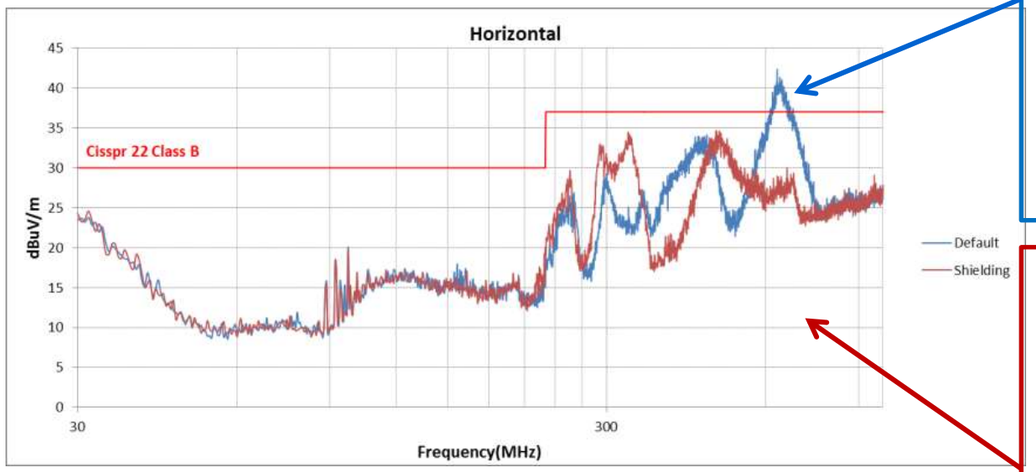


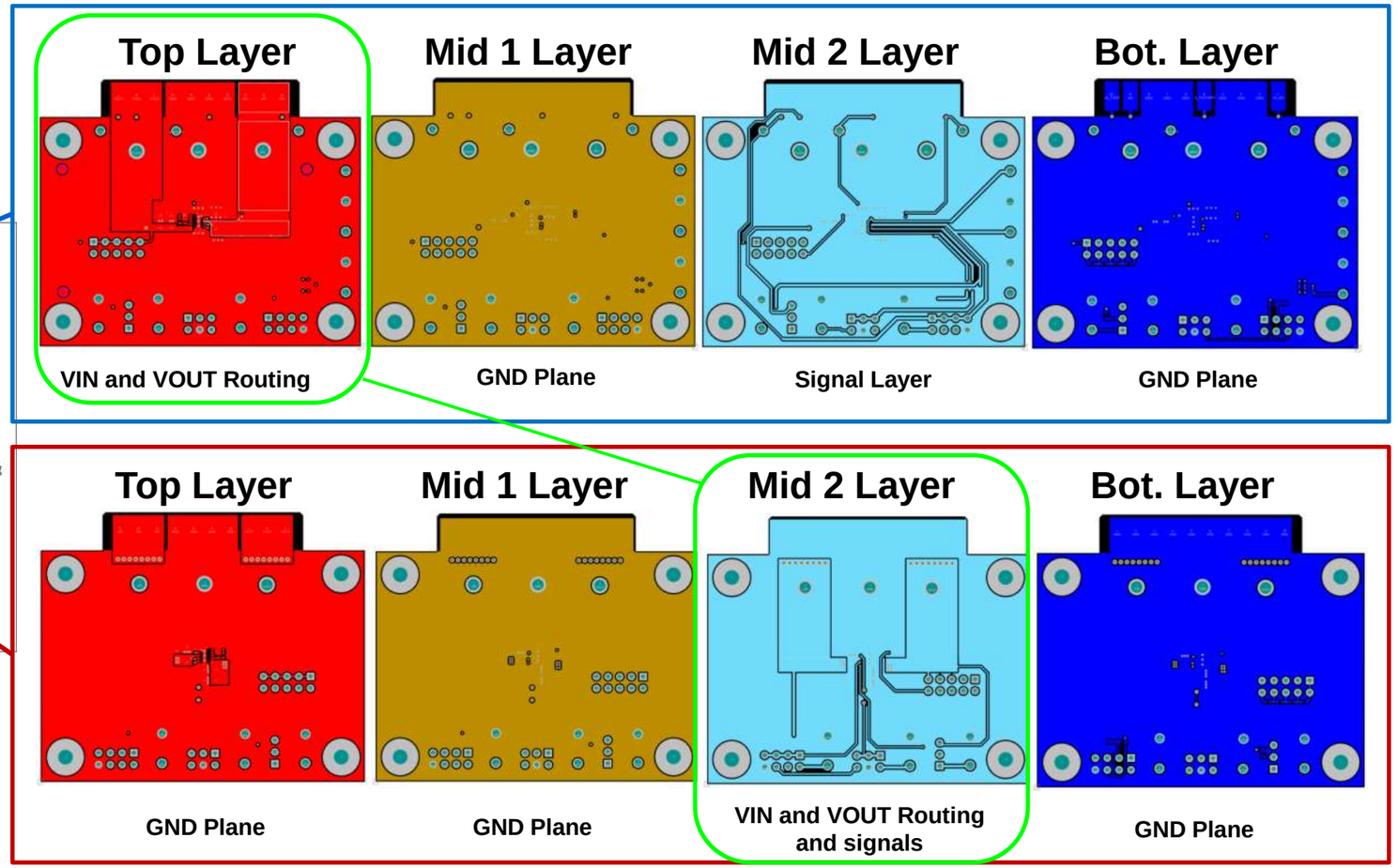




HF noise reduction – board layout tricks

Shielding

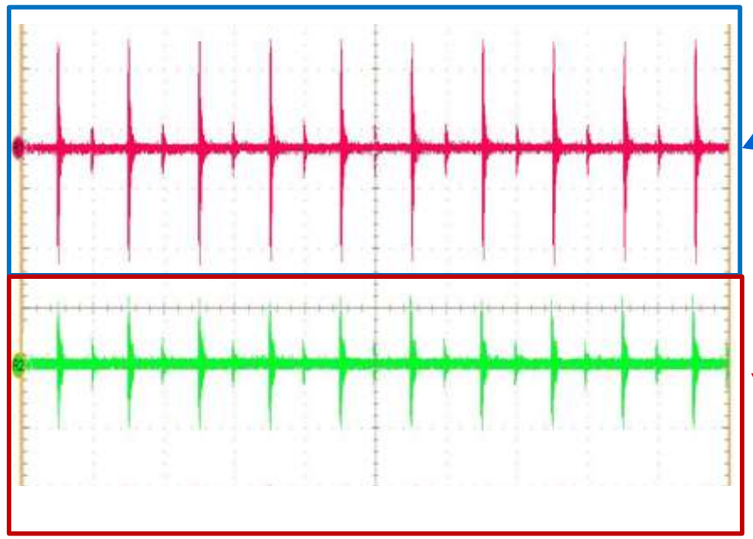


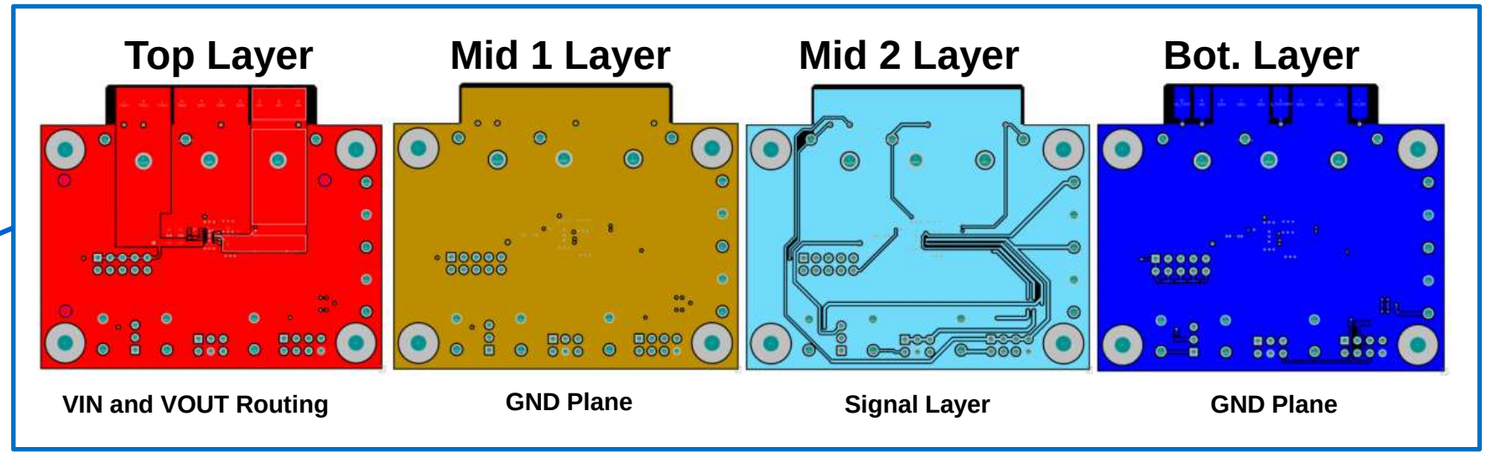


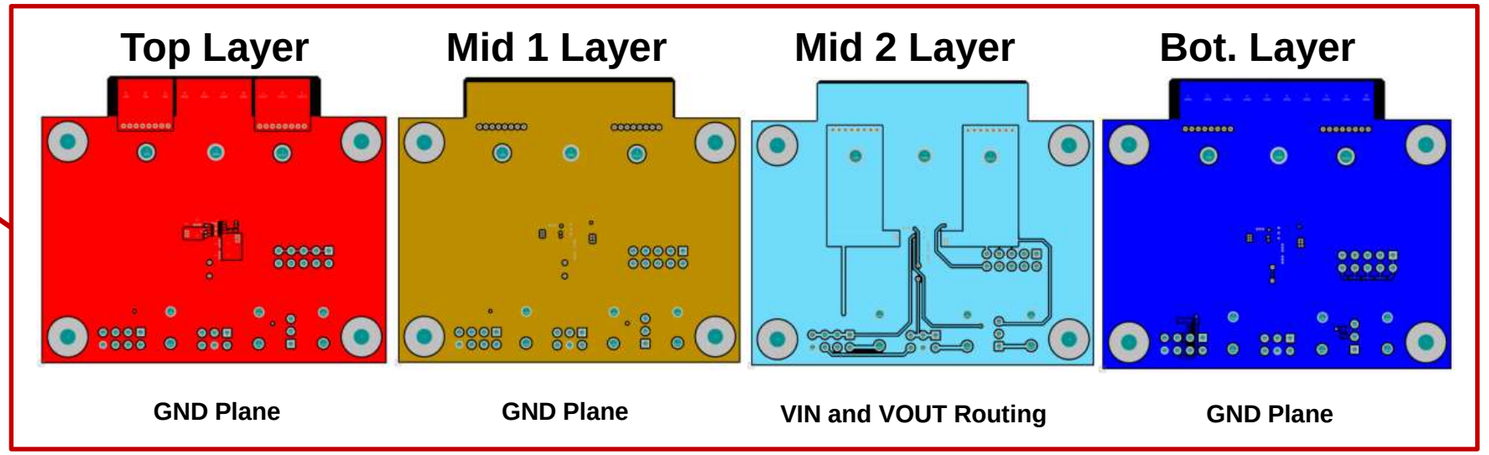
- Same BOM!
- Different stackup
  - Shielding the input (noisy) and output lines
  - Fail by ~5dB vs Pass by ~2dB

HF noise reduction – board layout tricks

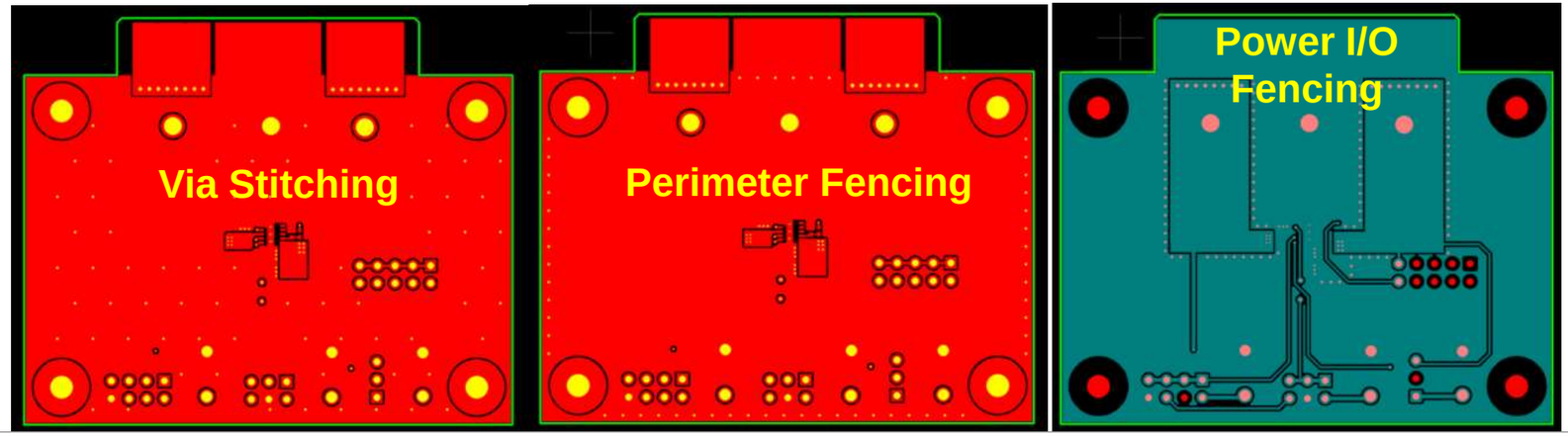
Shielding

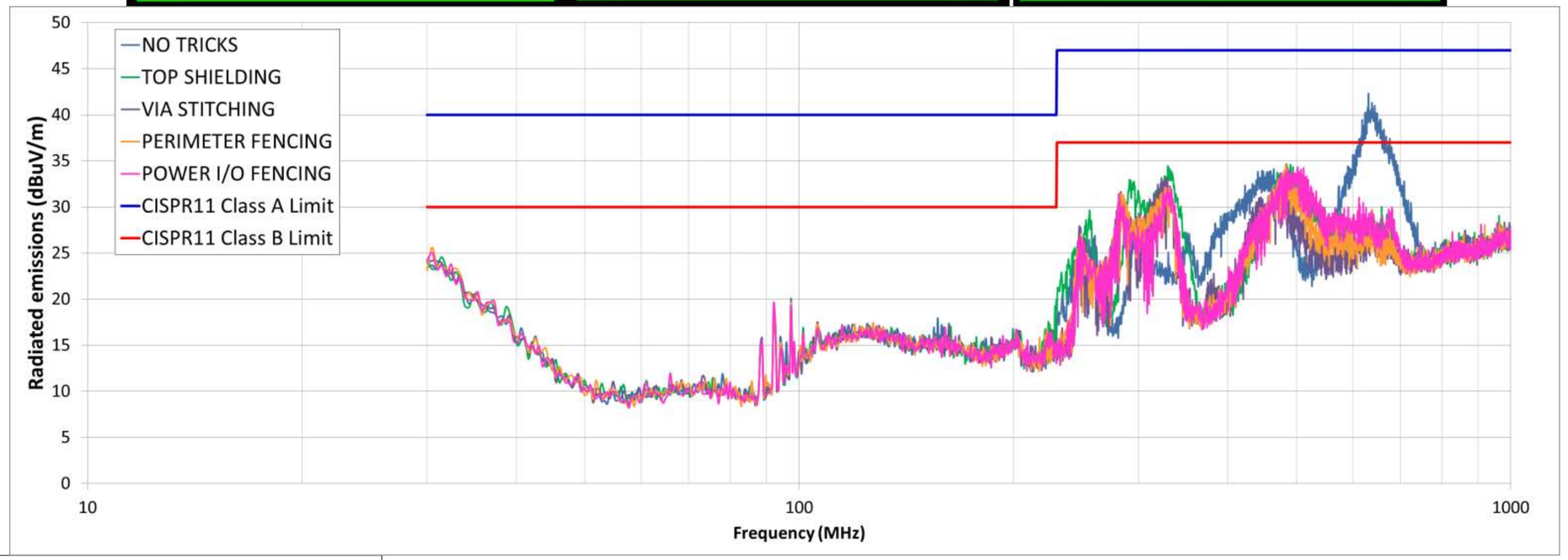




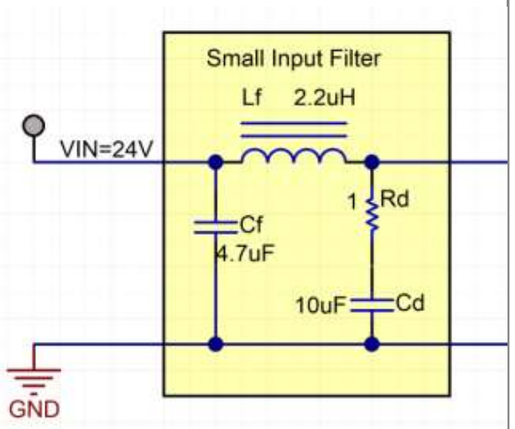


HF noise reduction – board layout tricks

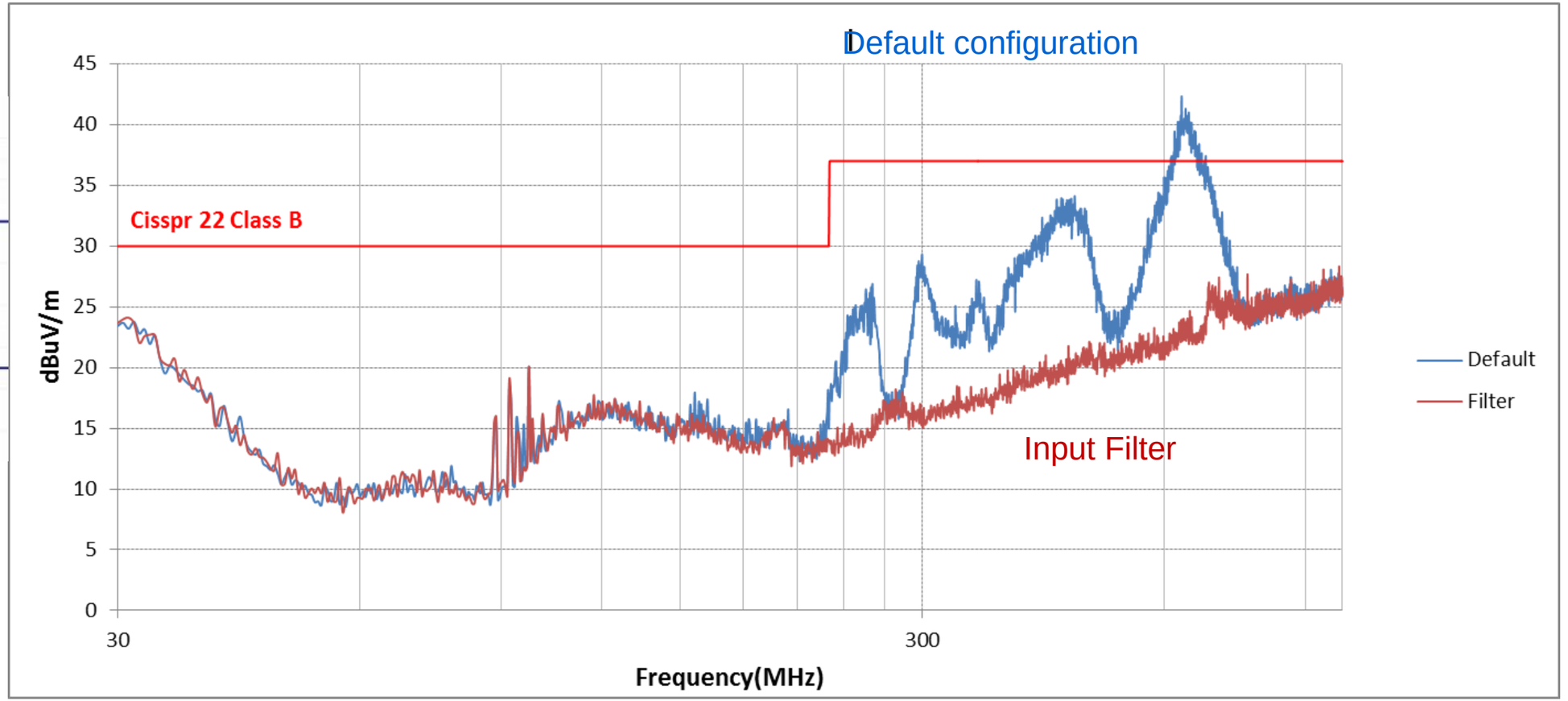




Conducted EMI filter and radiated EMI performance

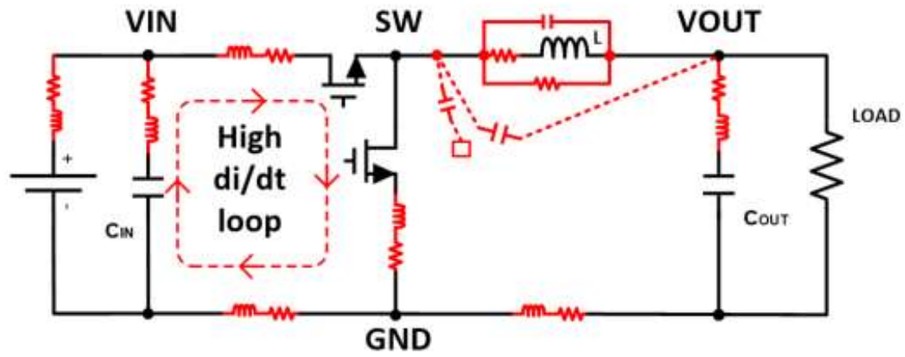


Calculator



HF noise reduction – package level parasitics

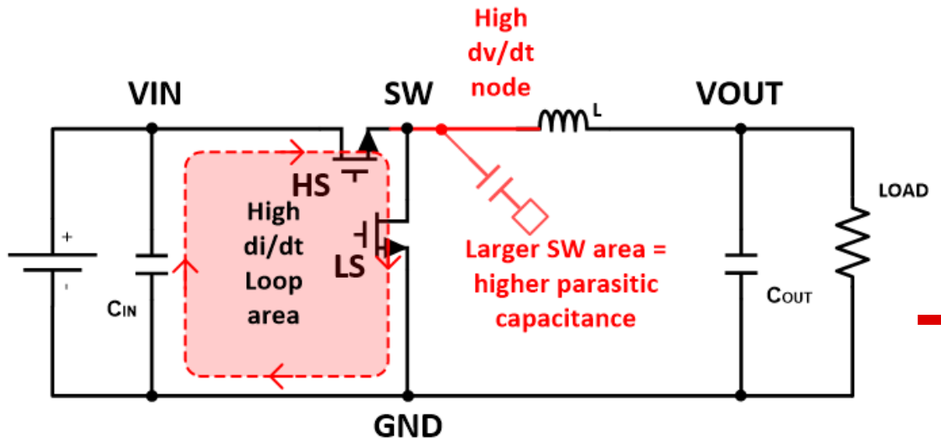
- Some packaging options are better for reducing inductance in the high di/dt loop.
- Power module packages can integrate a high frequency bypass capacitor.
- IC Pinout and Construction Matters

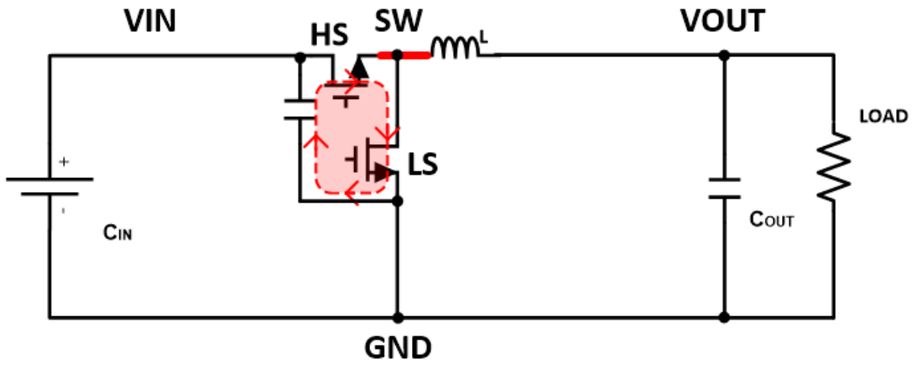


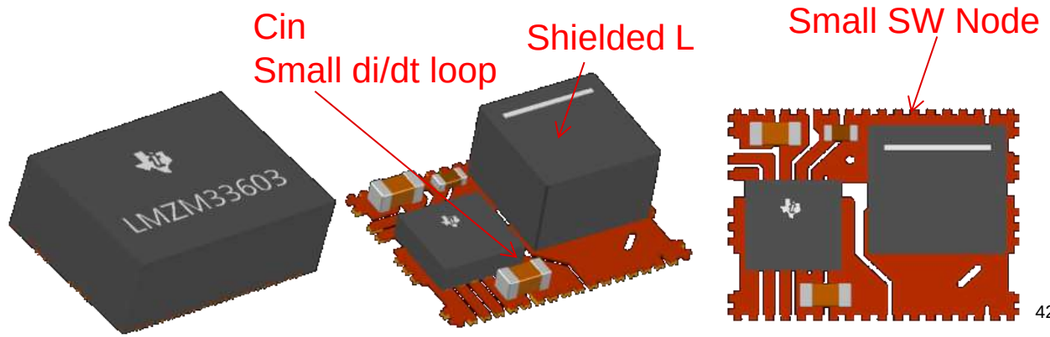
HF noise reduction – DC-DC power modules save you layout troubles

- Reducing the high di/dt loop area – integrated input capacitance.
- Reducing the high dv/dt node area – integrated L and smaller switch node.

Discrete solution without optimized layout → DC-DC Power Module

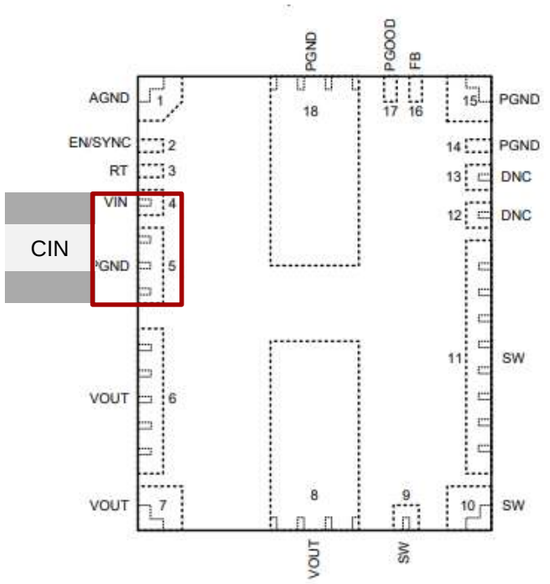




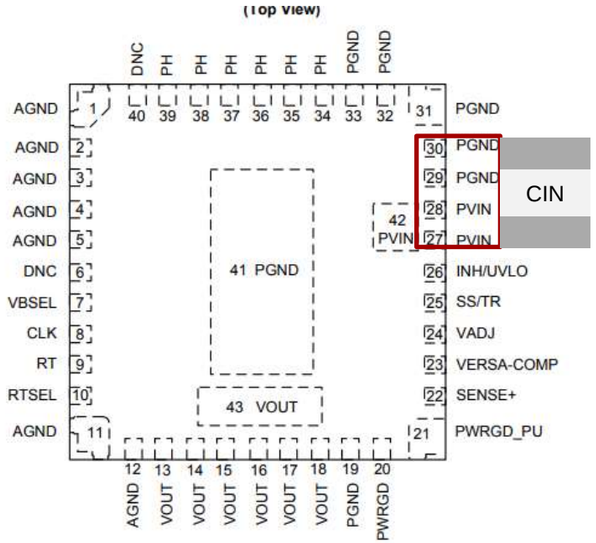


HF noise reduction – proper pinout

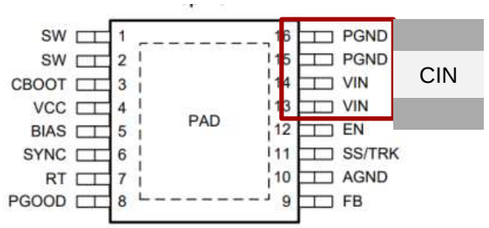
- To minimize the di/dt loop, it is best if the Buck regulator has VIN and PGND pins next to each other. This allow for placing the input capacitor as close as possible to the IC.



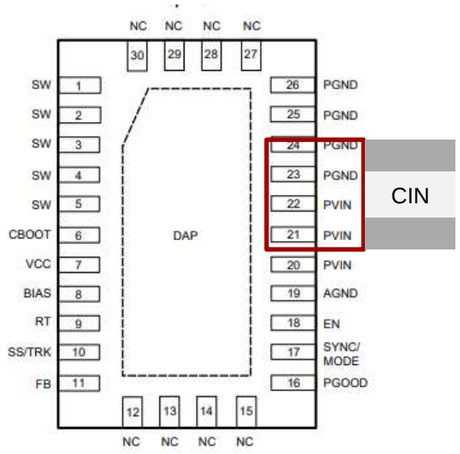
LMZM33603



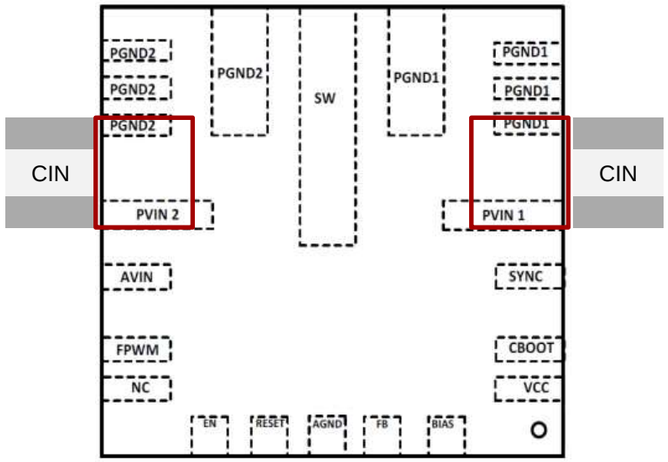
LMZ36002



LM46002

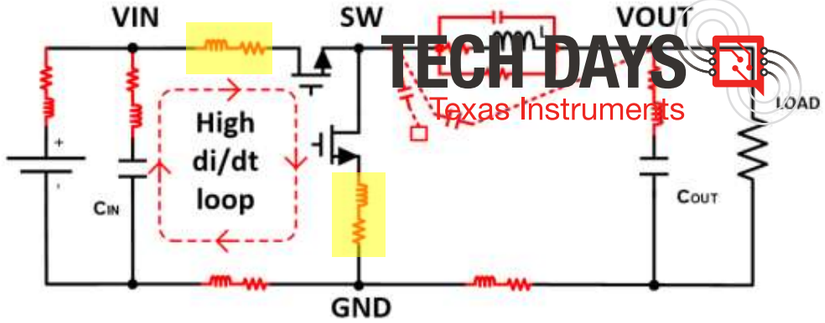


LM73606



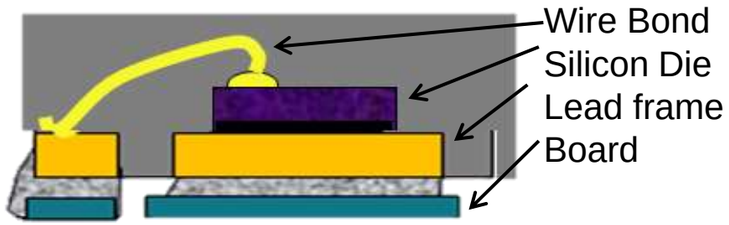
LMS3635

IC package construction can help

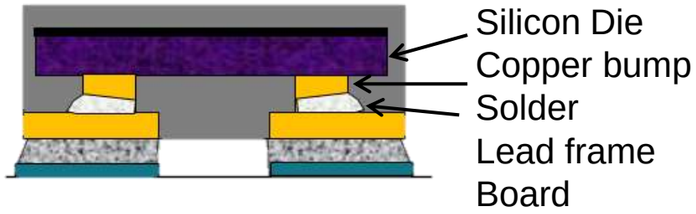


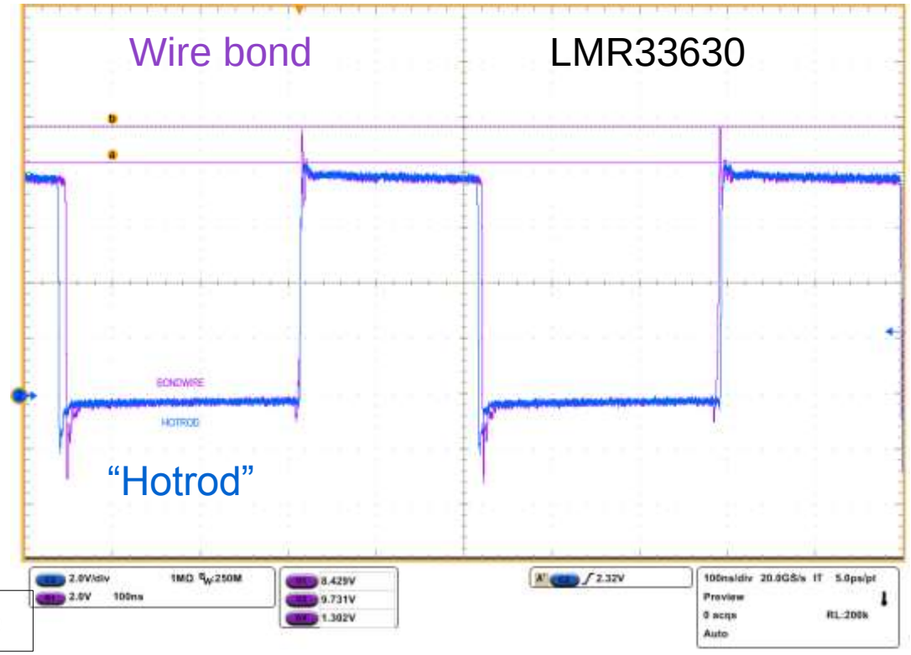
- Bond wire vs Copper pillar interconnects

Standard wire bond QFN package



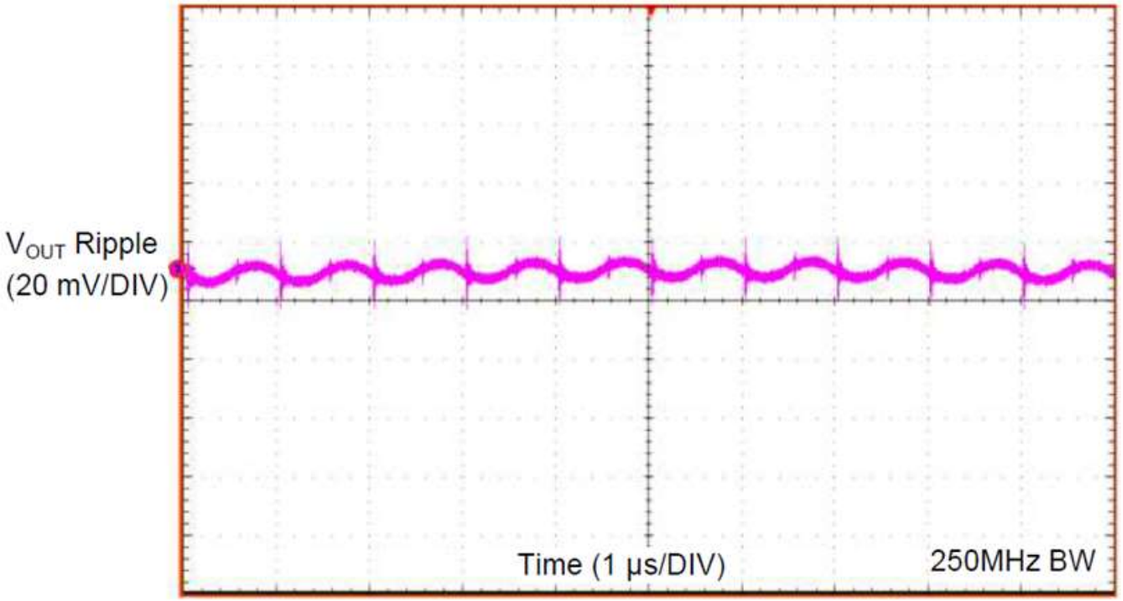
‘Hotrod’ flip chip on lead frame QFN



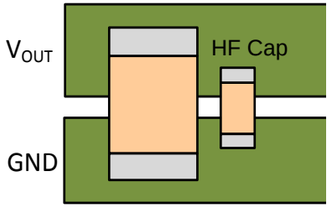


HF filtering

- After careful input capacitor placement and layout there will be some left over high frequency noise – we cannot completely eliminate parasitic L and C.

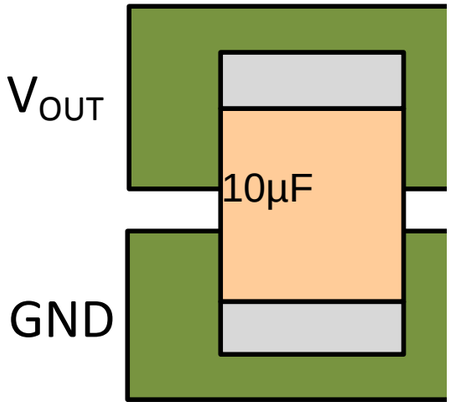


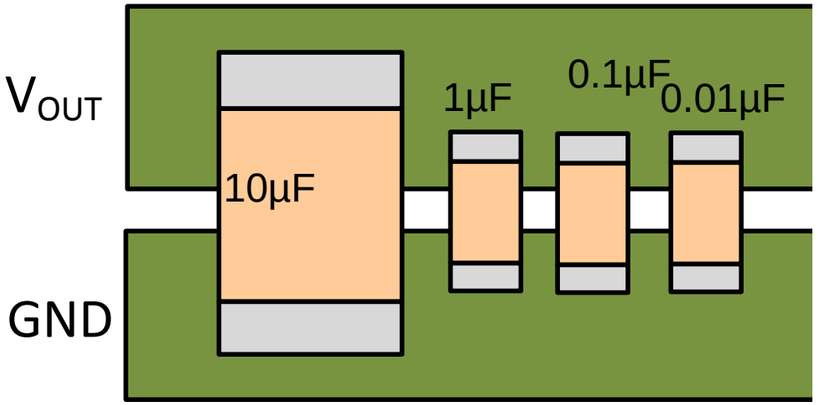
- How can we reduce it?

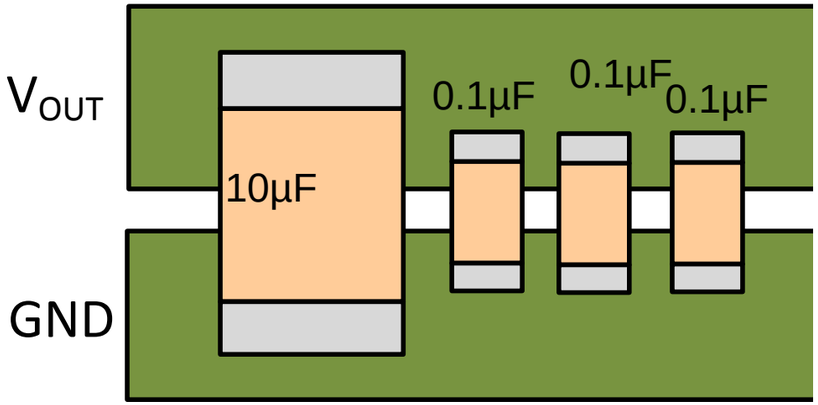


HF filtering

- Which one is better?



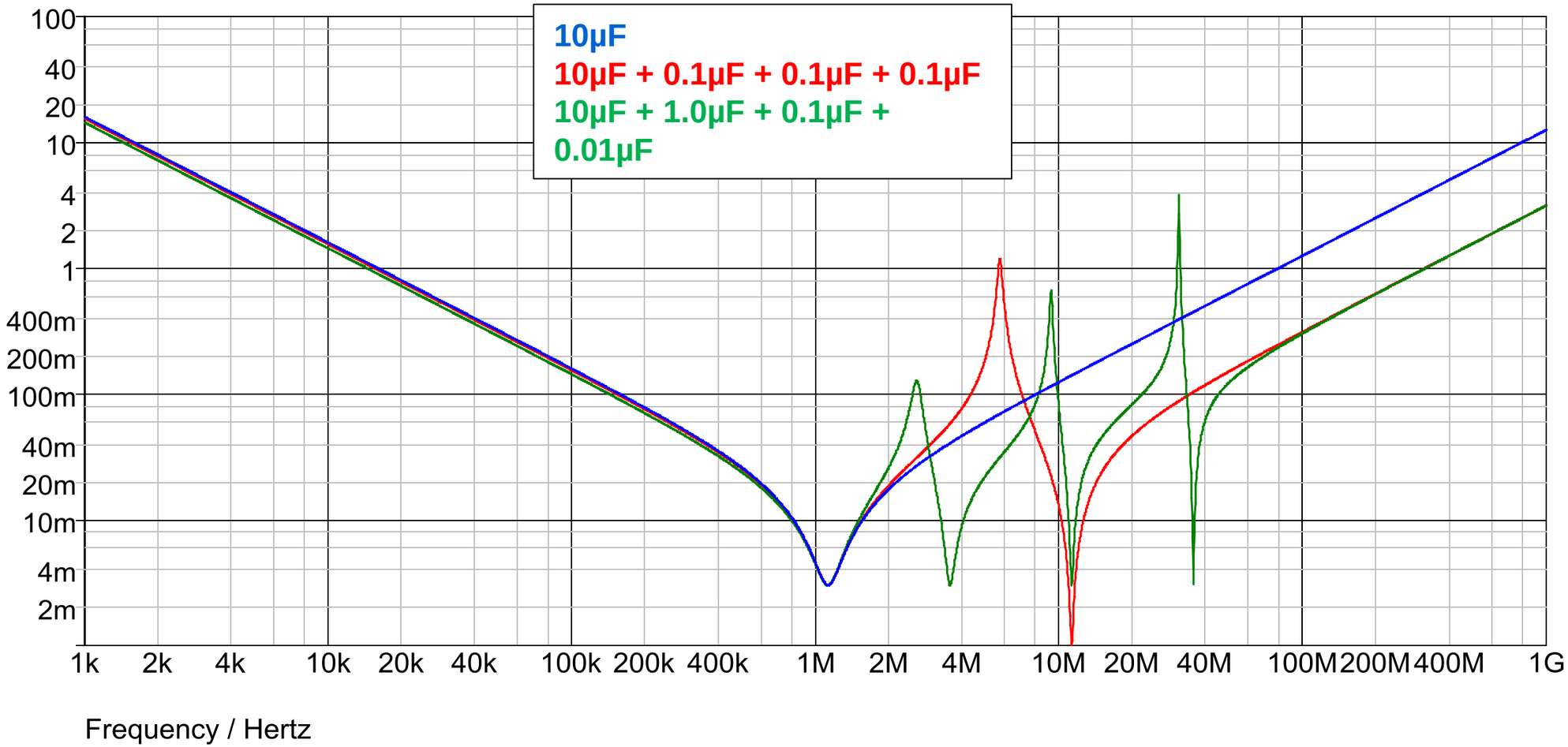




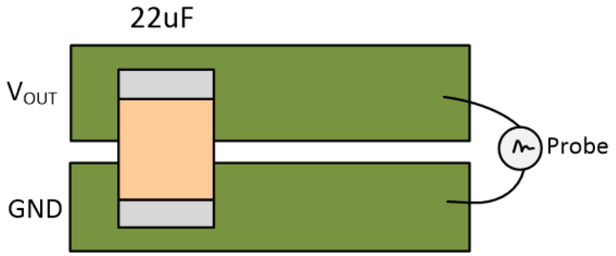
HF filtering

SIMetrix schematic example:

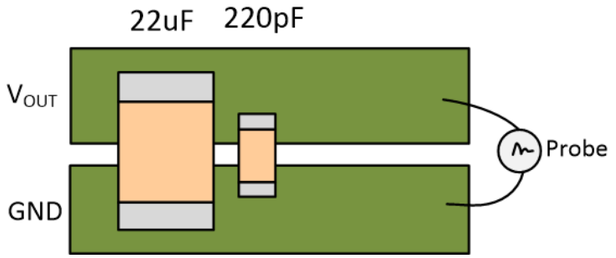
parallel_capacitor_impedance.sxsch



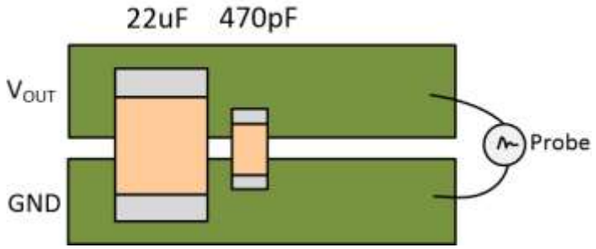
HF filtering with wrong capacitor (example)



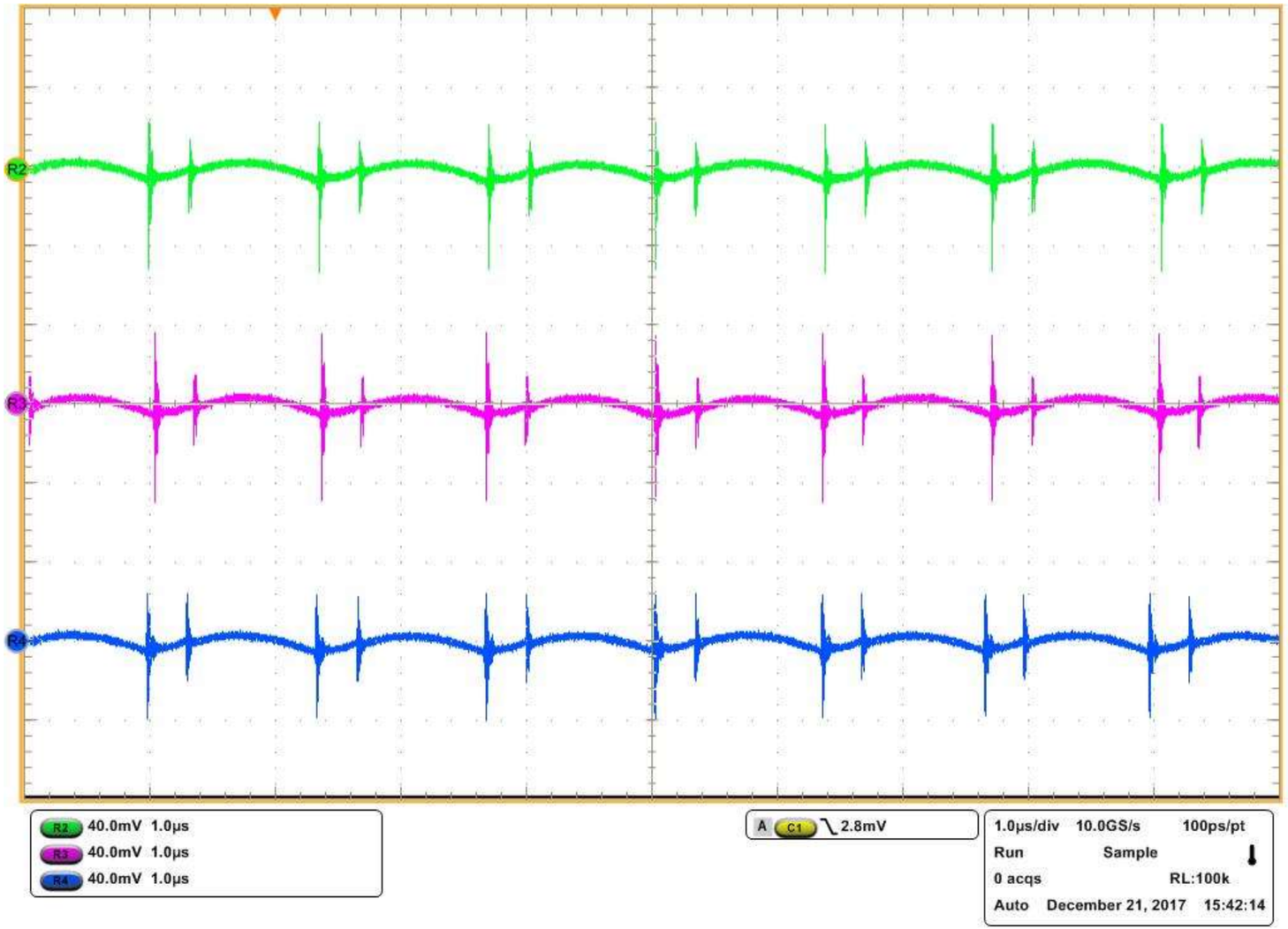
76.2mV



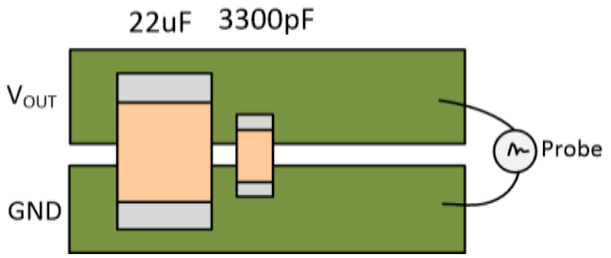
85.7mV



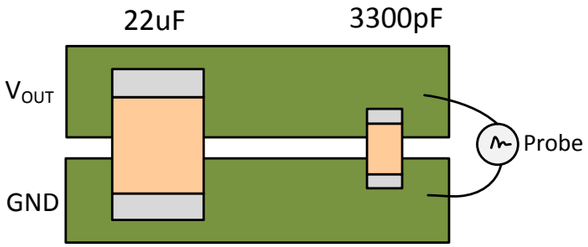
64.4mV



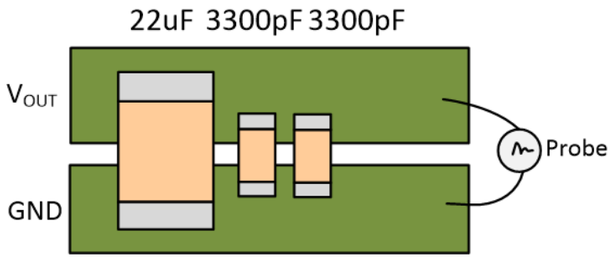
HF filtering - utilizing PCB parasitic inductance



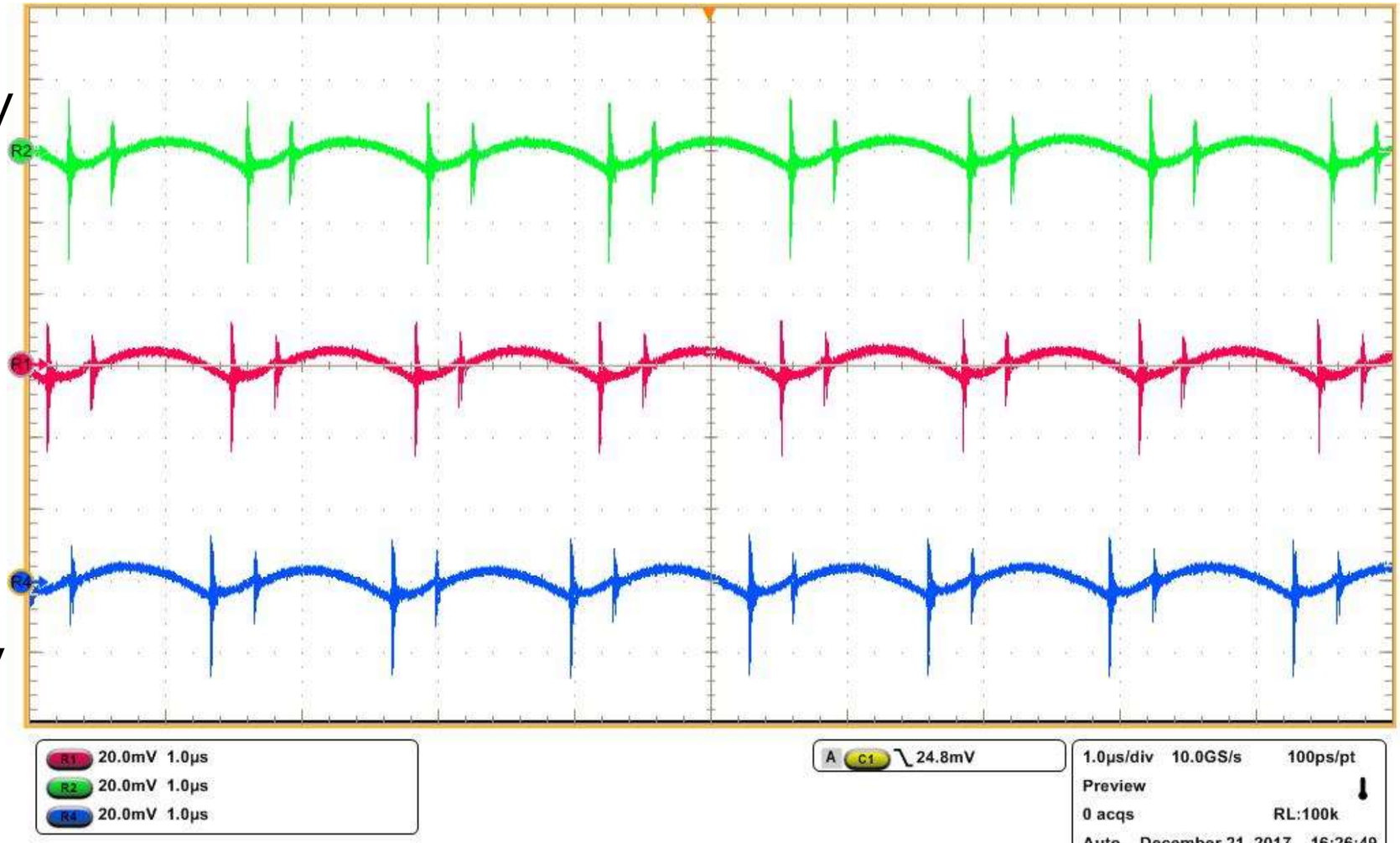
48.4mV



37.9mV



40.3mV

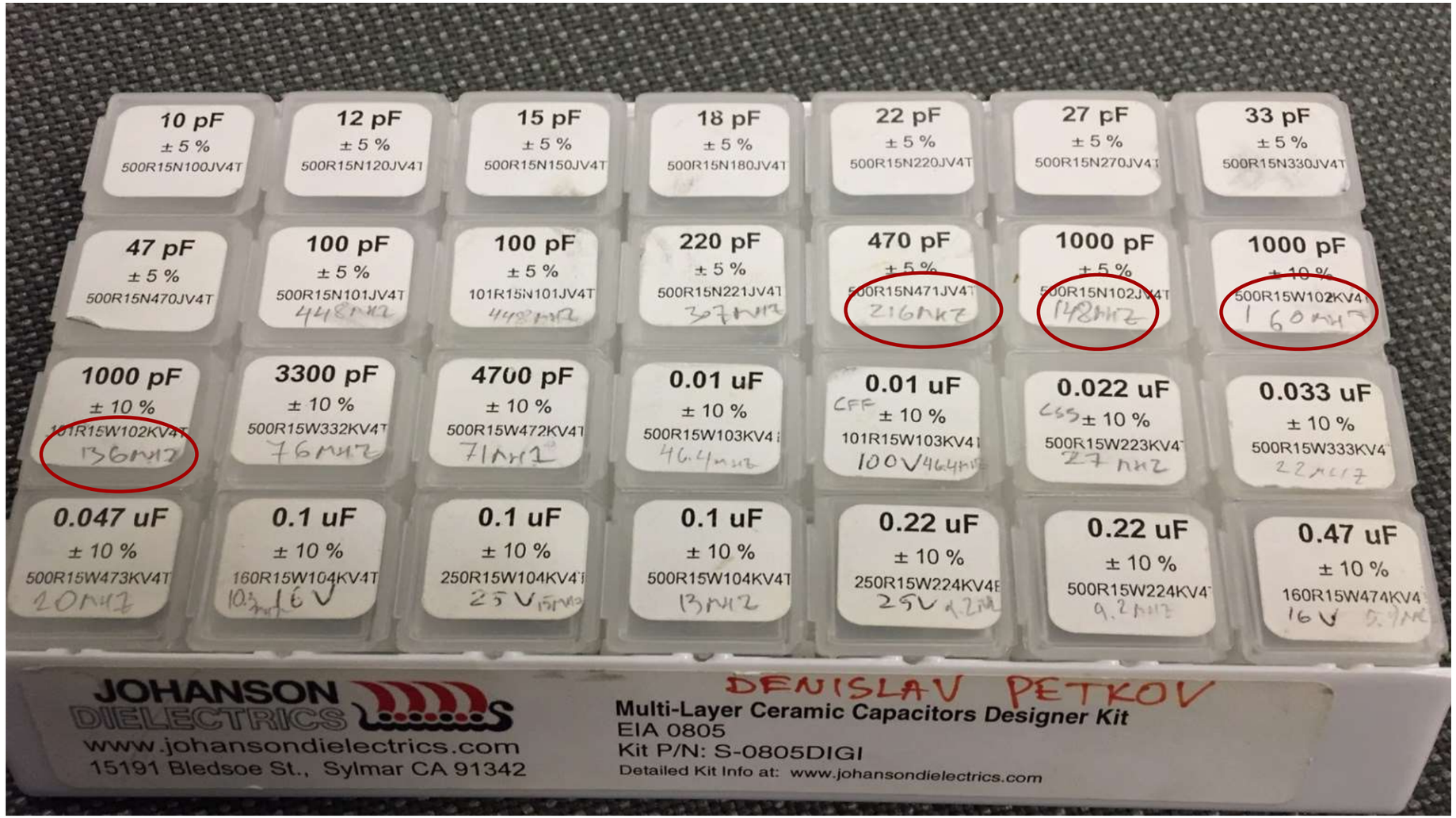


HF filtering – strategy

- Leave footprint in the layout for 2-3 HF filter capacitors.
- Measure the ringing frequency and pick a capacitor with an impedance notch close to, but lower than that frequency.
- Use multiple capacitors of the same value in parallel to avoid new peaks in the impedance curve.

HF filtering – pick the correct capacitor

- Measure your caps
- Mark up your capacitor kit!
- This data may also be available from the capacitor vendor.



Summary

- Understanding the Noise Sources
- Measuring Noise
- Reducing Noise (high frequency and low frequency)

Resources

- **Application Notes and Blogs on EMI and Noise Reduction**
  - Simple Success With Conducted EMI From DCDC Converters
  - Simplify low EMI design with power modules
  - Wiki on Understanding, measuring, and reducing output voltage ripple
  - Design a second-stage filter for noise sensitive applications
  - PCB layout techniques for low noise power designs (in progress)