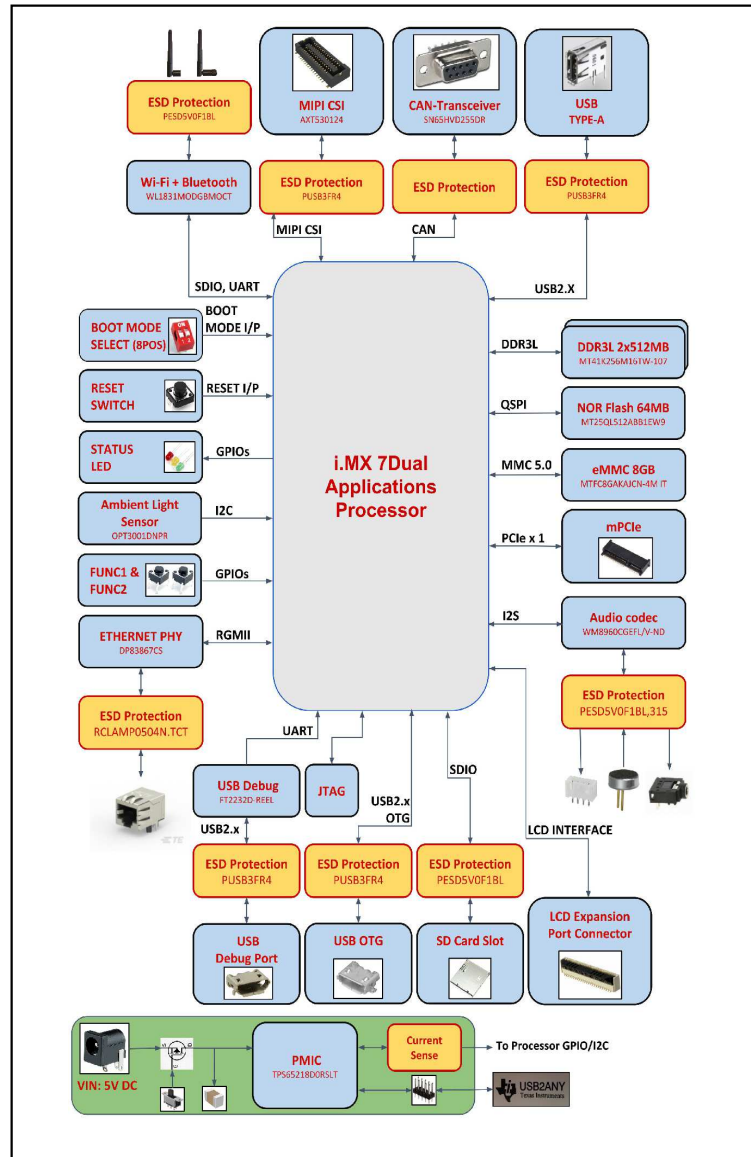


TIXU_MX7D

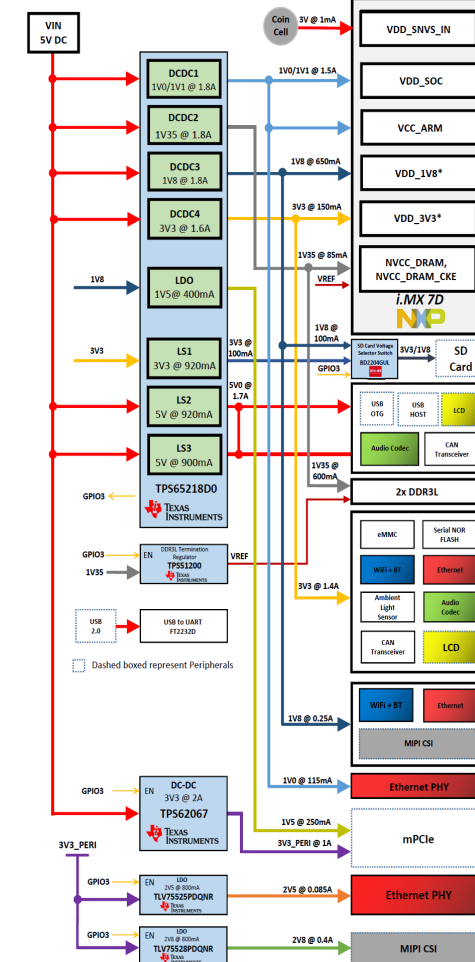
Content	
Page No	Sheet Name
01	COVER PAGE
02	BLOCK DIAGRAM
03	MAIN POWER
04	PMIC
05	POWER DC-DC
06	CPU POWER
07	CPU SIGNAL 1
08	CPU SIGNAL 2
09	DDR3L
10	eMMC/FLASH/SD
11	mini PCIe
12	WiFi BT
13	DEBUG UART/JTAG
14	AUDIO
15	BOOT/UART HEADER
16	CAN/LCD/ALS
17	I2C
18	USB/BUTTON
19	ETHERNET
20	CSI/WATCHDOG/IO
21	MISCELLANEOUS

Rev	Revision Notes	Designer	Approver	Date
A1	First Release	VVDN	TI	17-06-2019
A2	1. R538 Replaced with 300E Resistor 2. C535 Replaced with 4.7uF, 10V Capacitor 3. U37 replaced with TPS3808G2SDBVR 4. D34 Made NO MOUNT 5. R660 Made NO MOUNT, R684 Mounted with 0E	VVDN	TI	05-09-2019
B1	1. SD card VCC voltage changed to VCC_3V3 2. Pin connection changed in USB2ANY header H1 3. Added Capacitor C578, C579 across SW5 and SW6 4. PGOOD LED of PMIC connected from PGOOD pin of TP865218D0 5. PMIC_STANDBY from uP used for resetting DCDC1, DCDC2 of TP865218D0 6. PMIC_GPIOD1 used for enabling DCDC converters other than TP865218D0	VVDN	TI	24-10-2019

BLOCK DIAGRAM



POWER ARCHITECTURE



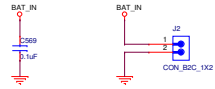
VDD_1V8* --> VDDA_1P8, VDD_LPSR_IN, VDD_TEMPSENSOR, NVCC_SD2, NVCC_SD3, NVCC_SPI, VDDA_ADC1_1P8, VDDA_ADC2_1P8, FUSE_FSOURCE, VDD_XTAL_1P8

VDD_3V3* --> NVCC_ENET1, NVCC_EPDC1, NVCC_EPDC2, NVCC_I2C, NVCC_LCD, NVCC_SAI, NVCC_UART, NVCC_GPIO1, NVCC_GPIO2, VDD_OTG1_3P3_IN, VDD_USB_OTG2_3P3_IN

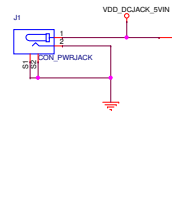
NVCC_SD1 of i.MX7D is powered from the output of SD Voltage Selector Switch

	Title : BLOCK DIAGRAM	
	Fab No : 501-1-00947	Rev : B1_01
	Asy No : 701-1-01125	Sheet 2 of 21

BATTERY IN

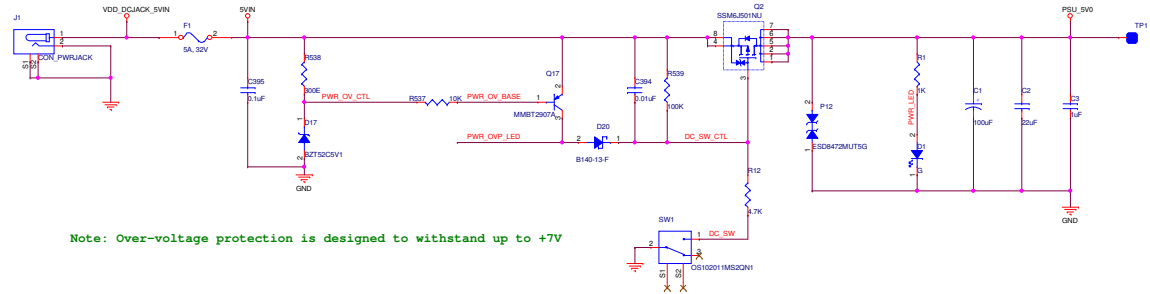


5V DC POWER

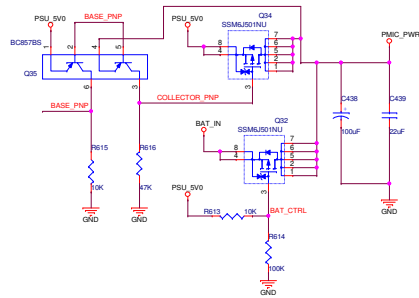


Note: Over-voltage protection is designed to withstand up to +7V

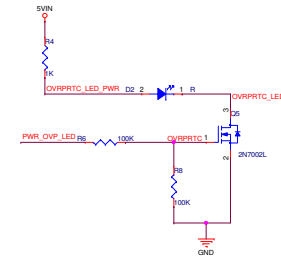
OVER VOLTAGE PROTECTION

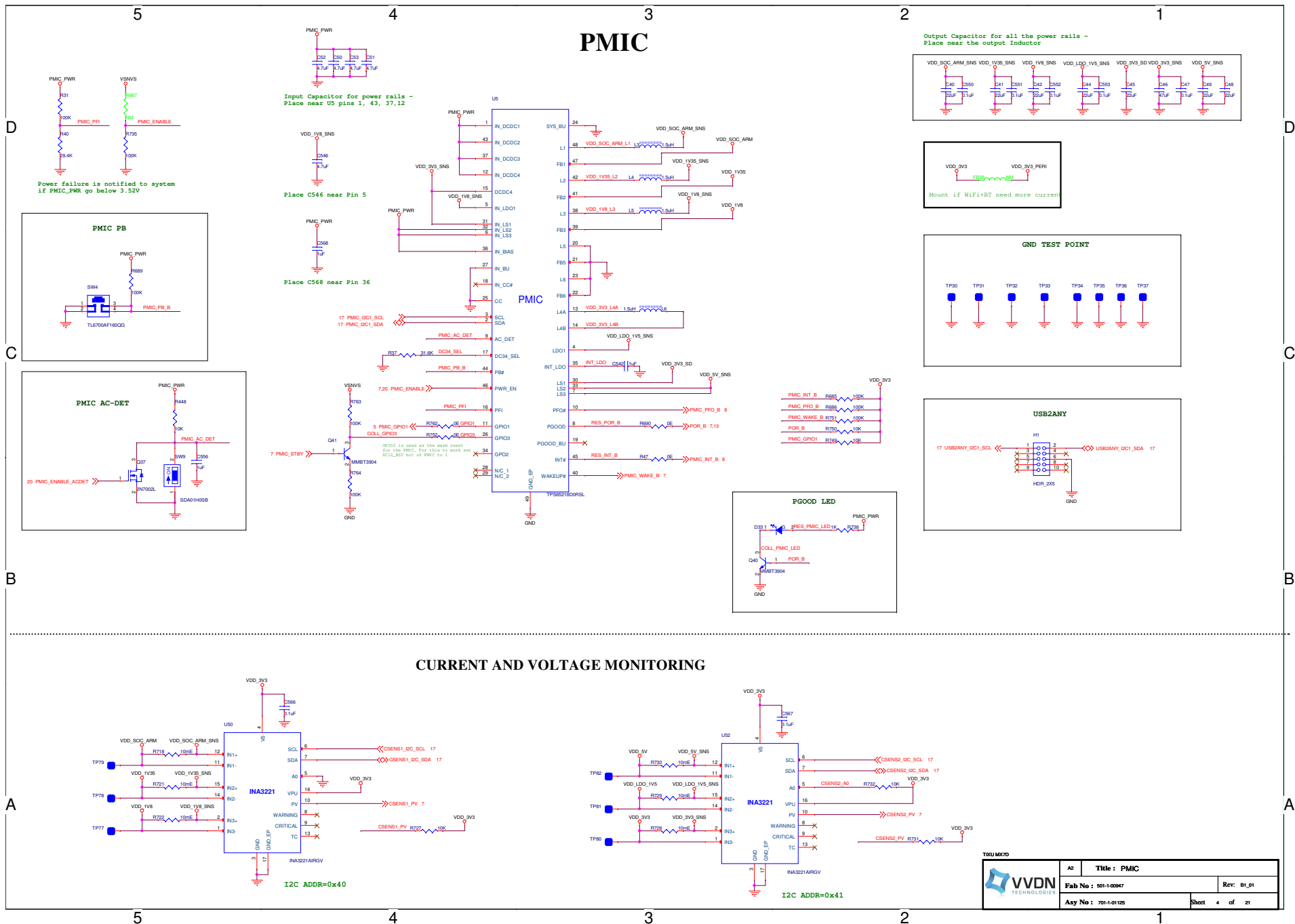


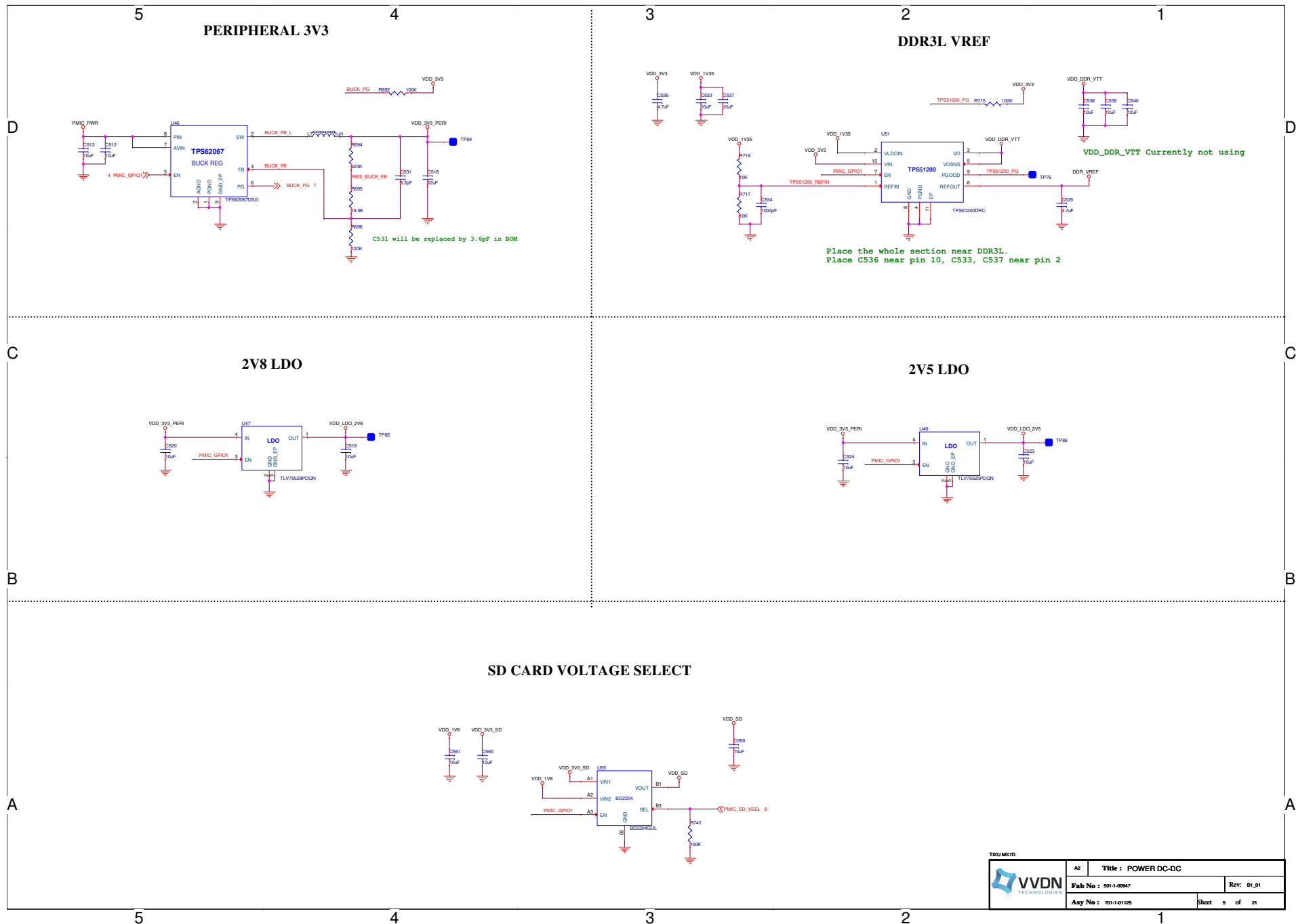
ORING



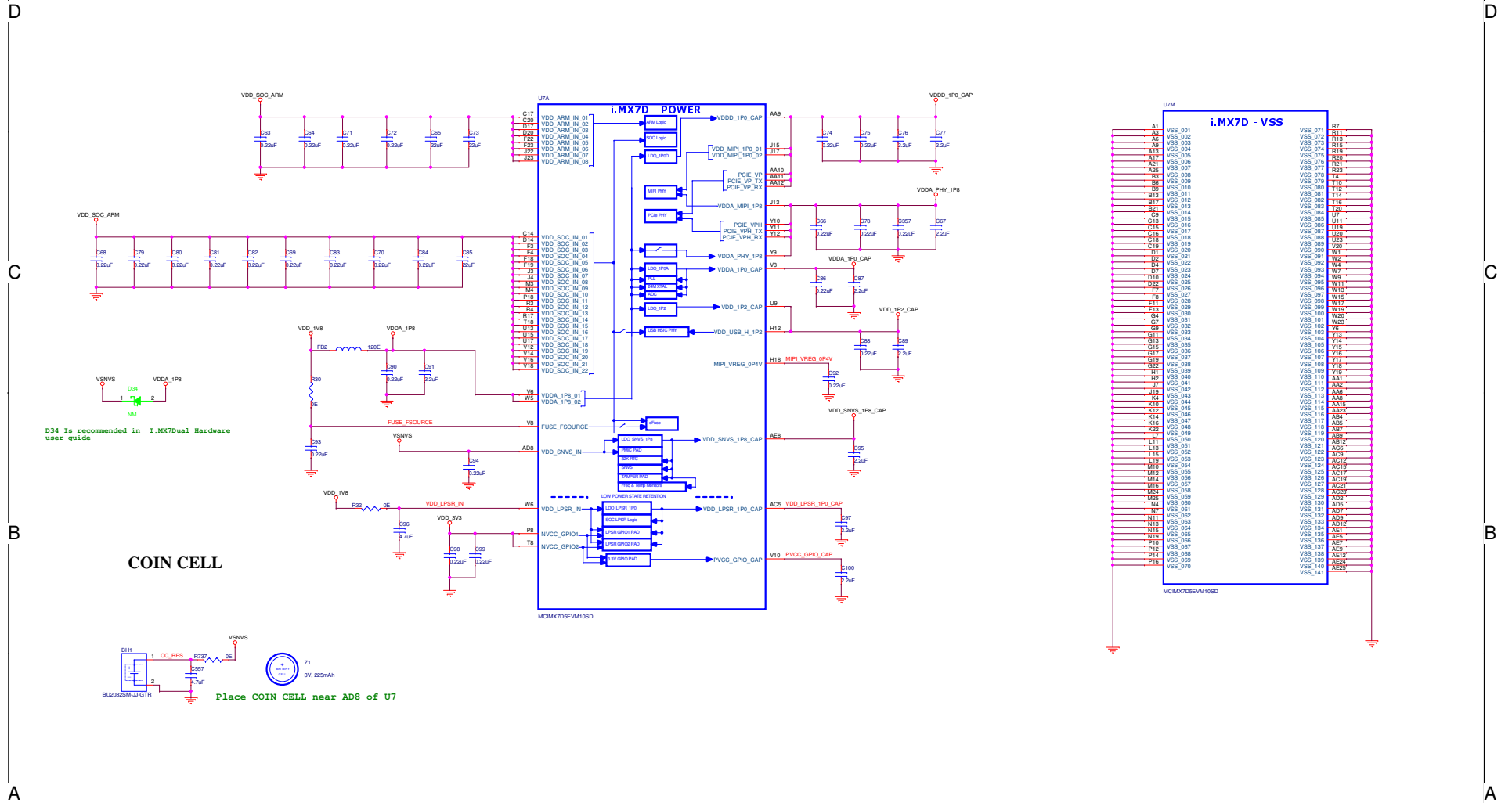
OVER VOLTAGE INDICATOR





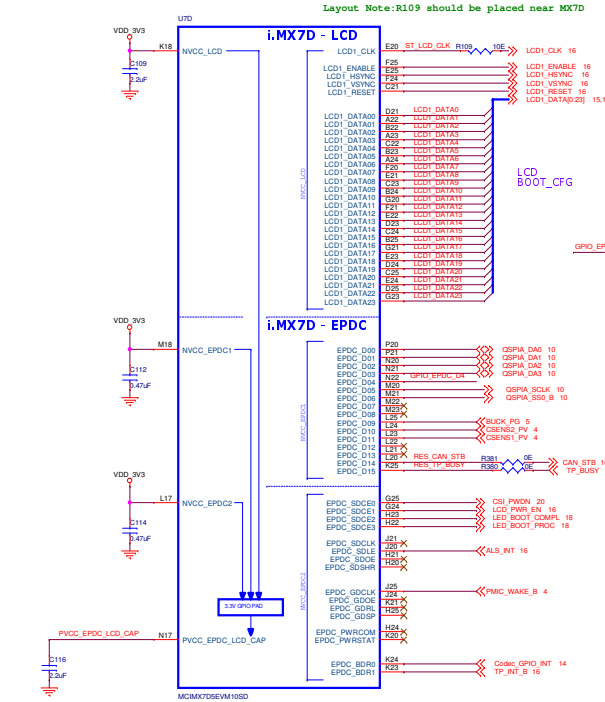
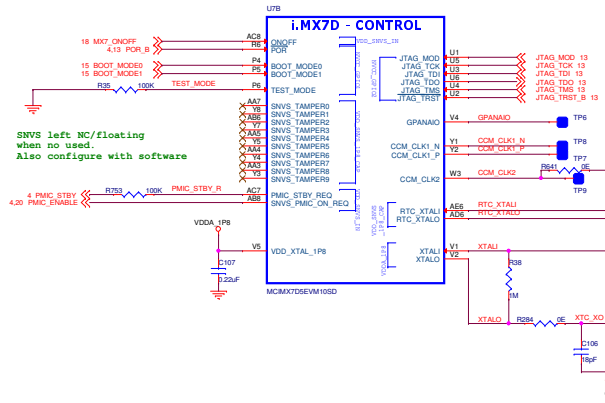


CPU POWER

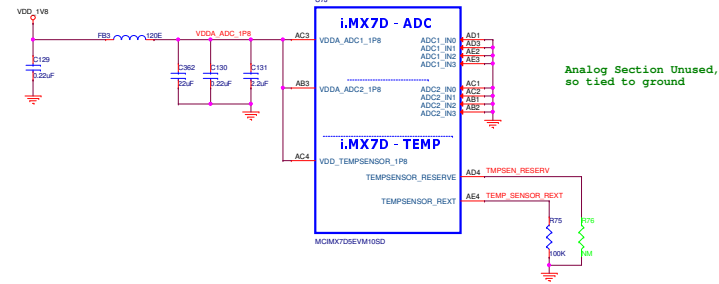
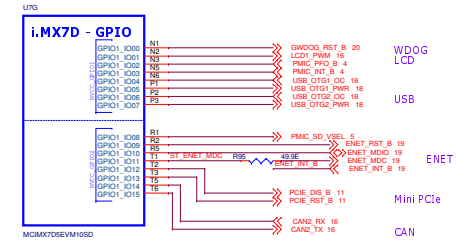
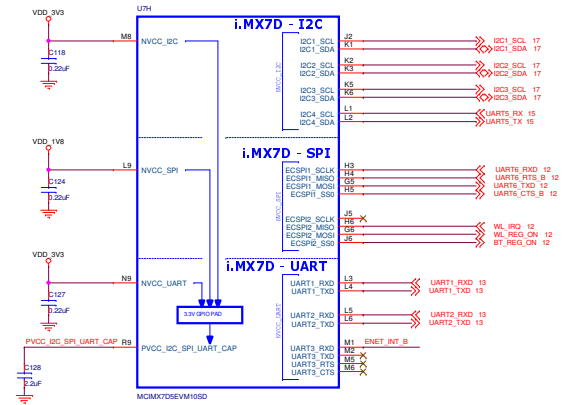
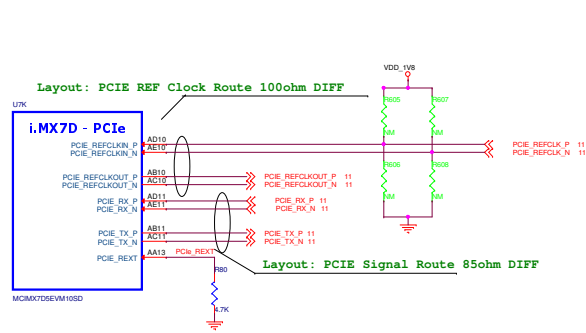
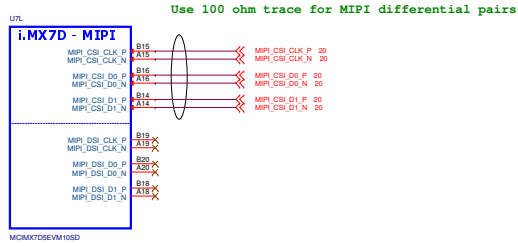
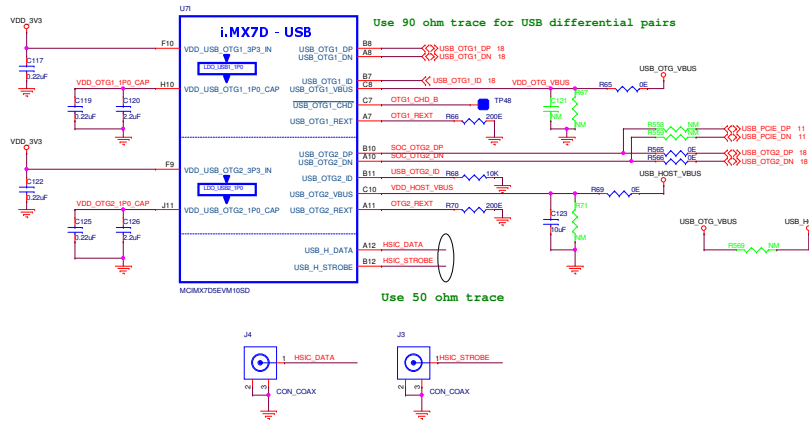


Title : CPU POWER	
Fab No : 501-00947	Rev: 01_01
Asy No : 701-01125	Sheet 6 of 21

CPU SIGNAL 1

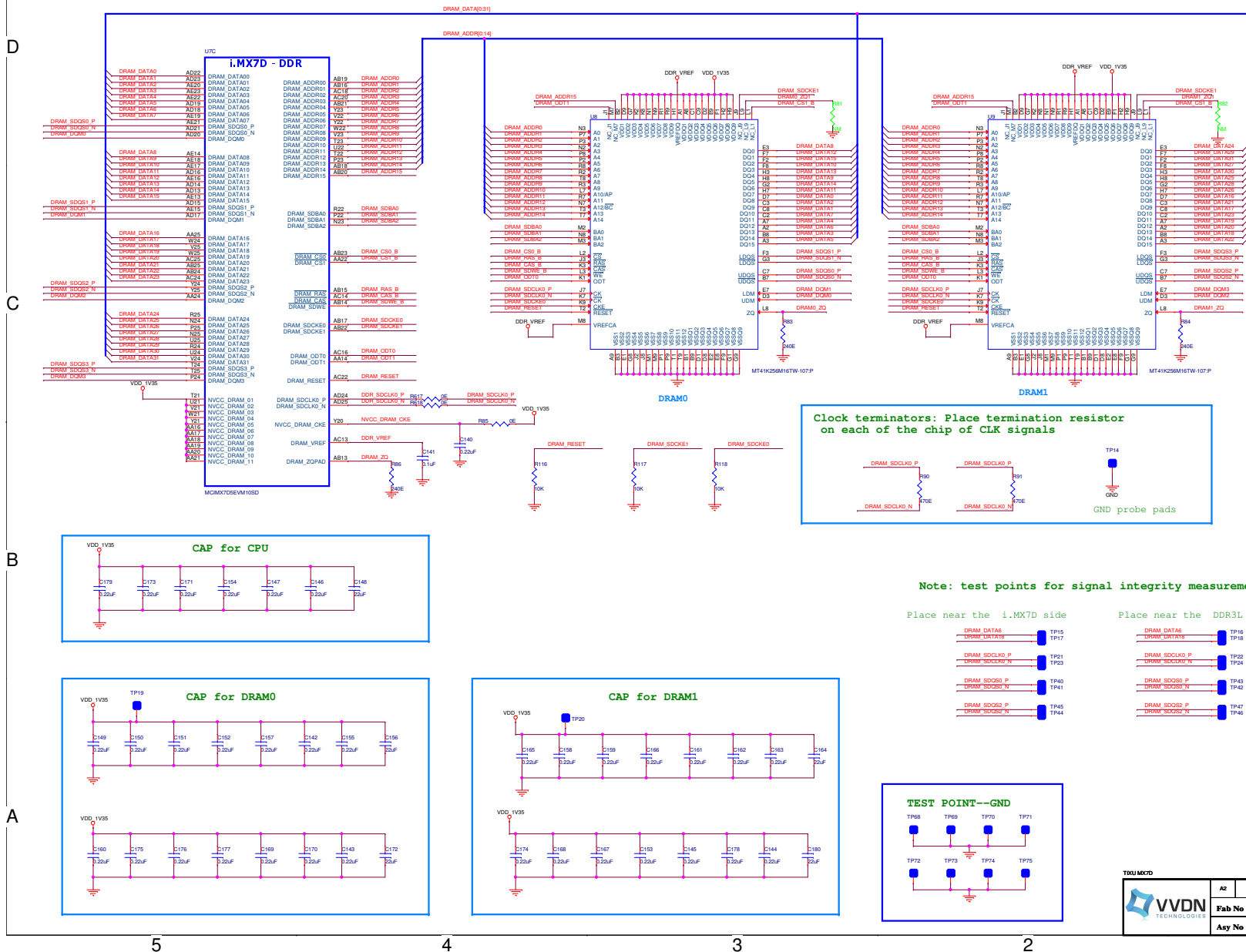


CPU SIGNAL 2

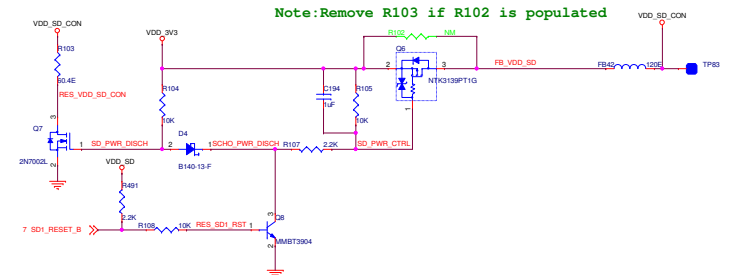
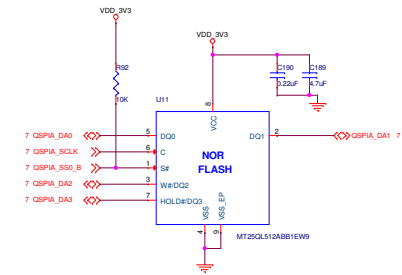


	Title : CPU SIGNAL 2	
	Fab No : 501-00947	Rev : 01_01
	Any No : 701-01125	Sheet 8 of 21

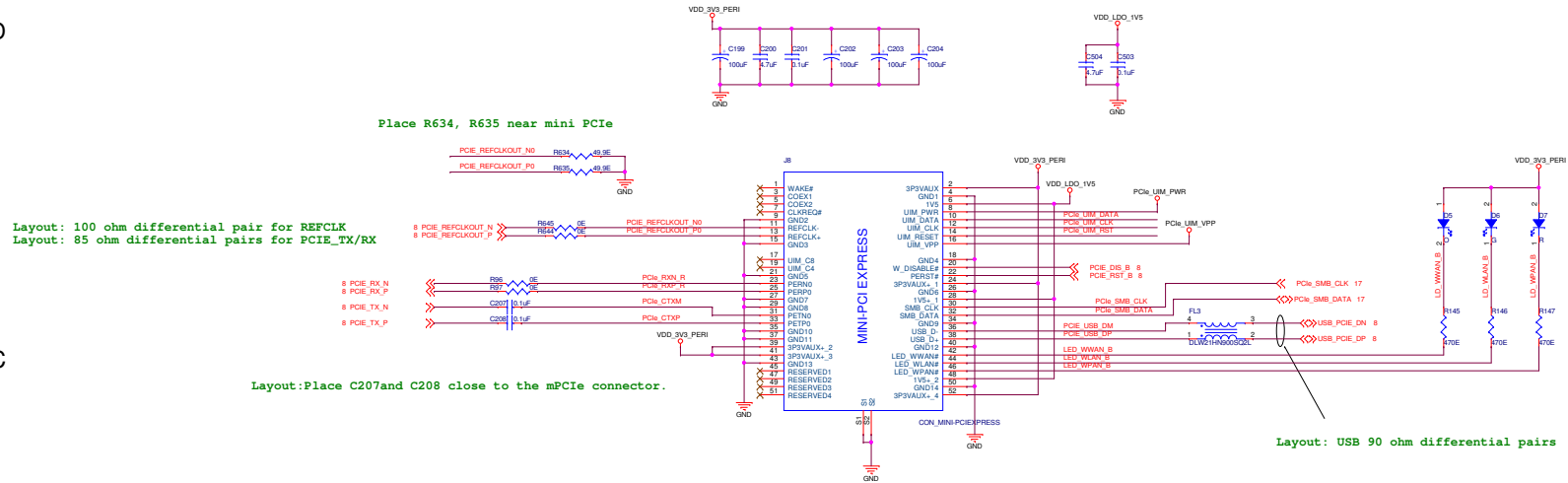
DDR3L



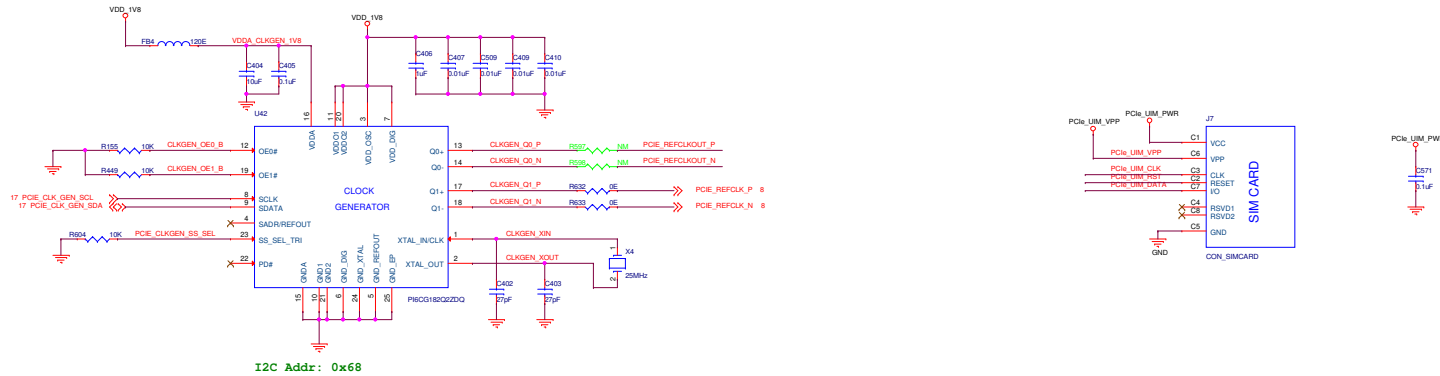
1



Mini-PCIE

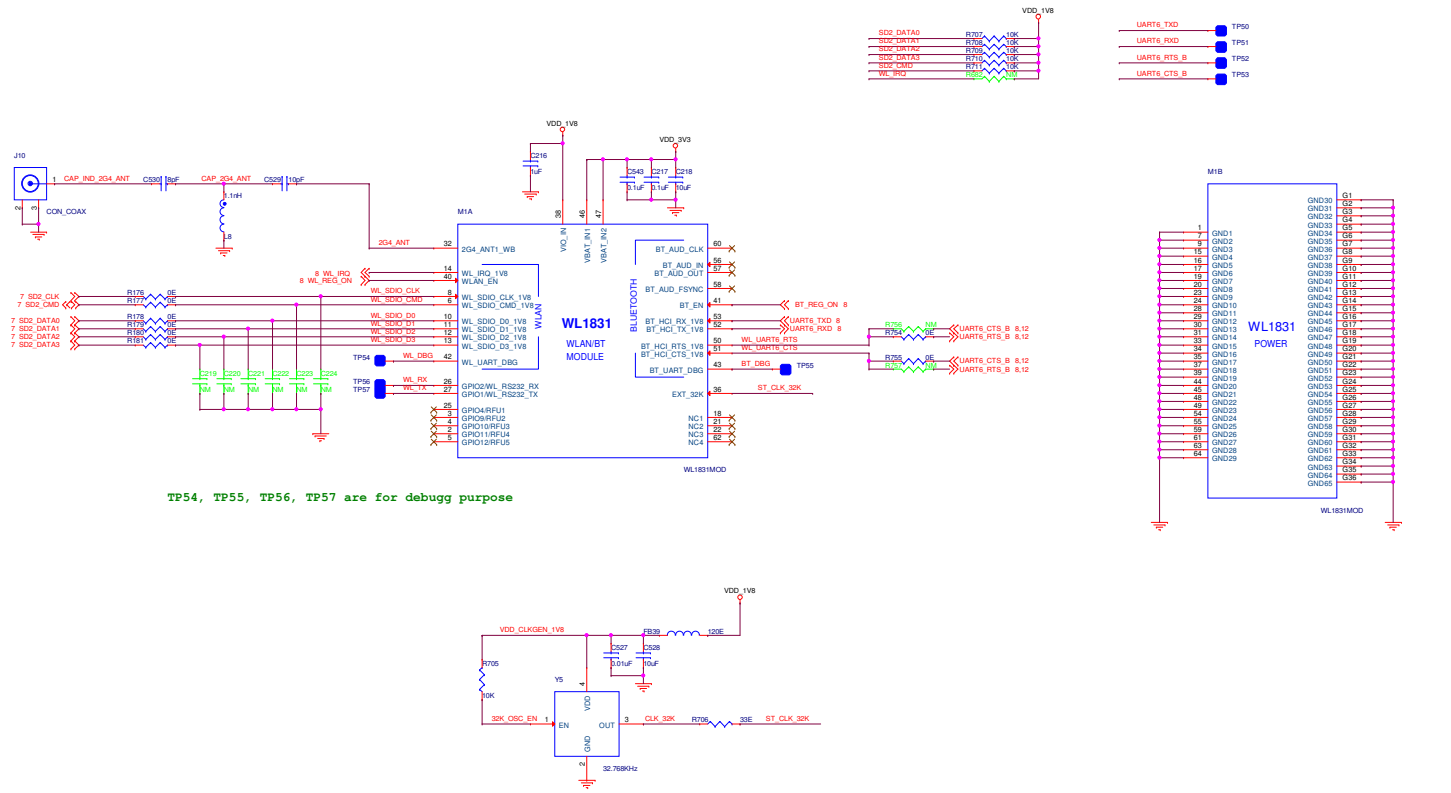


NOTE:
This design assumes a normal loading on the VDD_3V3_PERI rail of up to 1A.
The VDD_LDO_IV5 rail is allowed a maximum of 250 mA.



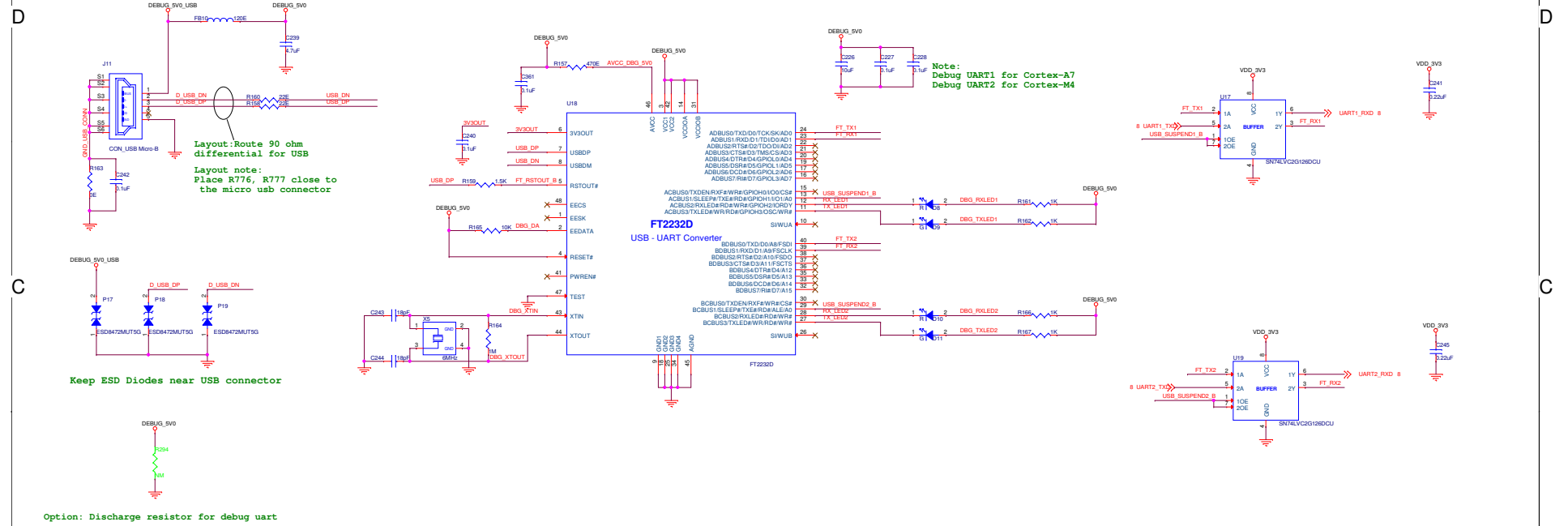
	Title : mini_PCie	
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 11 of 21
	TDX M0C7D	

WiFi/BT

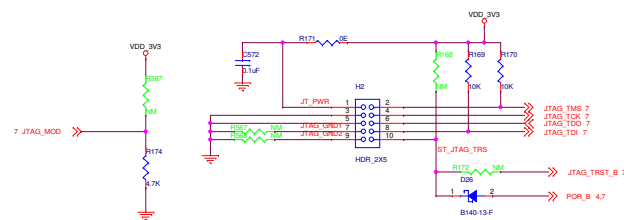


	Title : WiFi/BT		
	Rev: BT_01	Fab No : 501-1-00947	
	Sheet 12 of 21	Asy No : 701-1-01125	

DEBUG UART

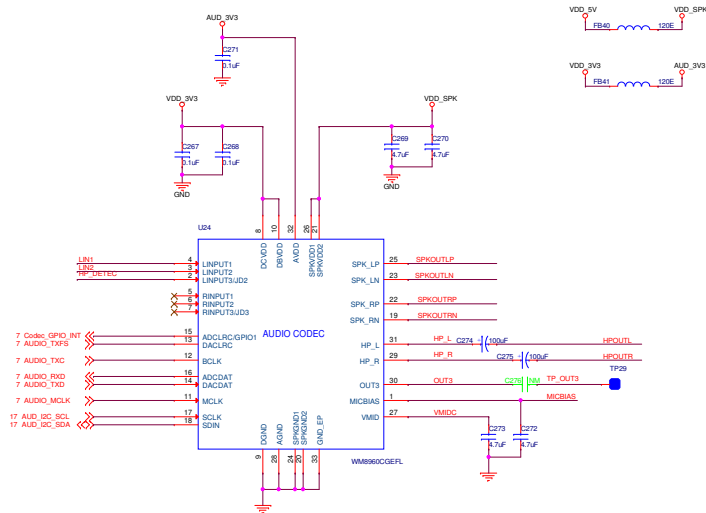


JTAG

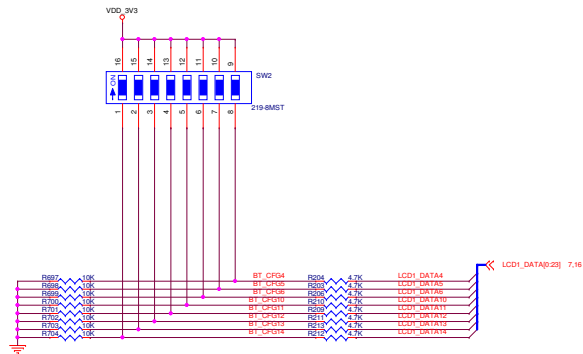


TKU MK7D			
 VVDN TECHNOLOGIES	A2	Title : DEBUG UART/JTAG	
	Fab No : 501-00947		Rev: 01_01
	Asy No : 701-01125		Sheet 13 of 21

AUDIO

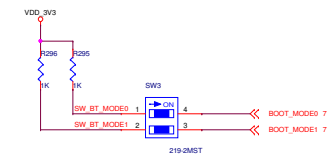


BOOT CONFIG



BOOT MODE

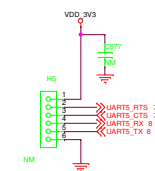
BOOT_MODE[1:0]	Boot type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved



BOOT TABLE - SW2

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3		0	0	Bus Width: 0 - 1-bit 1 - 4-bit
010 = MMC/eMMC Boot					Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)		
100 = QSPI Boot			0	0	0	0	0

UART HEADER



CAN

[illegible]

Ambient Light Sensor

The diagram shows the following components and connections:

- Power Supply:** VDD_3V3 is connected to pin 1 of the sensor. A 100nF capacitor (C2091) is connected between VDD_3V3 and GND.
- Grounding:** Pin 6 (GND) is connected to GND.
- Addressing:** Pin 2 (ADDR) is connected to a pull-up resistor (R663) to VDD_3V3 and a pull-down resistor (R674) to GND.
- I2C Interface:**
 - Pin 4 (SCL) is connected to pin 17 (ALS_SC_SCL).
 - Pin 6 (SDA) is connected to pin 17 (ALS_SC_SDA).
 - Pin 5 (INT) is connected to pin 7 (ALS_INT).
- Sensor:** OPT3001DNP, I2C Addr: 0x44.

Ambient Light Sensor

The diagram shows the following components and connections:

- Power Supply:** VDD_3V3 is connected to pin 1 of the sensor. A 100nF capacitor (C2091) is connected between VDD_3V3 and ground.
- Address Pin (ADDR):** Pin 2 is connected to a pull-up resistor (R663) to VDD_3V3 and to the ADDR_LIGHTSEN signal line.
- I2C Interface:**
 - SCL (pin 4) is connected to the I2C_SCL_17 signal line.
 - SDA (pin 6) is connected to the I2C_SDA_17 signal line.
 - INT (pin 5) is connected to the ALS_INT_7 signal line.
- Grounding:** Pin 3 (GND) is connected to ground. Pin 4 (GND) is also connected to ground.
- Component Values:** R663 is 10K, R658 is 10K, and C2091 is 100nF.
- Text Labels:** "I2C Addr: 0x44" is displayed in green text.

[illegible][illegible][illegible]

3

2

1

ADAFRUIT LCD

7 LCD_PWR_EN

VDD_3V3

2544

4.7uF

R254

Q20

CEQ254B1F4

VDD_3V3_LCD

7 LCD1_ENABLE

7 LCD1_VSYNC

7 LCD1_CLK

7 LCD1_RESET

7 LCD1_PWM

17 LCD1_DC_SCL

17 LCD1_DC_SDA

VDD_5V

C261

22uF

GND

VDD_3V3_LCD

C262

10uF

GND

VDD_3V3_LCD

C263

10uF

GND

VDD_3V3_LCD

C264

10uF

GND

214

LCD1_DATA0

LCD1_DATA1

LCD1_DATA2

LCD1_DATA3

LCD1_DATA4

LCD1_DATA5

LCD1_DATA6

LCD1_DATA7

LCD1_DATA8

LCD1_DATA9

LCD1_DATA10

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LCD1_DATA301

LCD1_DATA302

LCD1_DATA303

LCD1_DATA304

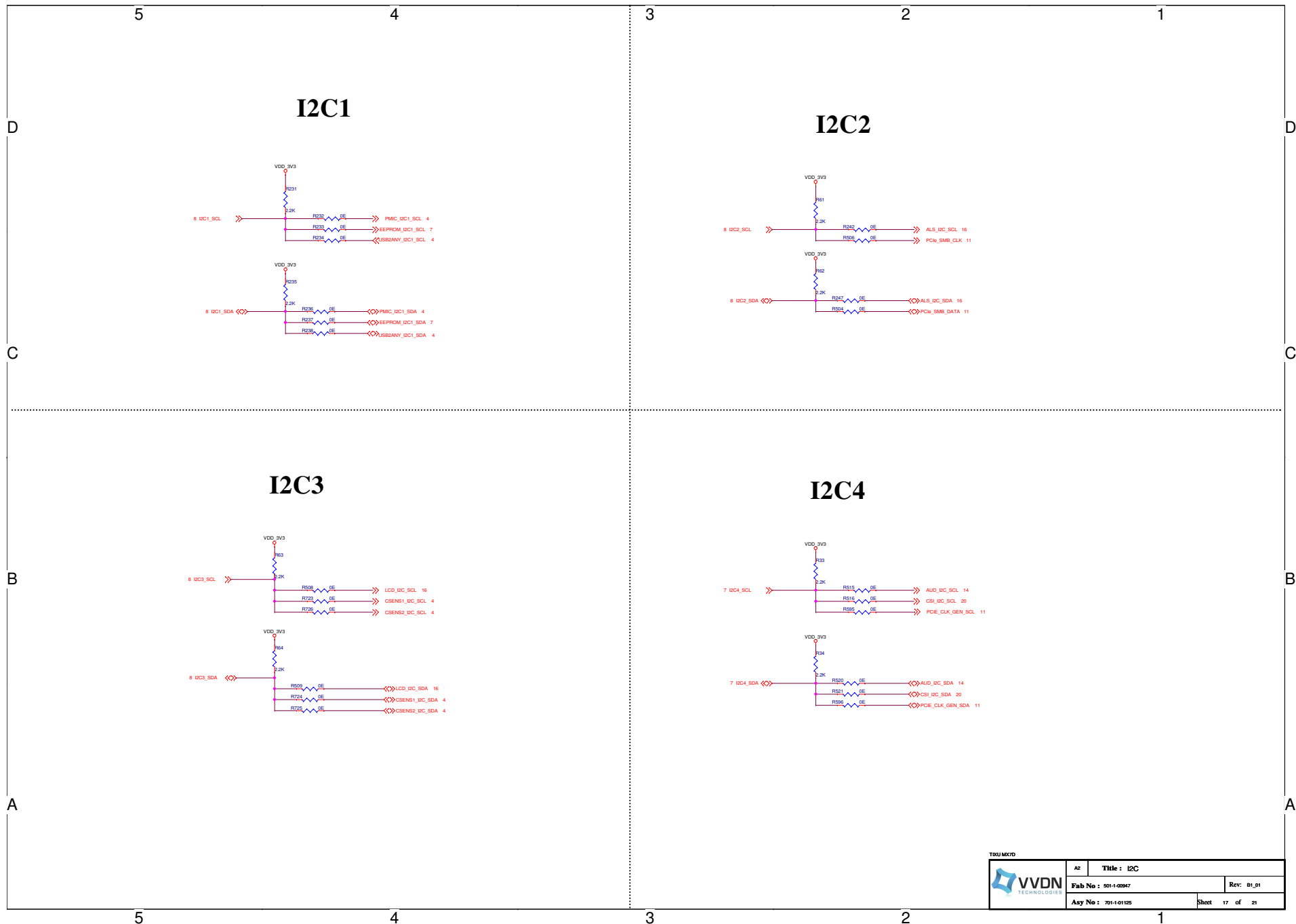
LCD1_DATA305

LCD1_DATA306

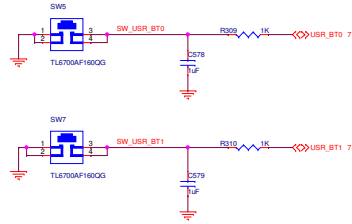
LCD1_DATA307

LCD1_DATA308

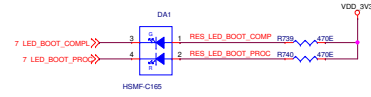
LCD1_DATA309



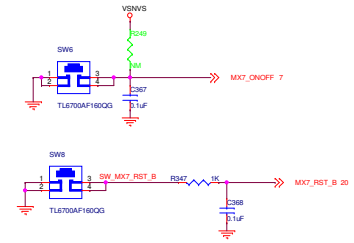
User Button



Status LED

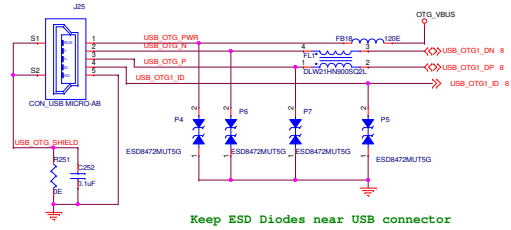


Power Button



USB OTG

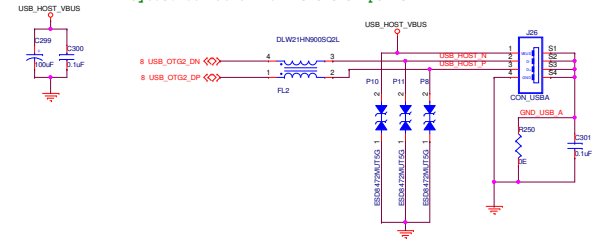
Layout: USB 90 ohm differential pairs



Keep ESD Diodes near USB connector

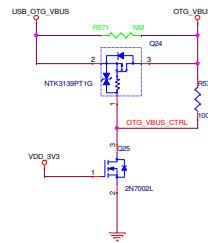
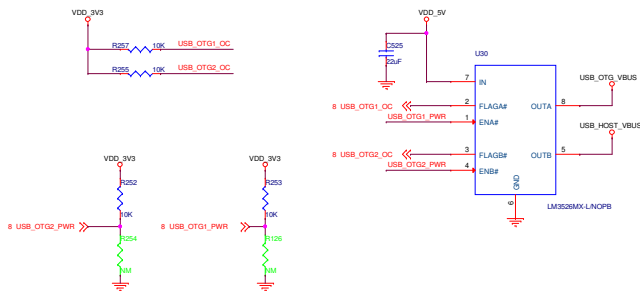
USB HOST

Layout: USB 90 ohm differential pairs



Keep ESD Diodes near USB connector

USB Power



TDLX MC7D			
	A2	Title : USB/BUTTON	
	Fab No : 501-00947		Rev: 01_01
	Asy No : 701-01125		Sheet 18 of 21

ETHERNET PHY

Layout: Place 49E9 Resistors in RX_D[0:3], RX_CLK, RX_CTRL as close to PHY

PHY address set to 0X00

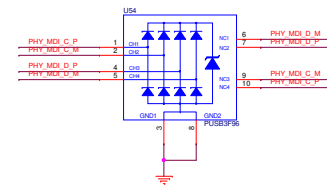
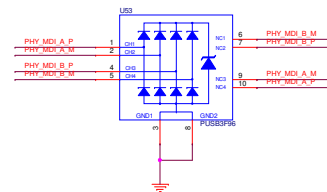
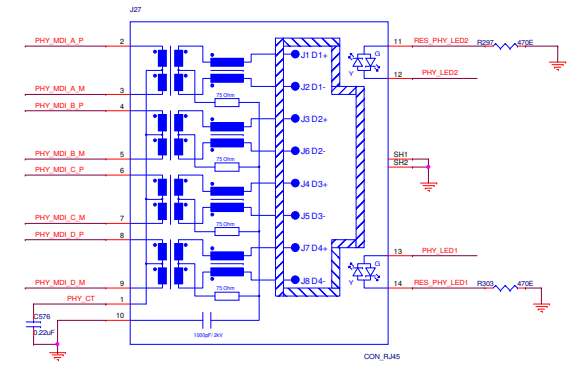
The RESET input must be held low for a minimum of 1ps

Layout: Place 1uF, 0.1uF capacitor as close as possible to VDD pins

Autoneg enable. For Disabling R306=2.49K, R300=NM

RGMII Clock Skew TX[0:2]=[000]
ANEG_SEL(Auto-negotiation)=[0]
PHY_LED[0:2] CANT CONFIGURE IN MODE4

All path length from P2, P3 should be kept small to minimize parasitic inductance. Also place near the connector J27



	A2	Title : ETHERNET	
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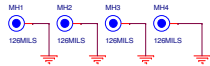
[illegible]

WATCH DOG

The diagram illustrates a Watch Dog timer circuit. The central component is the TPS3808QDS supervisor (U37). The VSNVS supply is connected to the VDD pin. The SENSE pin is connected to a network of resistors (R348, R127, R349) and capacitors (C185, C186, C187) connected to the MXT_RST_B and GWDOG_RST_B signals. The SUPER_MR_B pin is connected to the SENSE network. The RESET pin is connected to the SUPER_RST_B signal. The CT pin is connected to the SUPER_CT signal. The supervisor is also connected to the PMIC_ENABLE_ACDET and PMIC_ENABLE_47 signals through resistors (R350, R351) and capacitors (C188, C189).

MISCELLANEOUS

MOUNTING HOLES



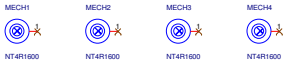
GLOBAL FIDUCIALS



LOCAL FIDUCIALS



MINI PCIe HANDOFF



TDX M07D		Title : MISCELLANEOUS	
VVDN TECHNOLOGIES		Fab No : 501-1-00947	Rev: 01_01
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