Schematics Drafted in : Allegro Design entry CIS 17.2

REV	Revision Notes	Designer	Approver	Date
A1	First Release	VVDN	TI	17-06-2019
A2	1. R538 Replaced with 300E Resistor 2. C535 Replaced with 4.7uF, 10V Capacitor 3. U37 replaced with TPS3808G25DBVR 4. D34 Made NO MOUNT 5. R660 Made NO MOUNT, R684 Mounted with 0E	VVDN	TI	05-09-2019
B1	1. SD card VCC voltage changed to VCC_3V3 2. Pin connection changed in USB2ANY header H1 3. Added Capacitor C578, C579 across SW5 and SW6 4. PGOOD LED of PMIC connected from PGOOD pin of TPS65218D0 5. PMIC_STANDBY from uP used for resetting DCDC1, DCDC2 of TPS65218D0 6. PMIC_GPIO1 used for enabling DCDC converters other than TPS65218D0	VVDN	TI	24-10-2019

TIXU_MX7D

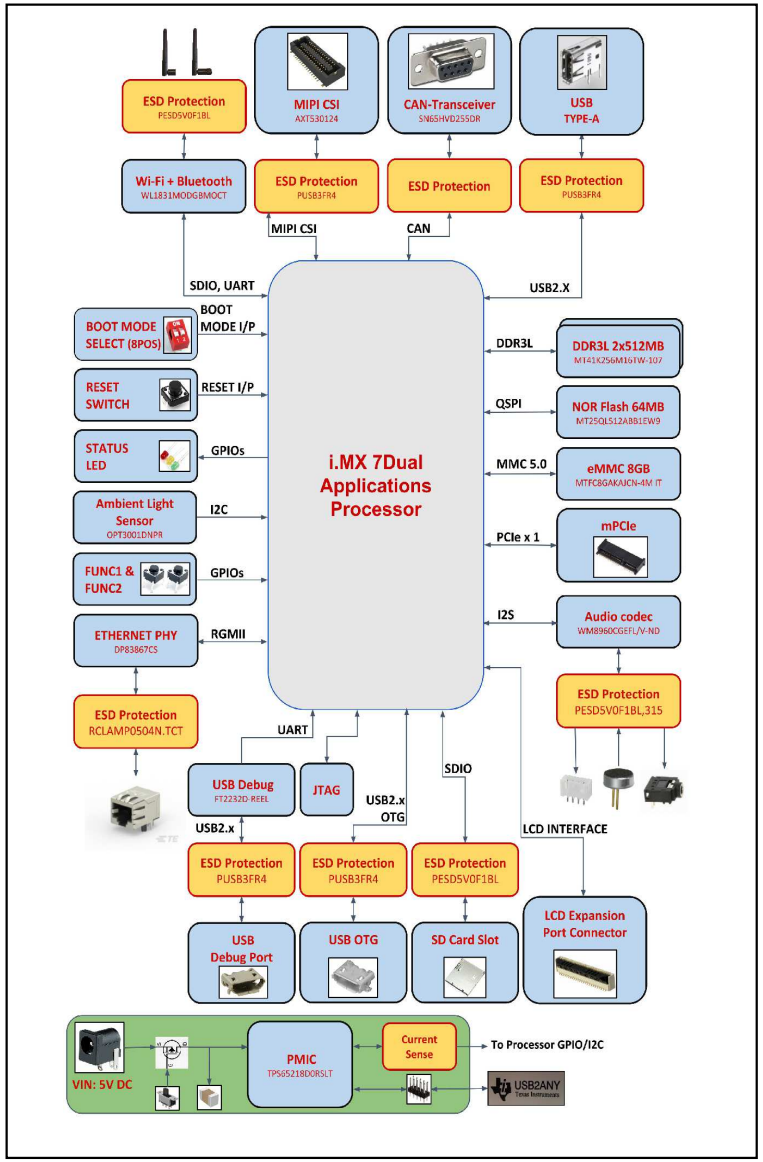
Content

TIXU MX7D

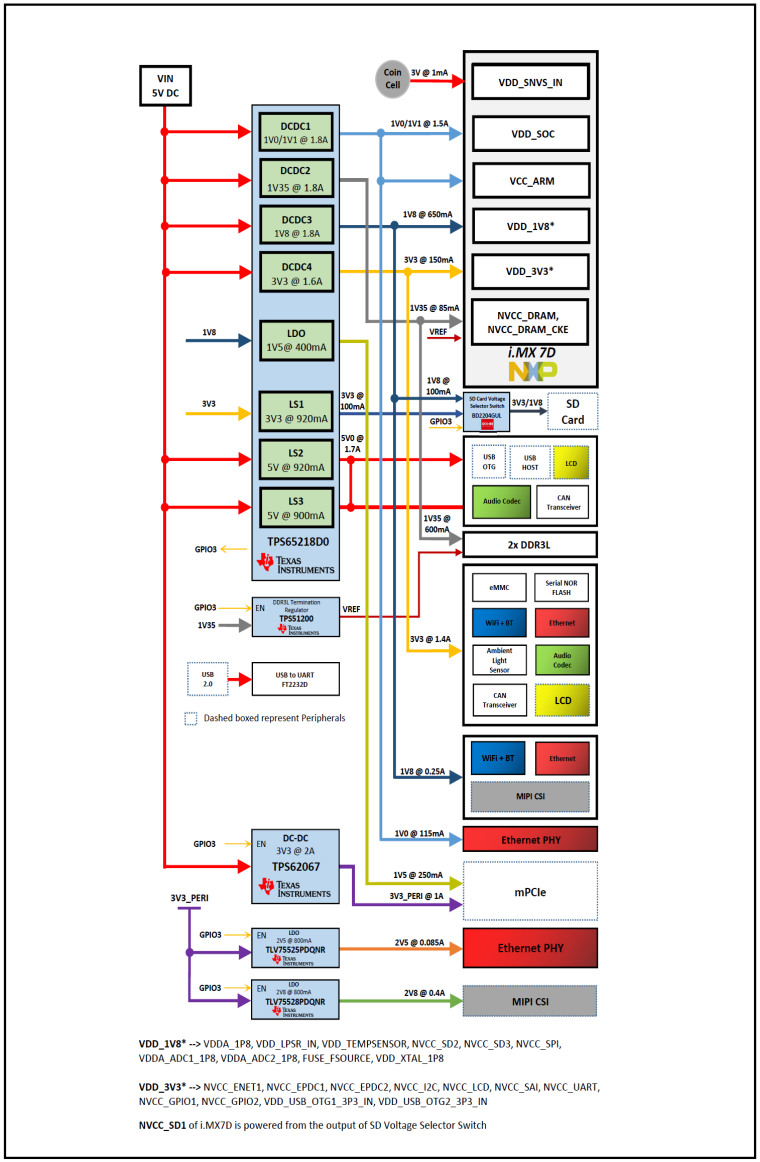
VVDN TECHNOLOGIES

A2	Title : COVER_PAGE	
Fab No : 501-1-00947		Rev: B1_01
Asy No : 701-1-01125		Sheet 1 of 21

BLOCK DIAGRAM



POWER ARCHITECTURE



VDD_1V8* --> VDDA_1P8, VDD_LPSR_IN, VDD_TEMPSENSOR, NVCC_SD2, NVCC_SD3, NVCC_SPI, VDDA_ADC1_1P8, VDDA_ADC2_1P8, FUSE_FSOURCE, VDD_XTAL_1P8

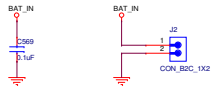
VDD_3V3* --> NVCC_ENET1, NVCC_EPDC1, NVCC_EPDC2, NVCC_I2C, NVCC_LCD, NVCC_SAI, NVCC_UART, NVCC_GPIO1, NVCC_GPIO2, VDD_USB_OTG1_3P3_IN, VDD_USB_OTG2_3P3_IN

NVCC_SD1 of i.MX7D is powered from the output of SD Voltage Selector Switch

TIDU MX7D

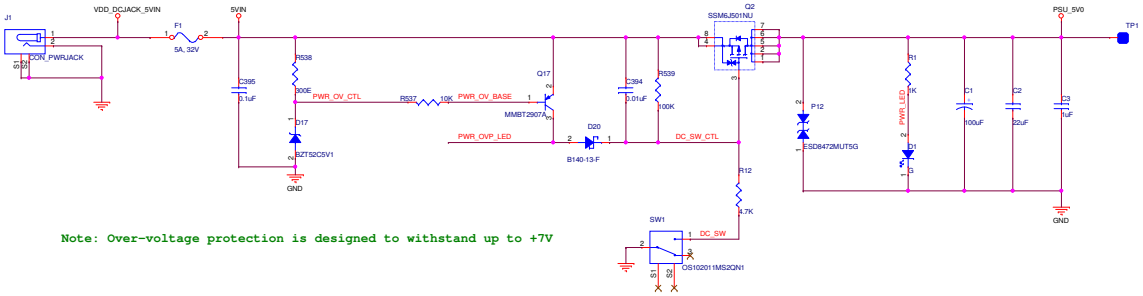
VVDN TECHNOLOGIES	A2	Title : BLOCK_DIAGRAM
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 2 of 21

BATTERY IN



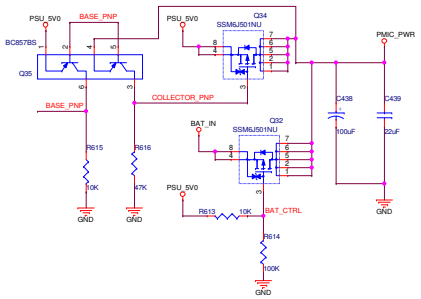
5V DC POWER

OVER VOLTAGE PROTECTION

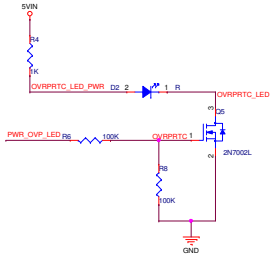


Note: Over-voltage protection is designed to withstand up to +7V

ORING



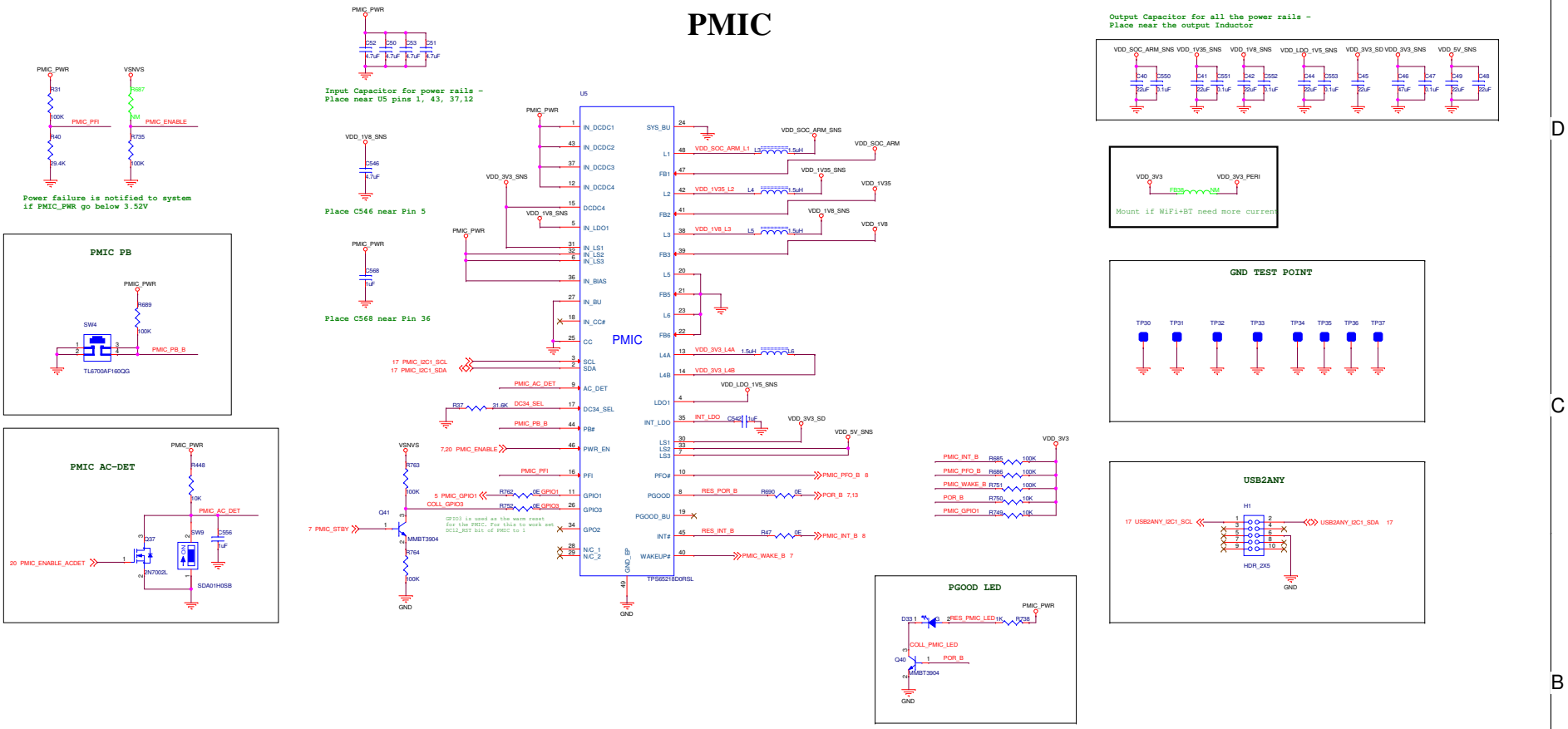
OVER VOLTAGE INDICATOR



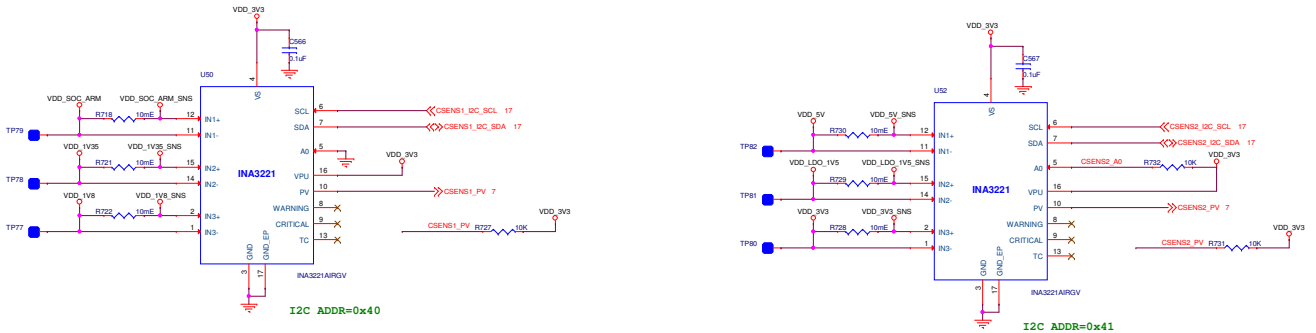
T0U MX7D

VVDN TECHNOLOGIES	A2	Title : MAIN POWER
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 3 of 21

PMIC

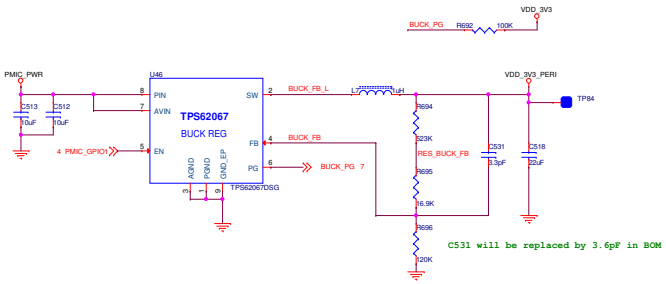


CURRENT AND VOLTAGE MONITORING

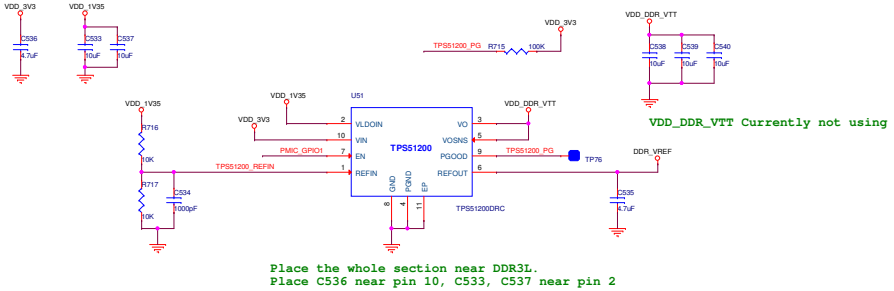


TDDU MX7D	A2	Title : PMIC	
VVDN TECHNOLOGIES	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 4 of 21	

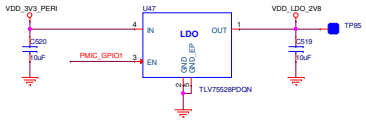
PERIPHERAL 3V3



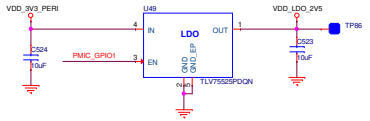
DDR3L VREF



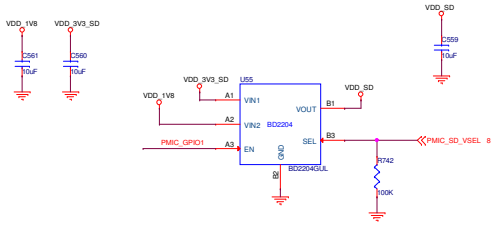
2V8 LDO



2V5 LDO



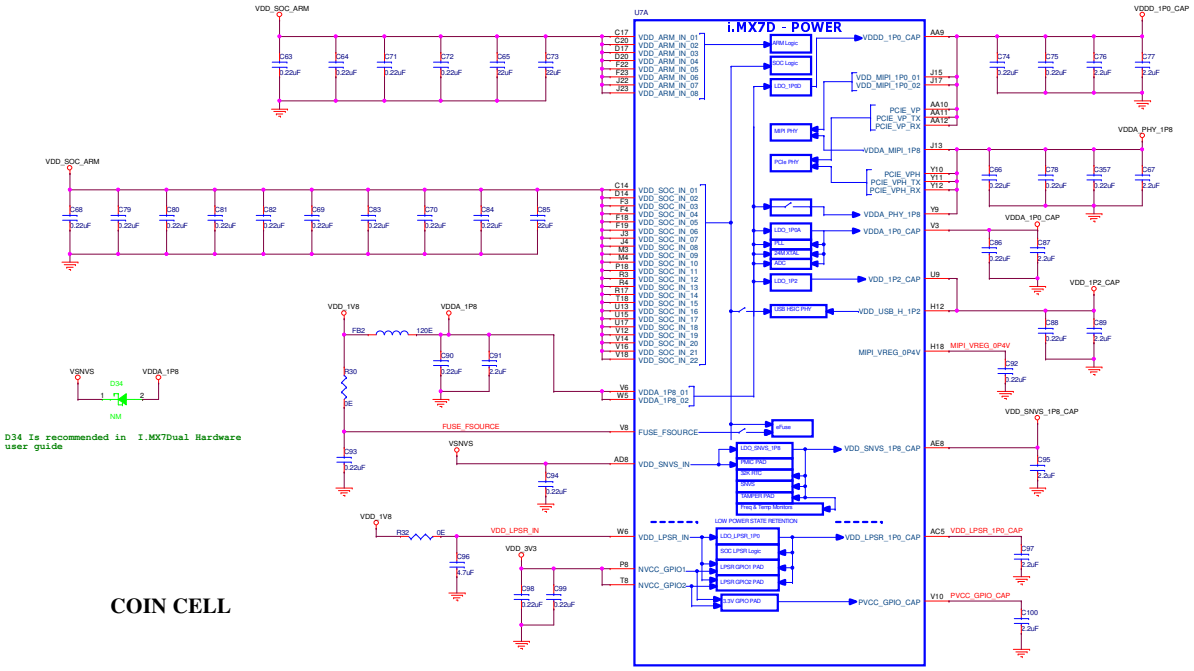
SD CARD VOLTAGE SELECT

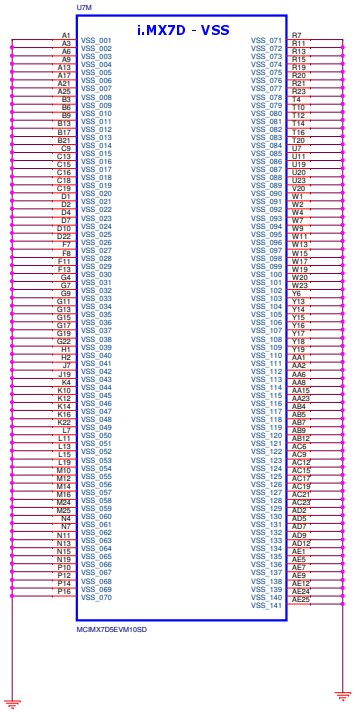


T8XU MX7D

VVDN TECHNOLOGIES	A2	Title : POWER DC-DC
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 5 of 21

CPU POWER





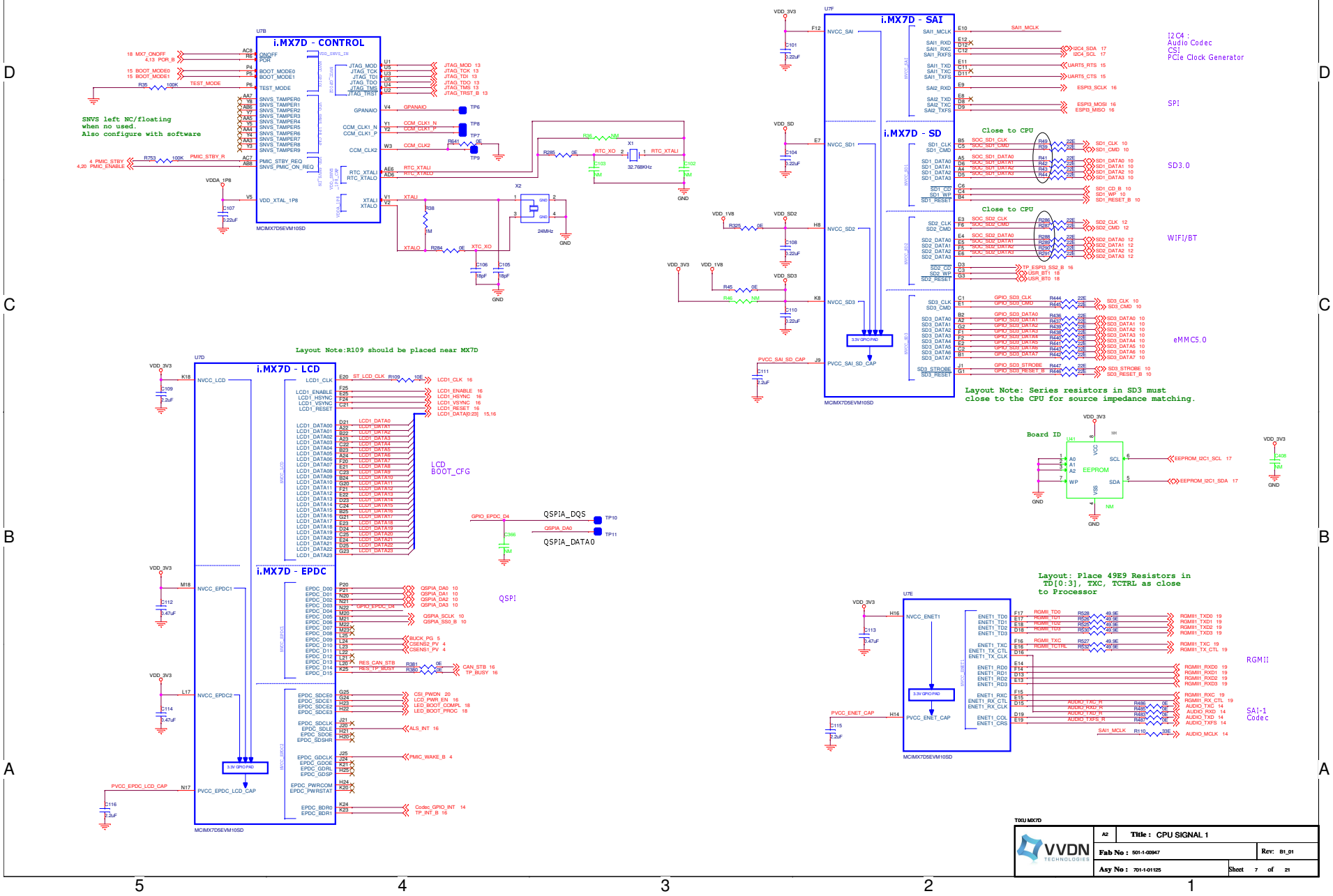
D34 Is recommended in I.MX7Dual Hardware user guide

COIN CELL

Place COIN CELL near AD8 of U7

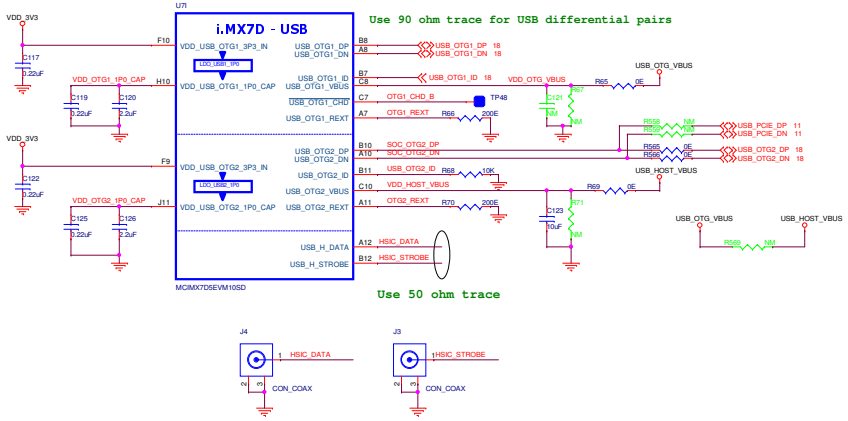
TXU MX7D	A2	Title : CPU POWER	
VVDN TECHNOLOGIES	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 6 of 21	

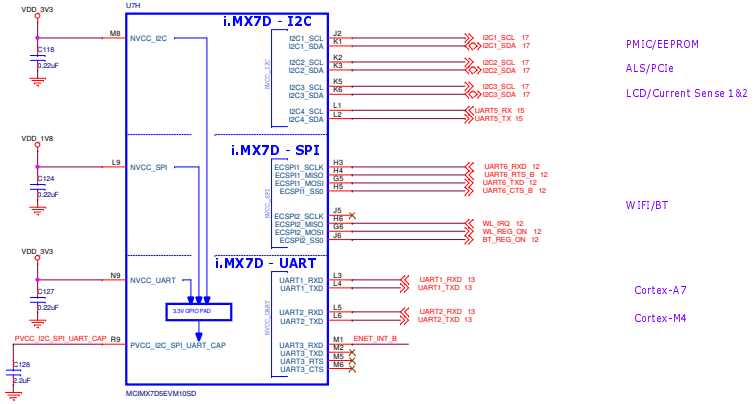
CPU SIGNAL 1

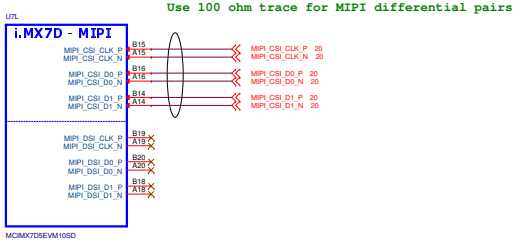


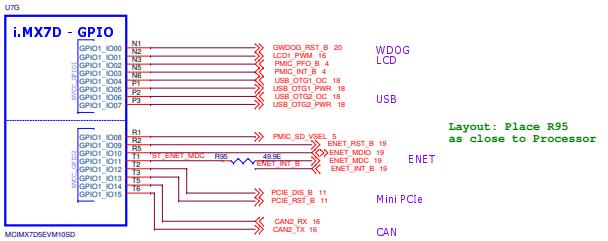
TXU MX7D	A2	Title : CPU SIGNAL 1	
VVDN TECHNOLOGIES	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 7 of 21	

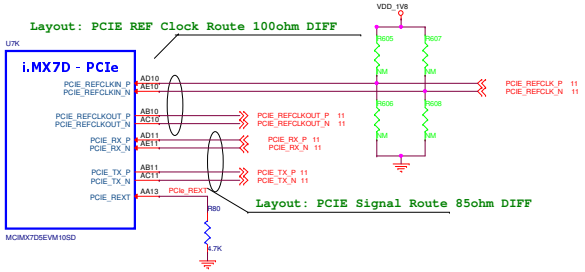
CPU SIGNAL 2

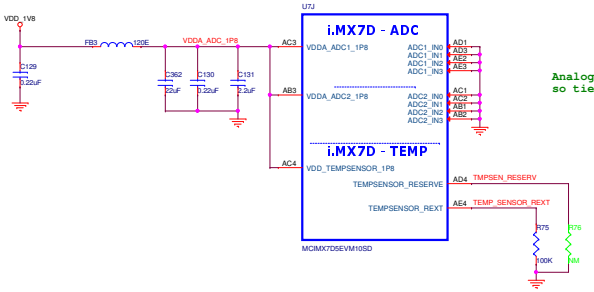












VVDN TECHNOLOGIES	A2	Title : CPU SIGNAL 2	
	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125		Sheet 8 of 21

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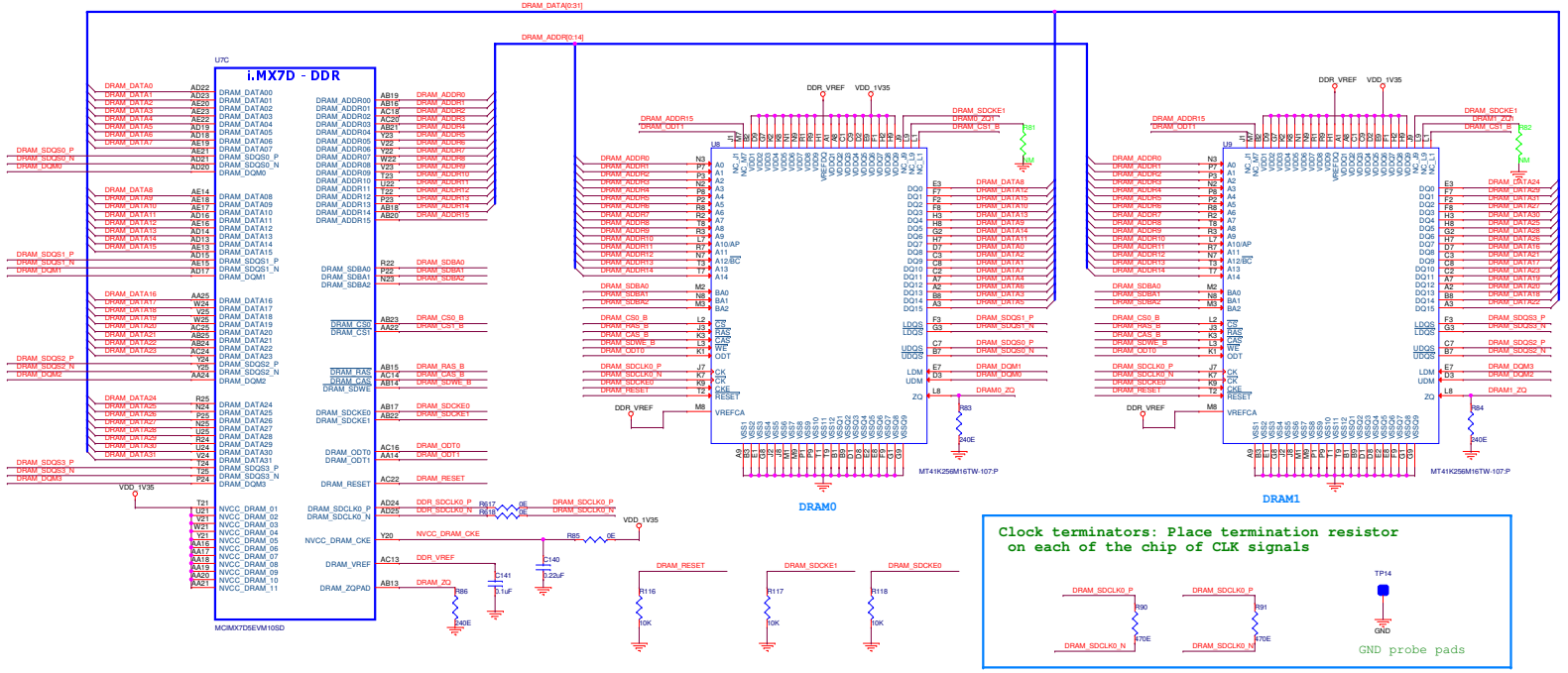
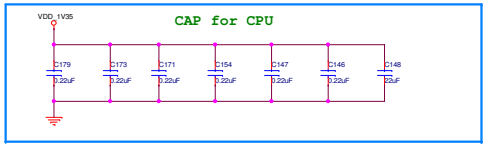
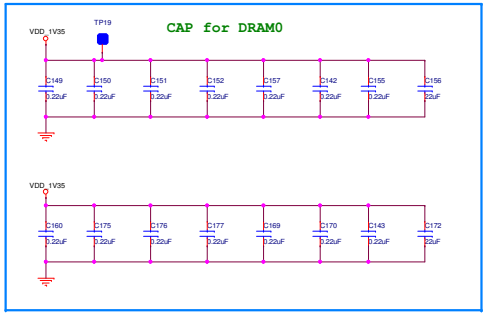
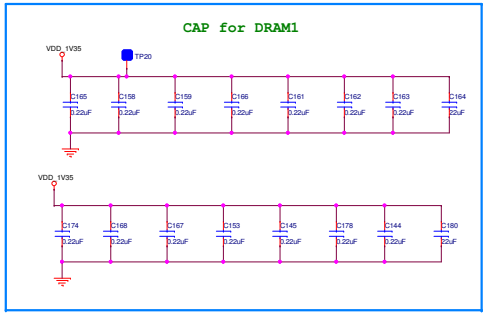
DDR3L





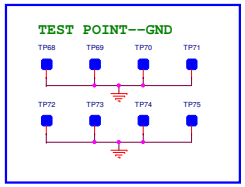




Note: test points for signal integrity measurement

Place near the i.MX7D side

Place near the DDR3L side



TXU MX7D

VVDN TECHNOLOGIES	A2	Title : DDR3L
	Fab No : 501-1-00947	Rev: B1_01
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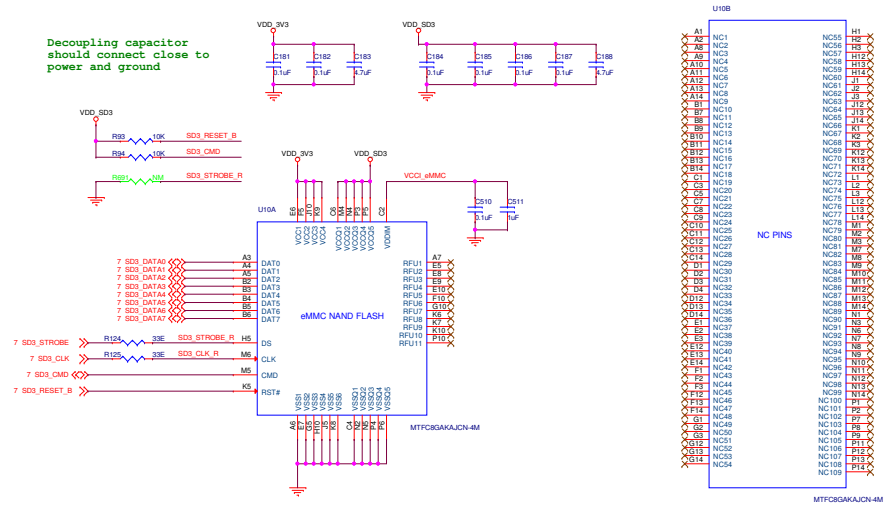
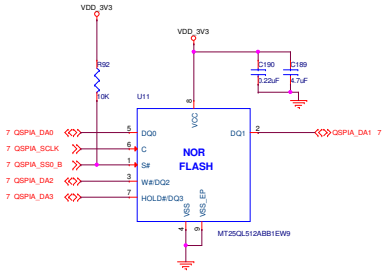
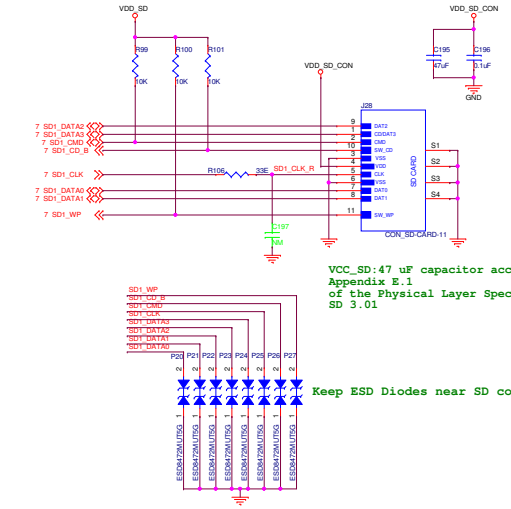
eMMC 5.0

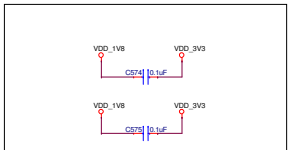


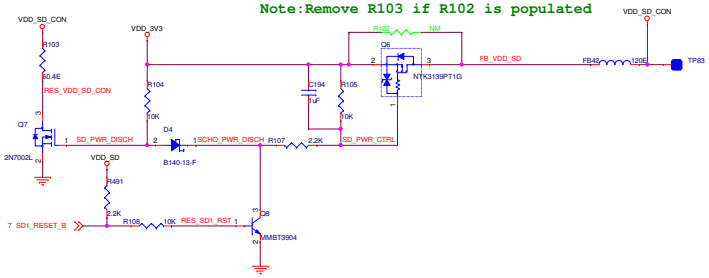
QSPI NOR FLASH



SD CARD



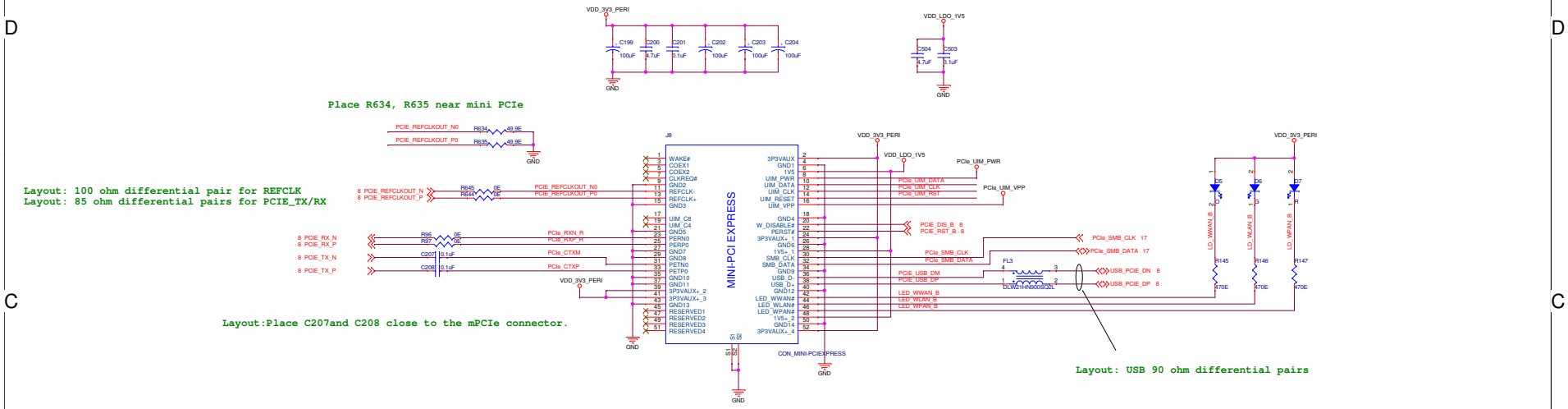




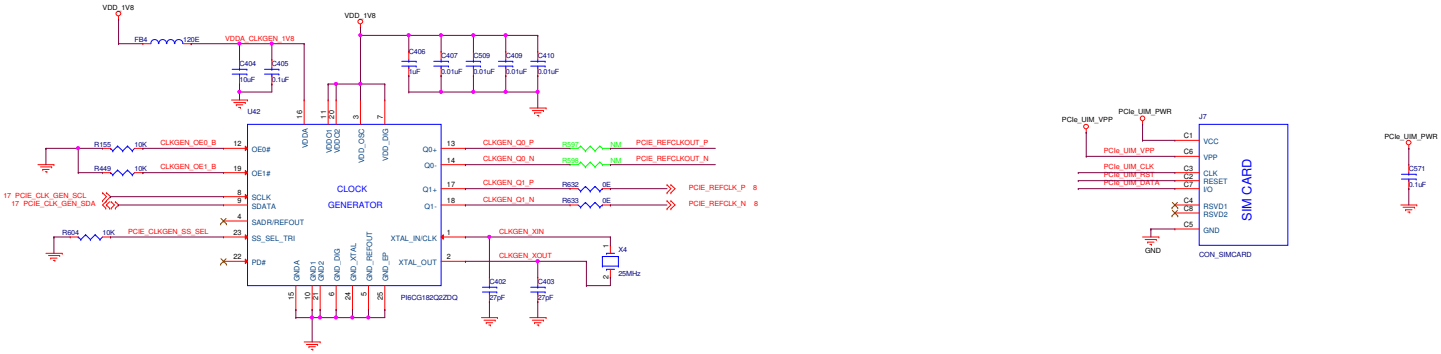
TIXU MX7D

VVDN TECHNOLOGIES	A2	Title : eMMC/FLASH/SD
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 10 of 21

Mini-PCIE



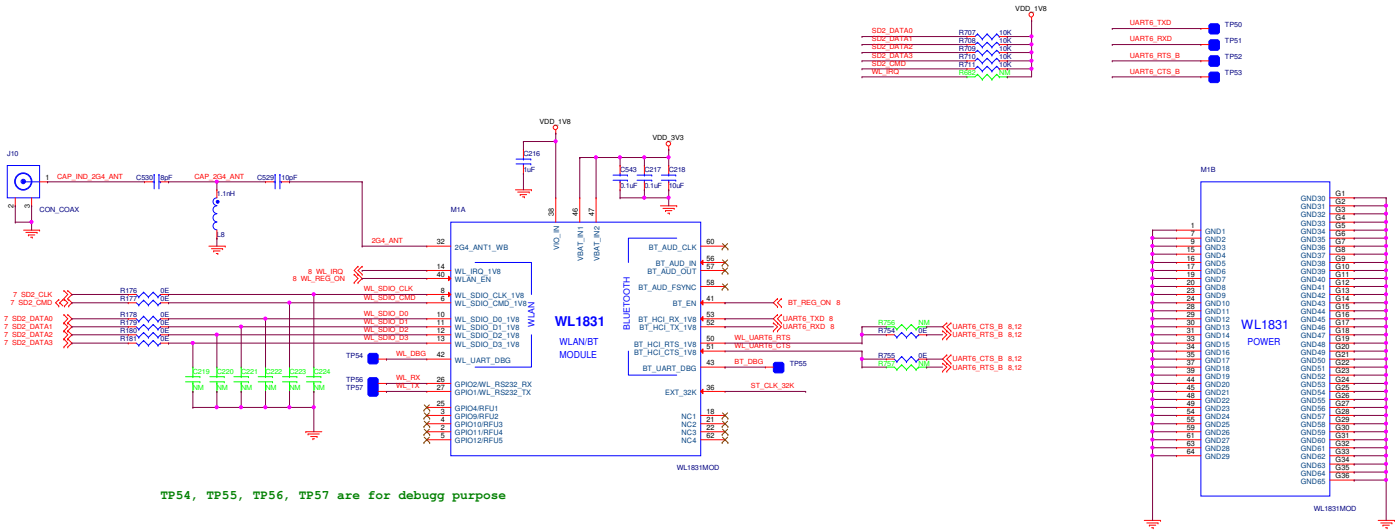
NOTE:
This design assumes a normal loading on the VDD_3V3_PERI rail of up to 1A.
The VDD_LDO_1V5 rail is allowed a maximum of 250 mA.



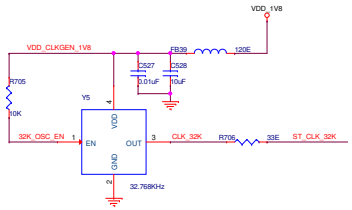
VVDN TECHNOLOGIES	A2	Title : mini_PCIe	
	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 11 of 21	

T0U MX7D

WiFi/BT

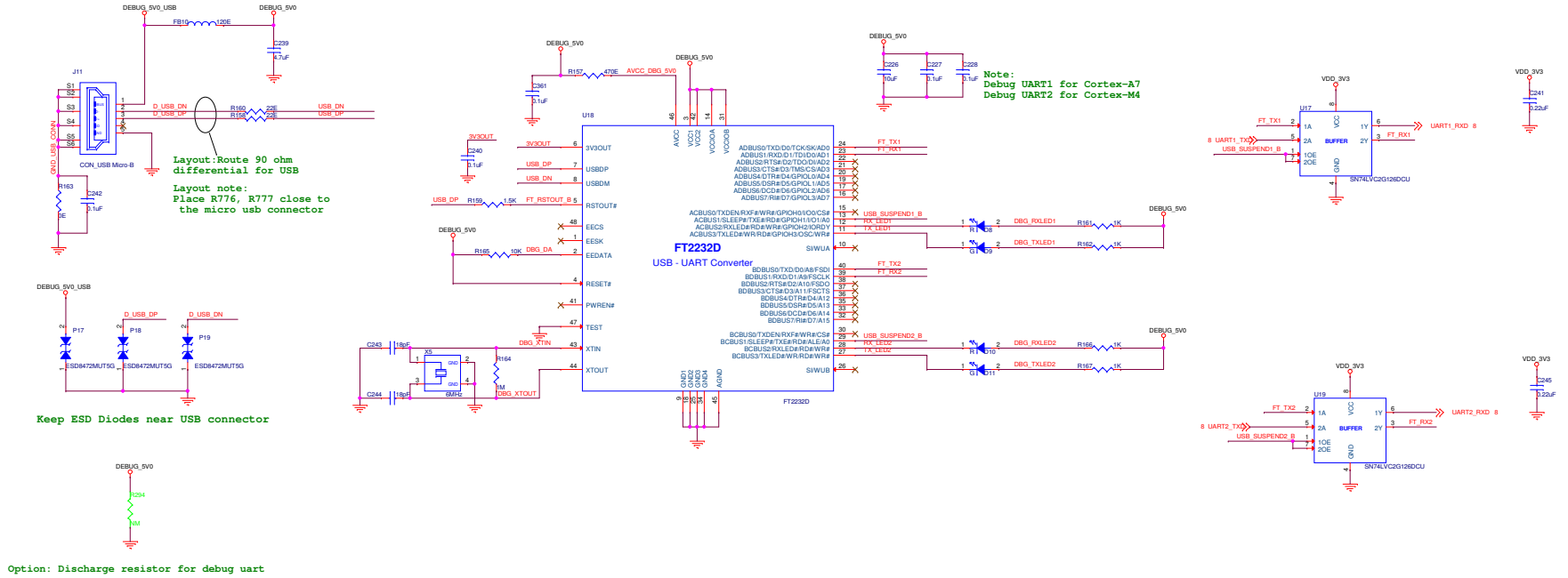


TP54, TP55, TP56, TP57 are for debugg purpose

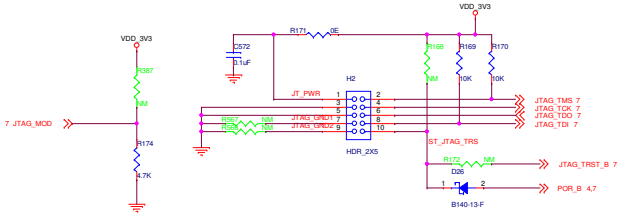


TIXU MX7D	A2	Title : WiFi/BT	
VVDN TECHNOLOGIES	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 12 of 21	

DEBUG UART

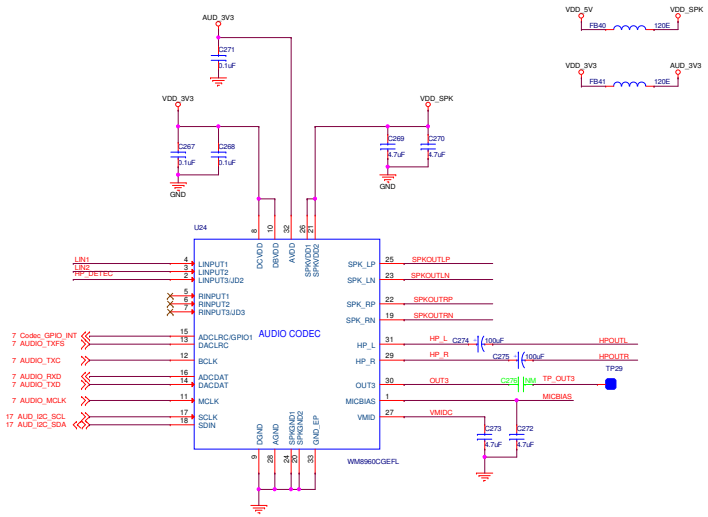


JTAG

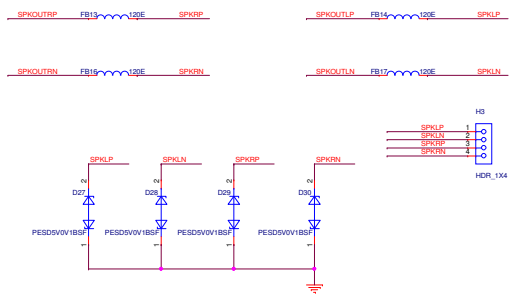


TIXU MX7D	A2	Title : DEBUG UART/JTAG	
VVDN TECHNOLOGIES	Fab No : 501-1-00947		Rev: B1_01
	Asy No : 701-1-01125	Sheet 13 of 21	

AUDIO

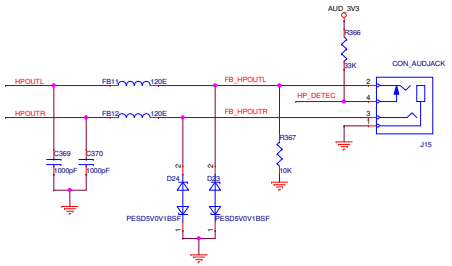


Speaker Out



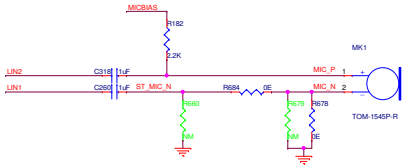
Keep ESD Diodes near SPK connector

HP OUT



Keep ESD Diodes near Headphone connector

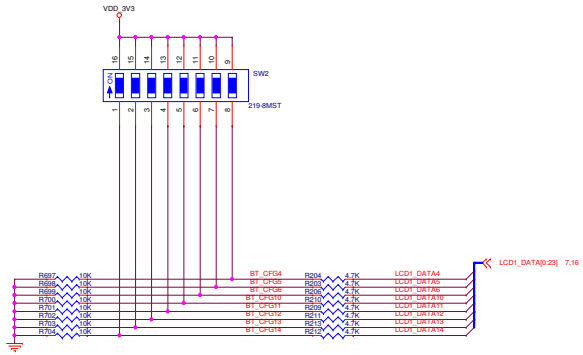
MIC INPUT



TIXU MX7D

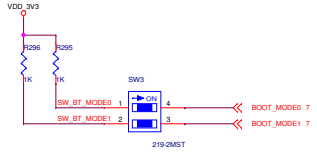
VVDN TECHNOLOGIES	A2	Title : AUDIO
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 14 of 21

BOOT CONFIG



BOOT MODE

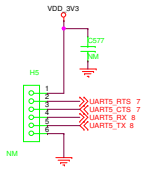
BOOT_MODE[1:0]	Boot type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved



BOOT TABLE – SW2

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3		0	0	Bus Width: 0 - 1-bit 1 - 4-bit
010 = MMC/eMMC Boot					Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)		
100 = QSPI Boot			0	0	0	0	0

UART HEADER

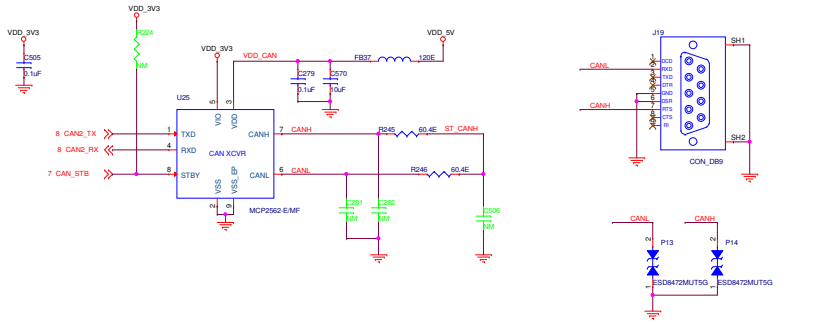


TIXU MX7D

VVDN TECHNOLOGIES

A2	Title : BOOT/UART HEADER	
Fab No : 501-1-00947		Rev: B1_01
Asy No : 701-1-01125		Sheet 15 of 21

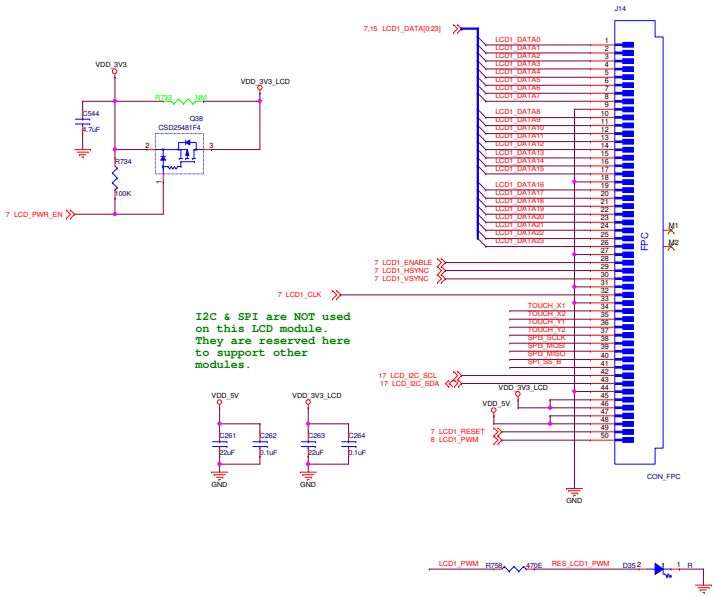
CAN



Keep ESD Diodes near CAN connector

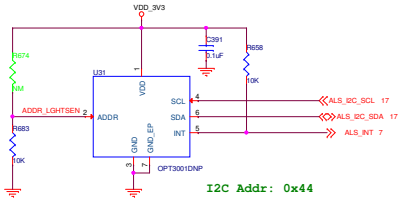
LCD

ADAFRUIT LCD



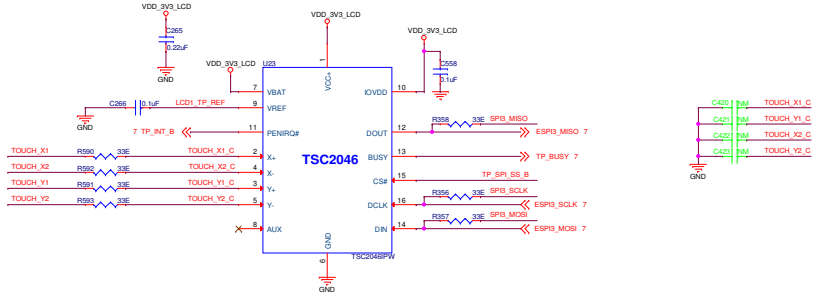
I2C & SPI are NOT used on this LCD module. They are reserved here to support other modules.

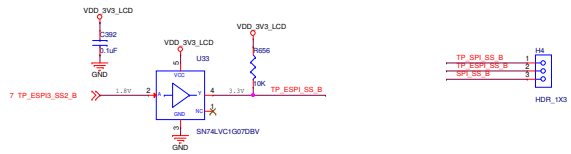
Ambient Light Sensor



I2C Addr: 0x44

Place C265 near VBAT





TIXU MX7D

VVDN TECHNOLOGIES	A2	Title : CAN,LCD/ALS
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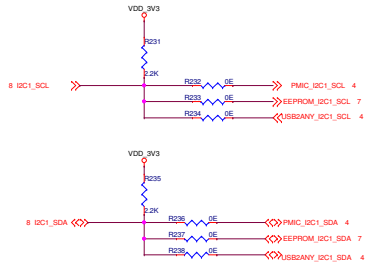
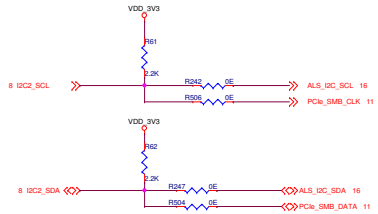
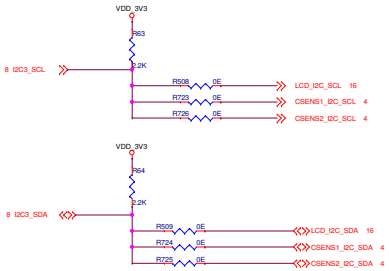
I2C1



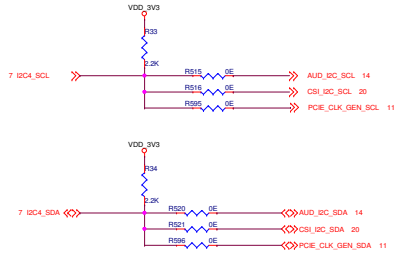
I2C2



I2C3



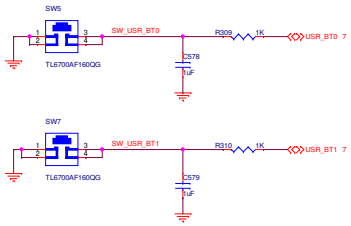
I2C4



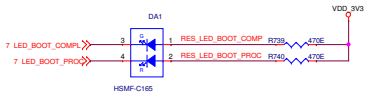
T8XU MX7D

VVDN TECHNOLOGIES	A2	Title : I2C
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 17 of 21

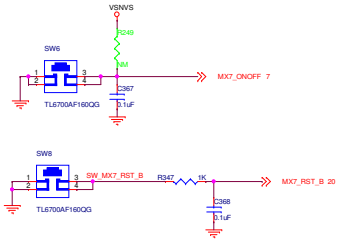
User Button



Status LED

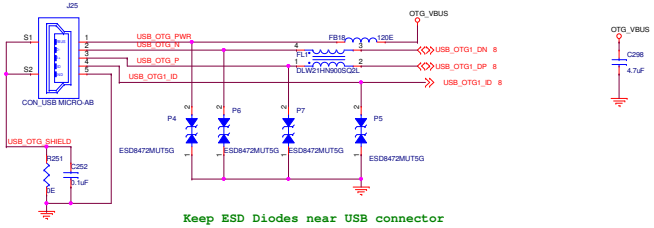


Power Button



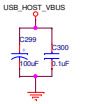
USB OTG

Layout: USB 90 ohm differential pairs

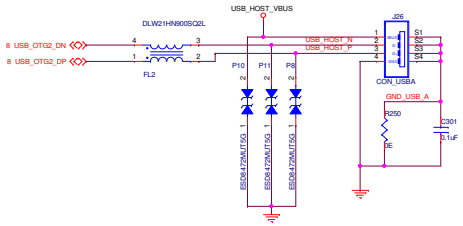


Keep ESD Diodes near USB connector

USB HOST

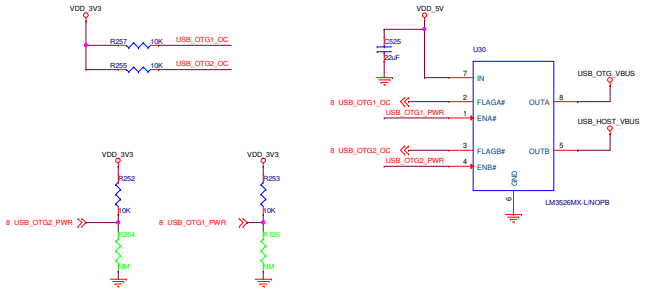


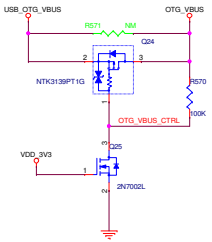
Layout: USB 90 ohm differential pairs



Keep ESD Diodes near USB connector

USB Power

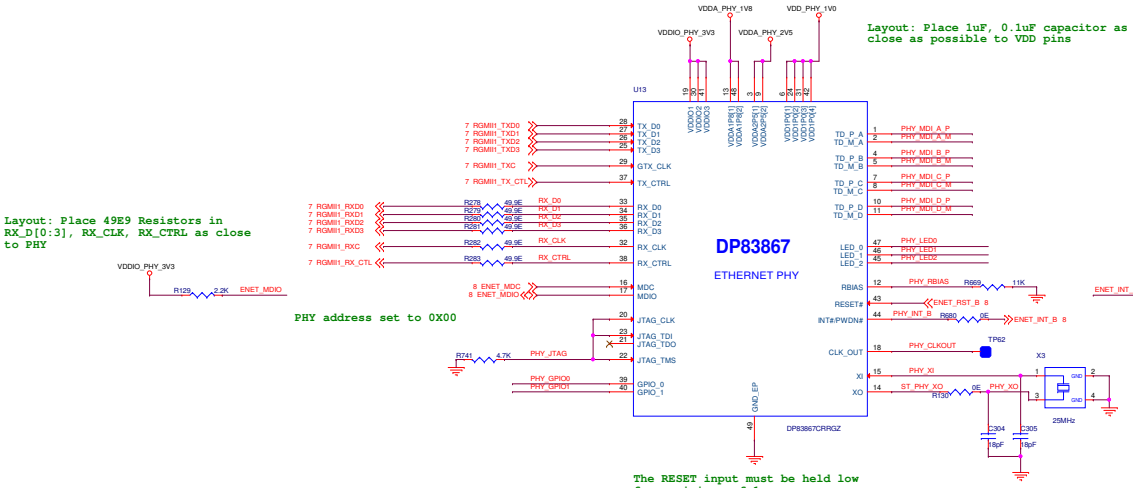


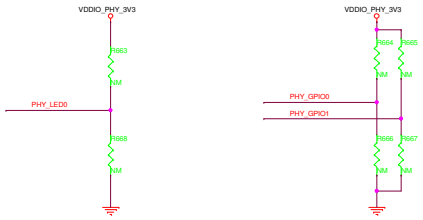


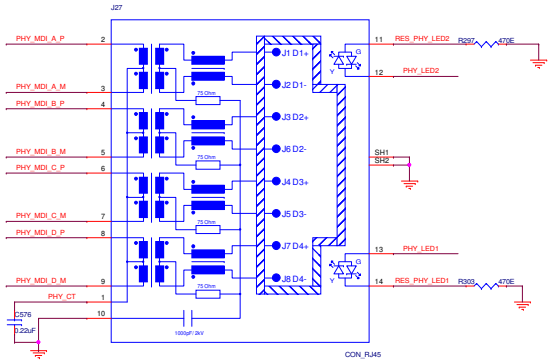
TIXU MX7D

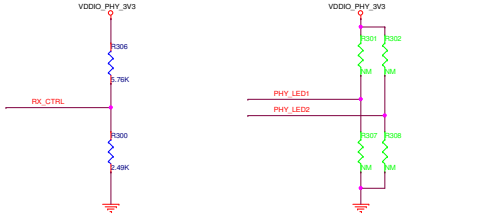
VVDN TECHNOLOGIES	A2	Title : USB/BUTTON
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 18 of 21

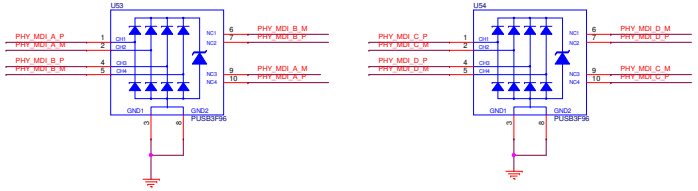
ETHERNET PHY











All path length from P2, P3 should be kept small to minimize parasitic inductance. Also place near the connector J27

TIXU MX7D

VVDN TECHNOLOGIES	A2	Title : ETHERNET
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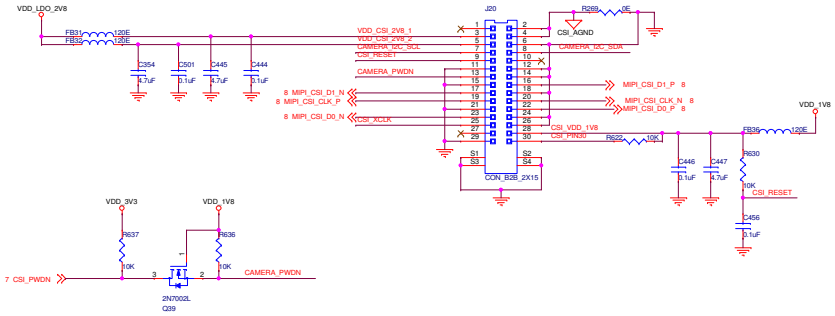
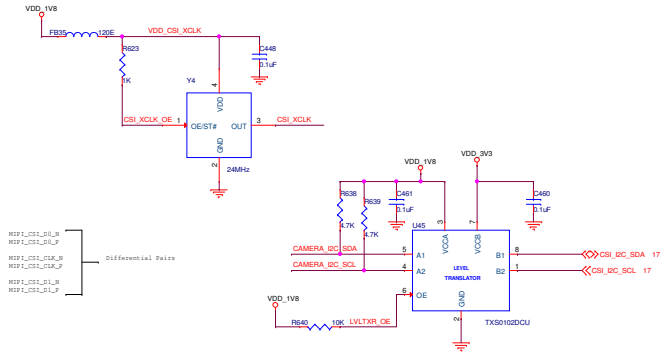
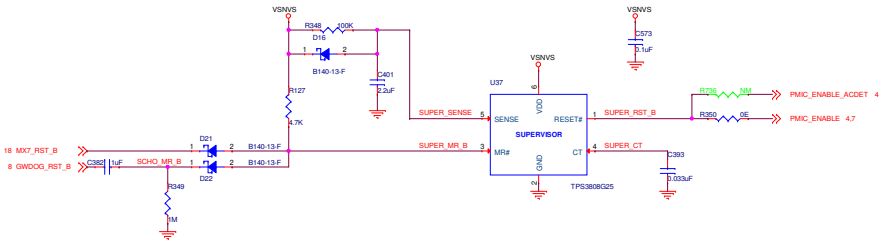
CSI





TXS0102 Have internal pull up of value 10K at A1, A2, B1, B2 pins

WATCH DOG



TIXU MX7D

VVDN TECHNOLOGIES	A2	Title : CSI/WATCHOG/IO
	Fab No : 501-1-00947	Rev: B1_01
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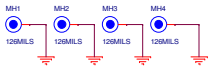
MISCELLANEOUS

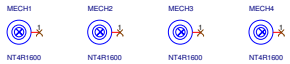
MOUNTING HOLES



GLOBAL FIDUCIALS

LOCAL FIDUCIALS

MINI PCIe HANDOFF



TIXU MX7D

VVDN TECHNOLOGIES	A2	Title : MISCELLANEOUS
	Fab No : 501-1-00947	Rev: B1_01
	Asy No : 701-1-01125	Sheet 21 of 21