Functional Safety Information

TPS22918-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS22918-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

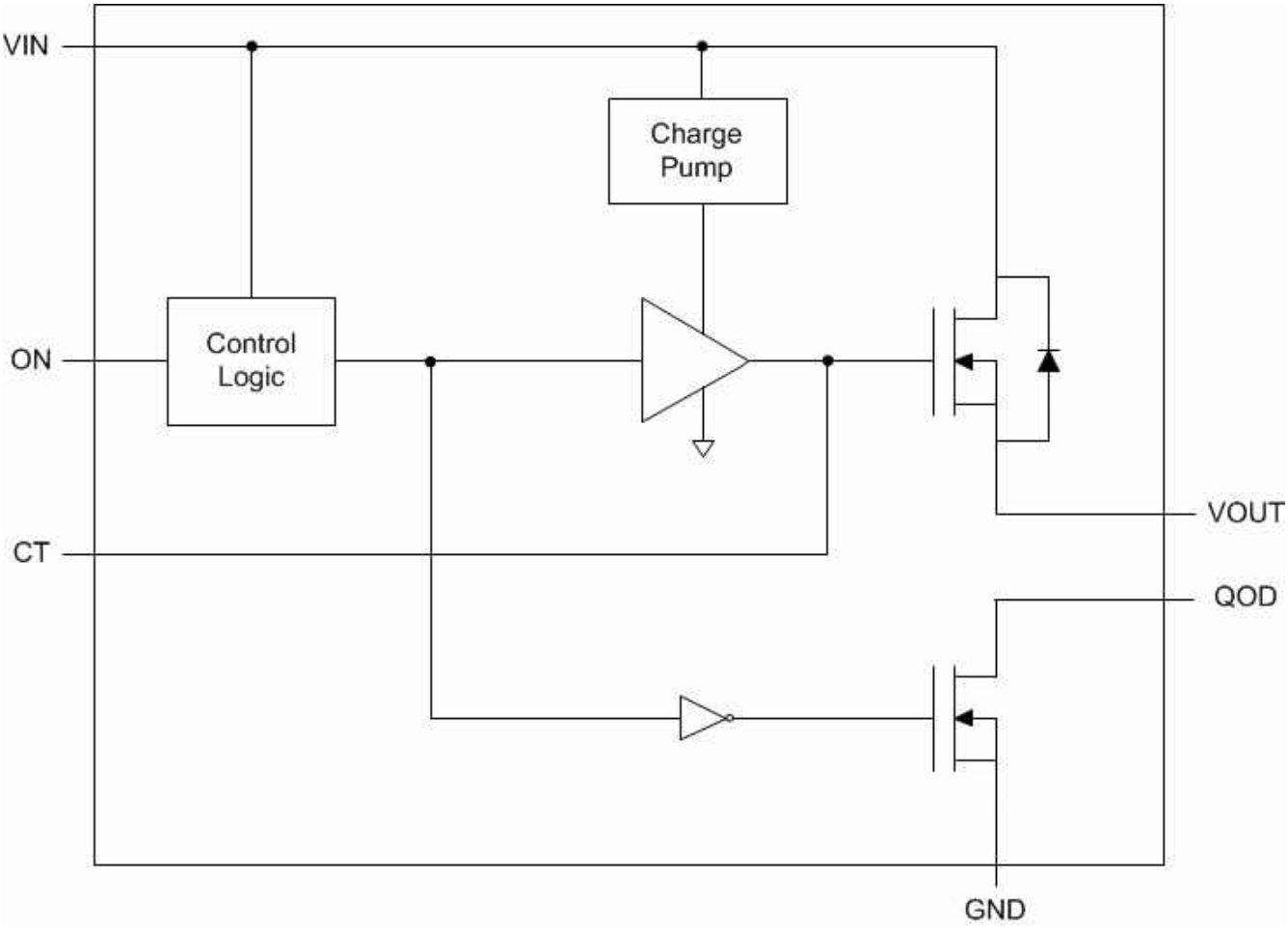

Figure 1-1. Functional Block Diagram

TPS22918-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS22918-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	4
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS22918-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open or Hi-Z	25%
VOUT stuck on (VIN)	15%
VOUT outside specification (voltage or rise time)	45%
QOD stuck on	5%
QOD stuck off	5%
Pin to pin short (any two pins)	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS22918-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS22918-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS22918-Q1 data sheet.

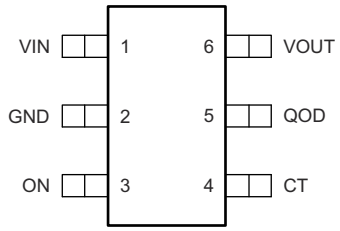

Figure 4-1. Pin Diagram

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND.
2	GND	—	Device ground
3	ON	I	Active high switch control input. Do not leave floating
4	CT	O	Switch slew rate control. Can be left floating.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin disconnected
6	VOUT	O	Switch output

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Absolute maximum ratings are not exceeded.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	The power supply is shorted.	D
GND	2	This is the GND pin. Normal operation.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ON	3	Device is disabled.	D
CT	4	Grounding this pin will prevent the device from turning on and may damage the device.	A
QOD	5	If the QOD pin is left floating in the application, short to ground has no effect. If the QOD pin is connected to VOUT, the device will not limit the power supply current and will be damaged.	D / A
VOUT	6	If the device is enabled, the device will not limit the power supply current and will be damaged.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	No power supply to the device. The device will not pass through voltage to VOUT.	D
GND	2	No GND connection to the device. Not functional.	B
ON	3	ON pin may float high or low, output state will not be known.	B
CT	4	Opening this pin will quicken the output rise time if a CT capacitor is attached.	C
QOD	5	If the QOD pin is left floating in the application, open-circuit has no effect. If the QOD pin is connected to VOUT, the device will no longer have quick output discharge functionality.	D / B
VOUT	6	The output will not deliver the voltage to the load.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	GND	The power supply is shorted.	D
GND	2	ON	Device is disabled.	D
CT	4	QOD	Device may exhibit odd switching behavior. Damage may occur.	A
QOD	5	VOUT	If the QOD pin is left floating in the application, this adds quick output discharge functionality. If the QOD pin is connected to OUT, the device will function as expected.	B / D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	Normal operation expected.	D
GND	2	The power supply is shorted.	D
ON	3	Device is enabled if the power supply is above the ON threshold (V_{IH})	D
CT	4	Biasing the CT pin may damage the device.	A
QOD	5	If the QOD pin is left floating in the application, this has no functional effect. If the QOD pin is connected to VOUT, the power MOSFET is shorted, and disabling the device will no longer block power to VOUT.	D / B
VOUT	6	Power MOSFET is shorted. Disabling the device will not longer block power to VOUT.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (August 2021)	**Page**
• Updated to current TI format	2

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