Application Report

Multiple FETs with the BQ76952, BQ76942 Battery Monitors

Willy Massoth

ABSTRACT

The typical schematics for the BQ76952 and BQ76942 battery monitors show single high-side series FETs. Many designers need to parallel FETs in their designs for current capability or heat dissipation. This document discusses and shows results of switching multiple FETs using BQ76952 devices and provides an example for designers implementing multiple FETs with this or other devices in the BQ769x2 family.

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1 Introduction

A typical battery has one set of terminals for both charge and discharge. Current passes through charge and discharge FETs arranged in series. Since the current flows through both FETs, the size and quantity used for charge and discharge are the same. The BQ76952 family of battery monitors consisting of the BQ76942 and BQ76952 support high-side series FETs. References to the BQ76952 in this document will generally apply to all family members unless specifically indicated. A typical schematic with the BQ76942 and series FETs is shown in Figure 1-1. The schematic is for a 7-cell implementation and includes pre-charge and pre-discharge FETs. The pre-charge path is used to limit current into the battery from a fixed voltage charger when the battery is deeply discharged. The pre-discharge path is used to charge high capacitive loads without a high current spike. With the series FETs, there is the possibility of charging through a disabled discharge FET or discharging through a disabled charge FET. The current through the body diode of the disabled FET can produce significant heat, so the BQ76952 devices use a body diode protection feature to enable the FET when current is flowing in the non-protected direction.

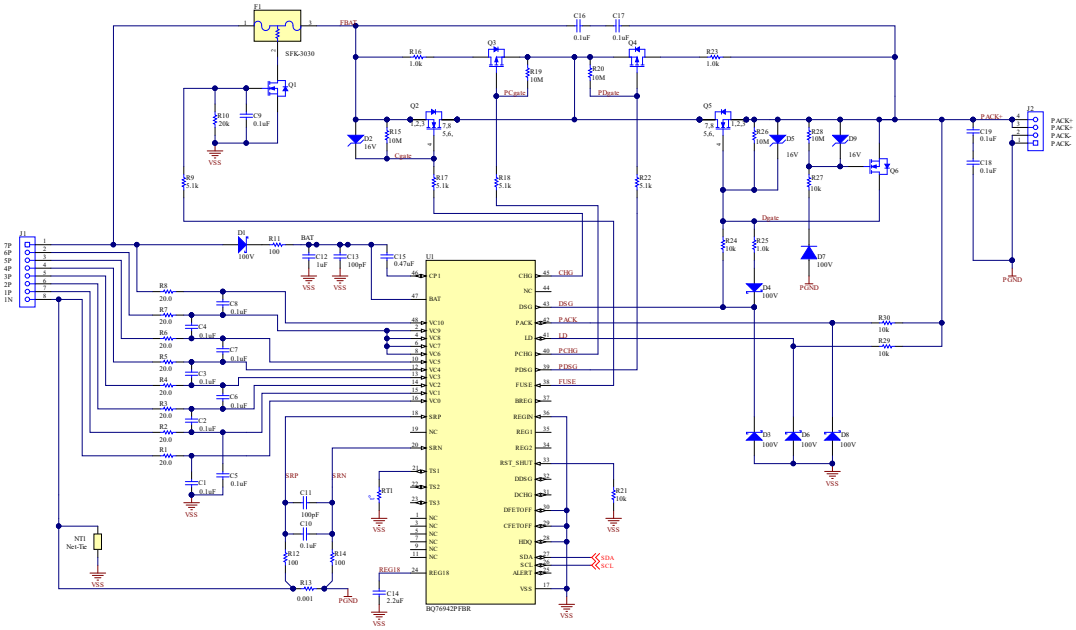

Figure 1-1. Typical 7S Series FET Schematic

The cell count and circuit configuration around the and low voltage pins of the device will vary with the implementation and will typically not be shown in further schematics in this application report. Like the main power FETs, the pre-charge and pre-discharge FETs must be selected for the application. The pre-charge and pre-discharge circuits are relatively low current to avoid high power in the battery pack and are not a focus of this application report.

2 Reverse Charge Circuit

The schematic includes a reverse charge circuit consisting of Q6 and the components surrounding its gate. The purpose of the circuit is to hold the gate of the discharge power FET at the source potential to keep it off when the PACK+ terminal is pulled below VSS. This circuit can be an important feature when a system uses a common connector such as a coaxial power connector for the charger. Since adapters with both polarities are available in the market, the incorrect charger could be attached resulting in both the battery and charger pushing current in the same direction. A discharge fault will occur and the PACK+ terminal could be pulled below VSS and the battery-. Since DSG does not go below VSS of the IC, without Q6 the gate of Q5 will be held near VSS while the source (PACK+) is pulled down by the charger. Current continues to flow from the battery as Q5 operates as a source follower, see Figure 2-1.

With the Q6 reverse charge circuit, when PACK+ is pulled below VSS the source of Q6 is pulled below its gate which is held up by D7 and R27. When Q6 turns on it pulls the Q5 gate to its source keeping the discharge FET off. Since DSG of U1 can not go below VSS, voltage is dropped across R24 which must be sized to dissipate the power required for the applied voltage. D4 blocks current through the smaller R25 which is selected for the turn off speed of Q5. DSG is not intended to provide power, D3 will carry the current rather than the IC pin. Similarly LD and PACK pins on U1 are not intended to provide power, D6 and D8 provide a current path when PACK+ is forced below VSS. If PACK+ is sufficiently below VSS, D9 will conduct keeping a safe VGS voltage on the Q6 gate with the additional voltage across R27. R28 keeps Q6 off when PACK+ is in a normal range. Figure 2-2 shows an example of the reverse charge circuit operation.

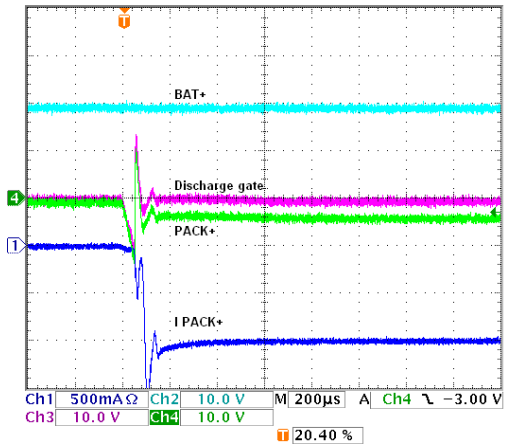

Figure 2-1. Negative PACK+ Without Reverse Charge Circuit

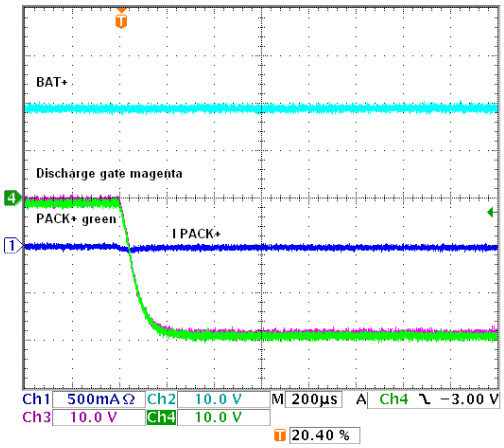

Figure 2-2. Negative PACK+ With Reverse Charge Circuit

3 Charge Pump (and FET Turn On)

The BQ76952 uses a charge pump to provide a voltage above the battery+ to turn on the high-side N-channel MOSFETs used in the system. The flying capacitor for the charge pump is internal, charge is stored in the CP1 capacitor external to the device. CP1 is the supply for the CHG and DSG drivers. In figures Figure 3-1 to Figure 3-4 the BQ76952 has been set to SHUTDOWN mode and is awakened by the TS2 signal. When the charge pump is at voltage it will turn off until its voltage drops and it runs again. It is common to see a ripple on the CP1 voltage, a slow drop followed by a rapid rise. In Figure 3-1 notice the slow cycling before the FETs turn on and the faster ripple once the FETs are on with the added load of the R_{GS} resistors and the load of the additional scope probes. Figure 3-2 shows more detail of the charge pump ramp at low voltage. Rise time is longer at the normal voltage shown in Figure 3-3. Using a larger CP1 capacitor also increases the rise time as in Figure 3-4. Notice the charge pump is still transitioning as the FETs turn on. Using a CP1 capacitor larger than 2.2 µF is not recommended with the BQ769x2 family devices.

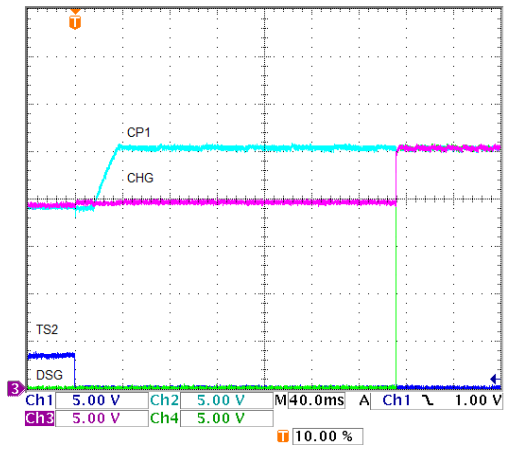

Figure 3-1. Charge Pump and FET Turn On, Low Voltage, 470 nF

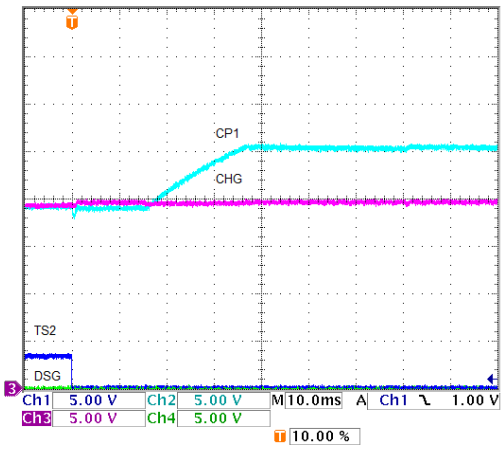

Figure 3-2. Charge Pump Start, Low Voltage, 470 nF

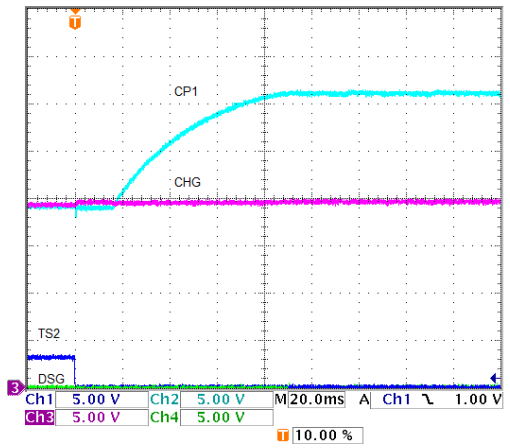

Figure 3-3. Charge Pump Start, Normal, 470 nF

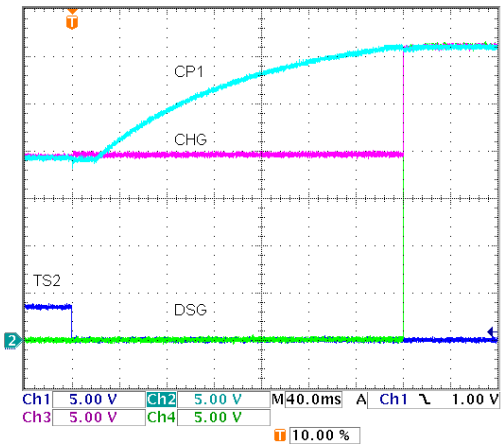

Figure 3-4. Charge Pump Start and FET Turn On, 2 µF CP1 Cap

The rounded shape of the CP1 signal at startup indicates the charge pump can produce more current at a lower voltage. CP1 is the power supply for the high side FET drivers. When CHG or DSG turn on the current for the CHG and DSG to turn on the FETs comes from the CP1 capacitor. As an approximation with ideal switching

charge is not lost and the charge on the CP1 capacitor before turn on is distributed between CP1 and the FET gate capacitance after turn on.

$$Q = V1 \times C_{CP1} = V2 \times (C_{CP1} + (N \times Ciss)) \quad (1)$$

So the voltage after turn on will be a ratio of the initial voltage.

$$V2 = V1 \times C_{CP1} / (C_{CP1} + (N \times Ciss)) \quad (2)$$

where

- V1 is the charge pump voltage before switching on the FETs
- V2 is the charge pump and FET gate voltage after switching on the FETs
- C_{CP1} is the charge pump capacitor
- N is the number of FETs switching
- Ciss is the gate capacitance of the FET used

The charge pump will take time to replenish the charge transferred to the gates and bring the voltage back to the regulated CP1 voltage range. Figure 3-5 shows the drop in charge pump voltage turning on 24 CSD19536KCS FETs when using a 470 nF for C_{CP1}. Figure 3-6 shows the smaller drop when turning on the same 24 FETs when using 2 µF for C_{CP1}.

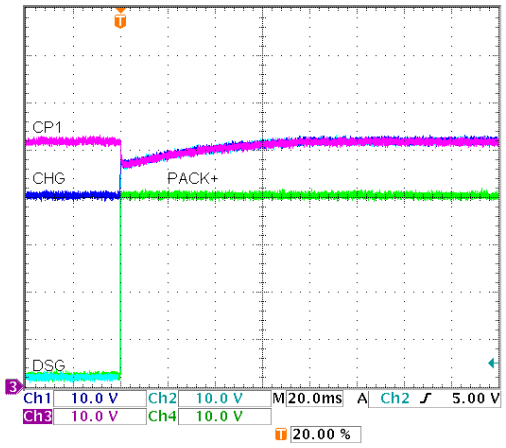

Figure 3-5. CP1 drop, 24 FETs, C_{CP1} 470 nF

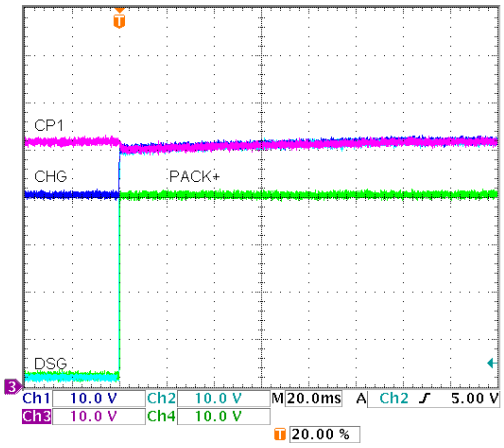

Figure 3-6. CP1 drop, 24 FETs, C_{CP1} 2 µF

4 Parallel FET Test Circuits

When FETs are operated in parallel they can oscillate when switching. A small resistance or ferrite bead is often used in the individual gate path to avoid the oscillation. Figure 4-1 shows a test circuit with multiple FETs. 51-Ω resistors are used in the test circuits of this application report to isolate the individual gates from the common Cgate and Dgate signals. Cgate and Dgate are commonly used in the figures in this document rather than an individual gate voltage unless noted. When a single FET is used the 51-Ω resistor remains. FETs are populated as needed, the remainder of the BQ769x2 schematic remains the same. The CSD19536KCS FETs used in this application note have a typical Ciss of 9.25 nF. R41 and R44 are adjusted for the number of FETs. The reverse charge circuit is retained in the parallel FET test circuits, Q29 is the clamping FET.

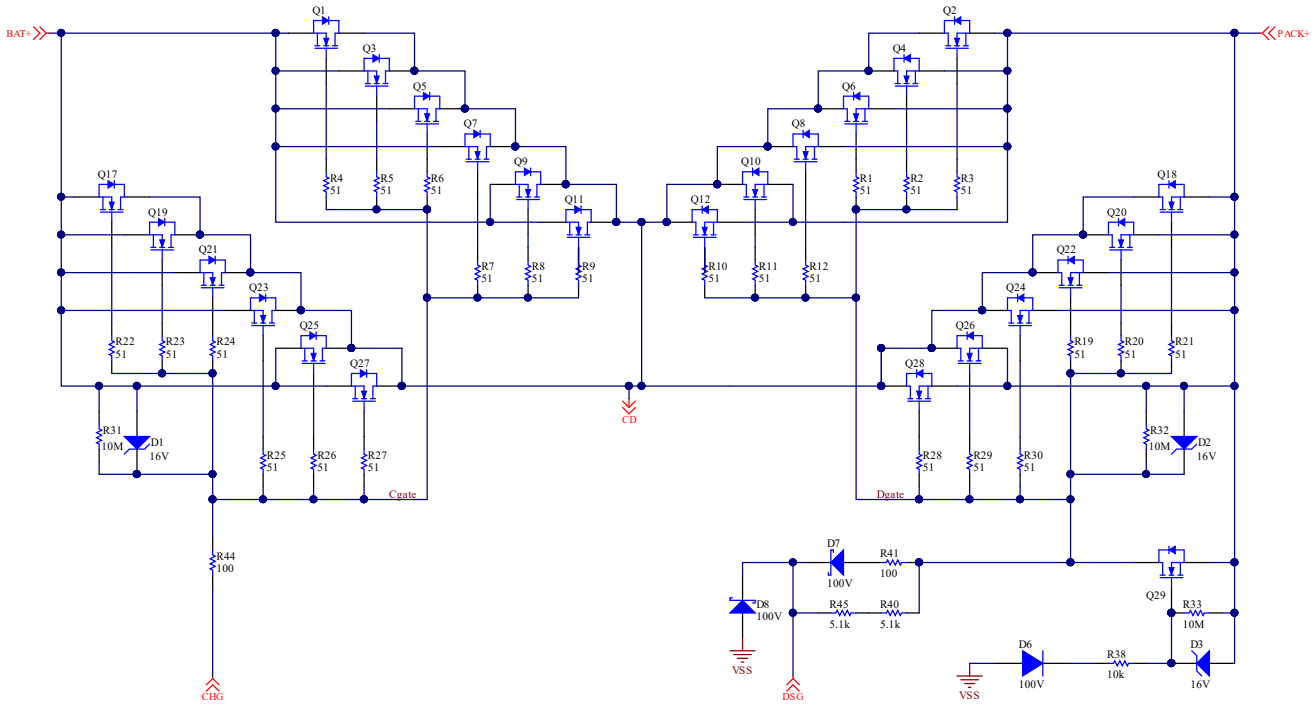

Figure 4-1. Multiple FET Test Circuit

The BQ769x2 has internal driver resistances, so for larger loads, a local turn off circuit may be used. Figure 4-2 shows a circuit where PNP transistors are used to provide a local current loop for turn off of the FETs. The allows turn off with a smaller current loop through the transistor and external resistance. During charge FET turn off CHG draws base current from Q30 through R44 while the collector current discharges the charge FET gates through R35. Similarly DSG draws base current for Q31 through the combination of R40, R45, R41 and D7. The collector current discharges the FET gates through R37. Turn on is still from the charge pump capacitor through D4 for CHG and D5 for DSG. When the diode drop across D4 and D5 is a concern a Schottky type diode could be used or a large value parallel resistor may be added to bring the gates to full voltage after the initial current surge.

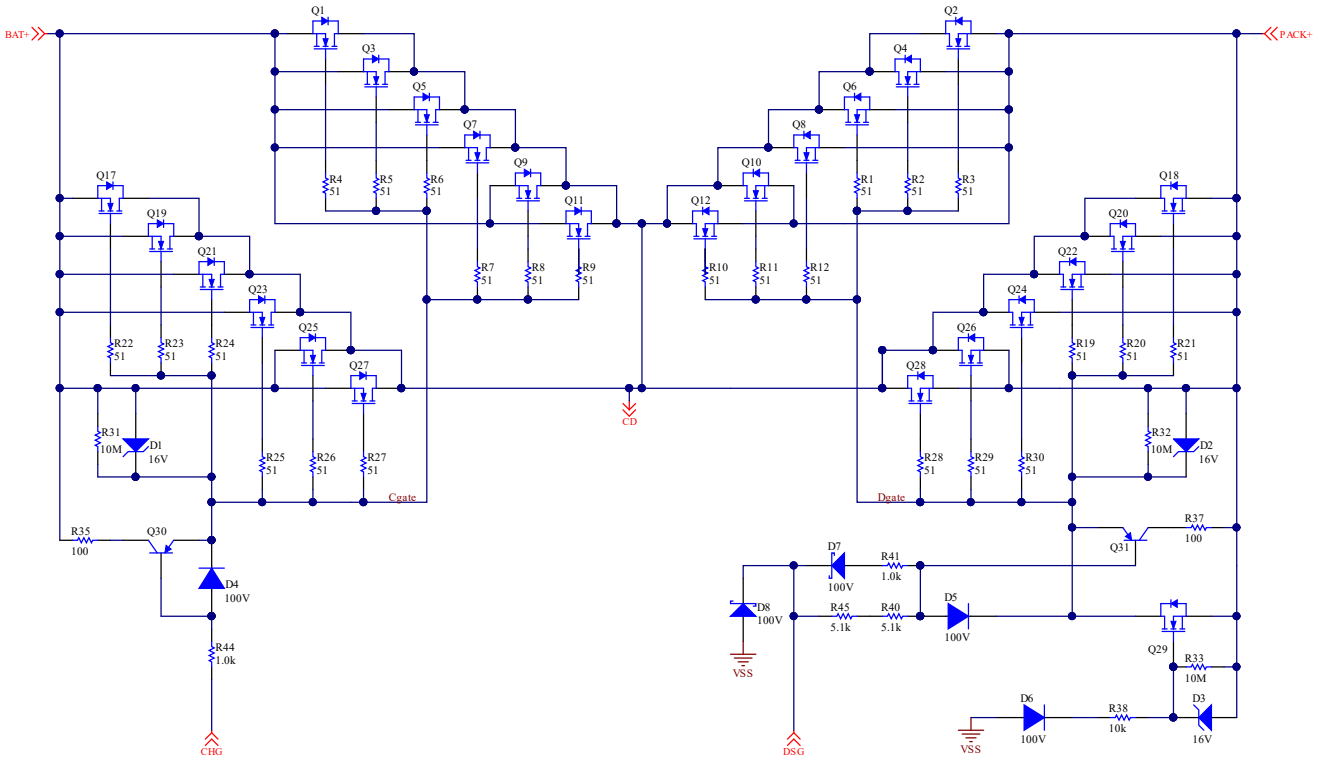

Figure 4-2. Multiple FET Test Circuit With Local Current Loops

5 CHG Driver

The charge driver operates between the BAT pin level and the CP1 voltage. Figure 5-1 to Figure 5-18 show examples for the charge driver switching different FET counts with different circuit connections. In many of the waveforms the current and some voltages show ripple where the connected equipment settled into regulation with the new load. Charge waveform examples are at 20-V and 1-A charge current.

Figure 5-1 to Figure 5-4 show turn on and off of one and 2 FETs with R44 = 5.1 kΩ. The added capacitance of the second gate slows the turn on and off.

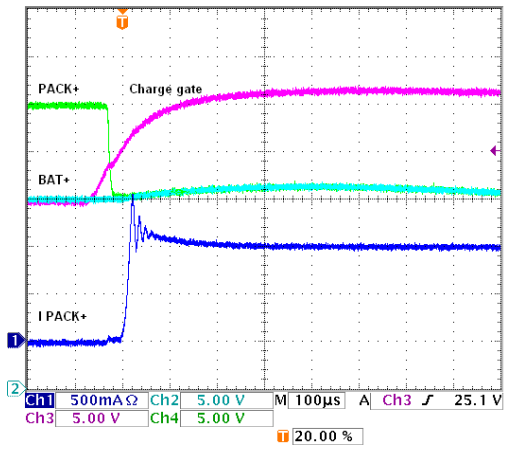

Figure 5-1. CHG On, Single FET, 5.1 kΩ, 470 nF

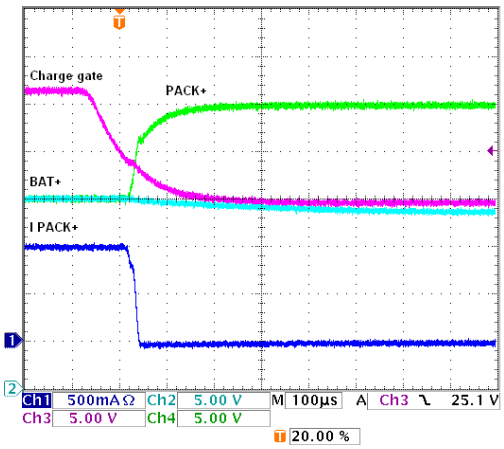

Figure 5-2. CHG Off, Single FET, 5.1 kΩ

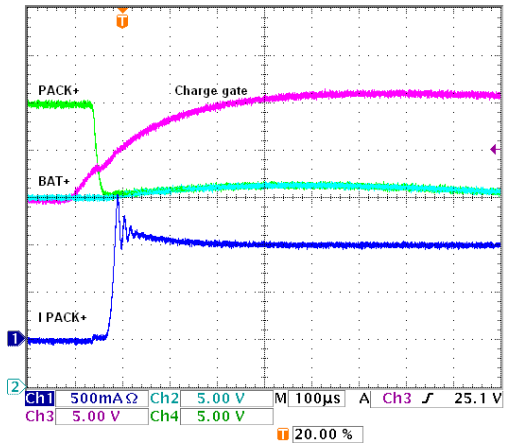

Figure 5-3. CHG On, 2 FETs, 5.1 kΩ, 470 nF

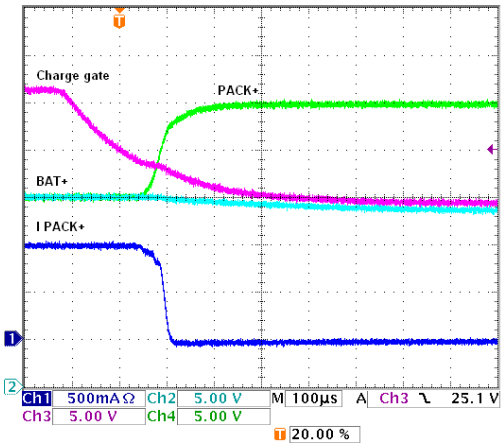

Figure 5-4. CHG Off, 2 FETs, 5.1 kΩ

Figure 5-5 to Figure 5-8 show turn on and off with R44 replaced with 1 kΩ then 100 Ω. The difference between the CHG pin and common charge gate (Cgate) net can be observed. The smaller resistor drives the gate faster and the larger gate load slows the pin transition.

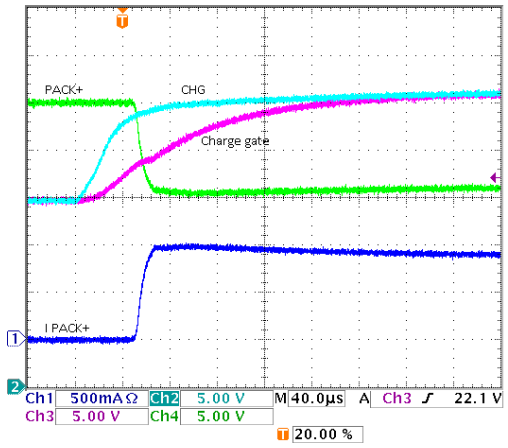

Figure 5-5. CHG On, Single FET, 1 kΩ, 470 nF

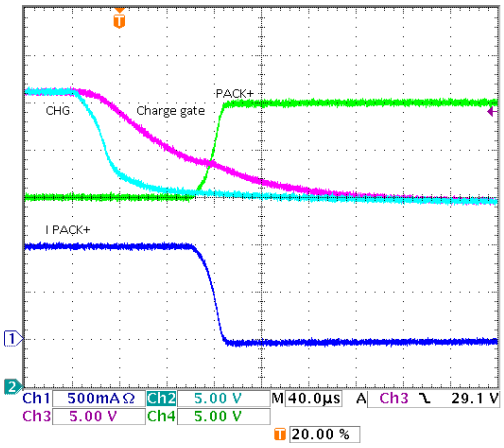

Figure 5-6. CHG Off, Single FET, 1 kΩ

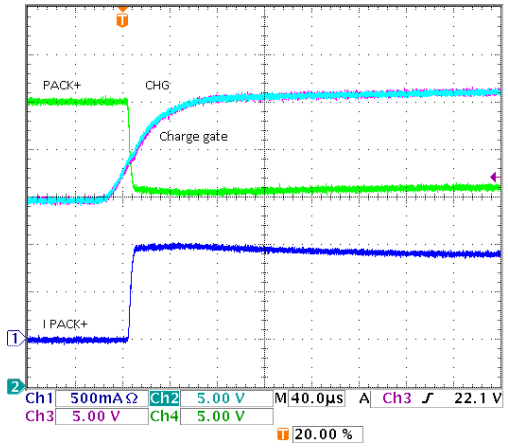

Figure 5-7. CHG On, Single FET, 100 Ω, 470 nF

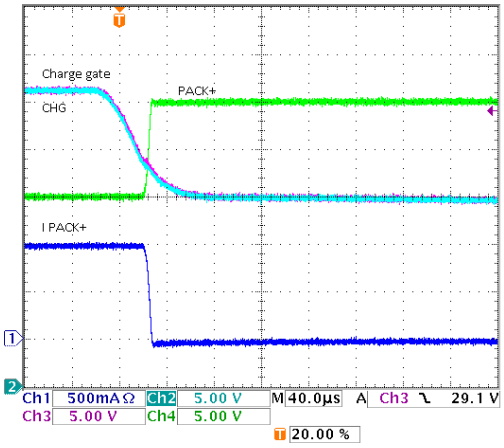

Figure 5-8. CHG Off, Single FET, 100 Ω

With more FETs switching is slowed as the resistance acts on the gate capacitance. Figure 5-9 shows turn off of 4 FETs using R44 at 100 Ω. For faster switching the local current loop created by a PNP transistor controlled by the BQ769x2 CHG pin shown in Figure 4-2 allows the gate to discharge through a lower resistance for a faster transition as shown in Figure 5-10. R44 remains at 100 Ω for this example.

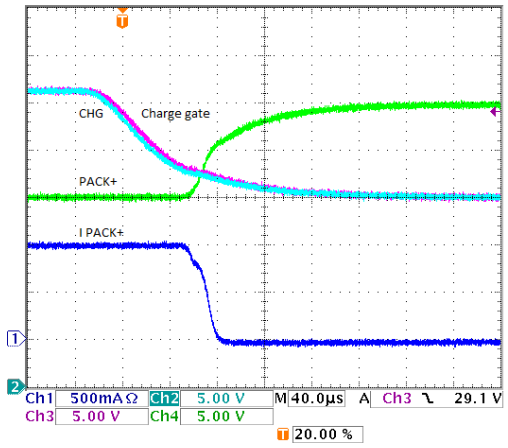

Figure 5-9. CHG Off, 4 FETs, 100 Ω

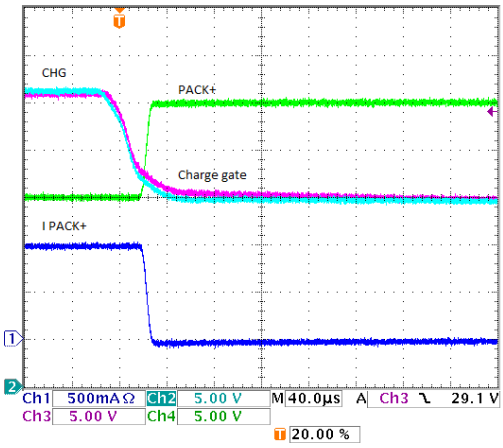

Figure 5-10. CHG Off, 4 FETs, 100 Ω, PNP

Switching 8 FETs with R44 at 100 Ω and without the PNP is shown in Figure 5-11. The slow transition would indicate most of the resistance is internal to the CHG driver. Figure 5-12 shows that even with R44 at 5.1 kΩ the turn off time is must faster as the CHG pin only sinks the base current for the PNP. The 5.1-kΩ R44 does slow turn on as shown in Figure 5-13, using 100-Ω R44 in Figure 5-14 increases turn on speed although the 100 Ω was not needed for turn off.

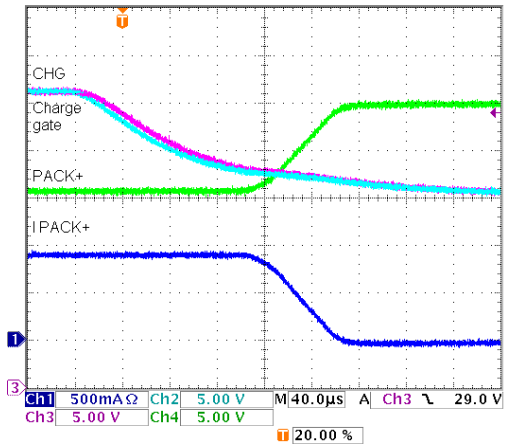

Figure 5-11. CHG Off, 8 FETs, 100 Ω

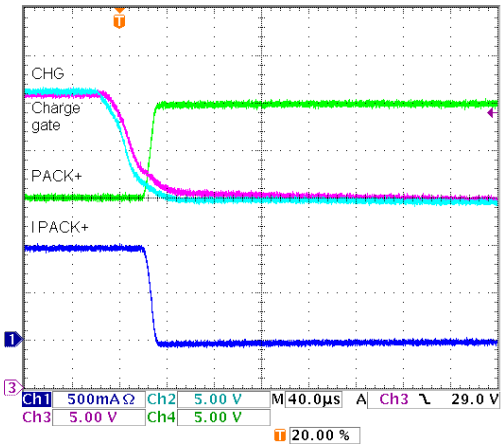

Figure 5-12. CHG Off, 8 FETs, 5.1 kΩ, PNP

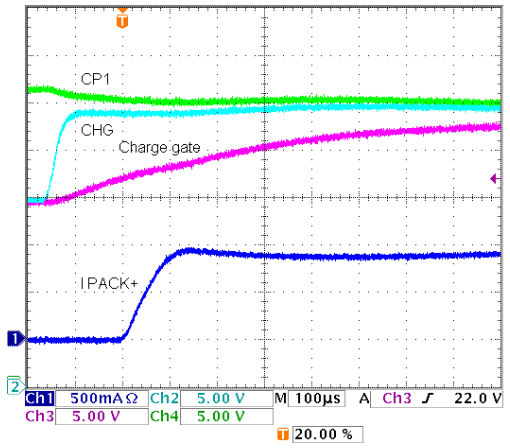

Figure 5-13. CHG On, 8 FETs, 5.1 kΩ, PNP, 470 nF

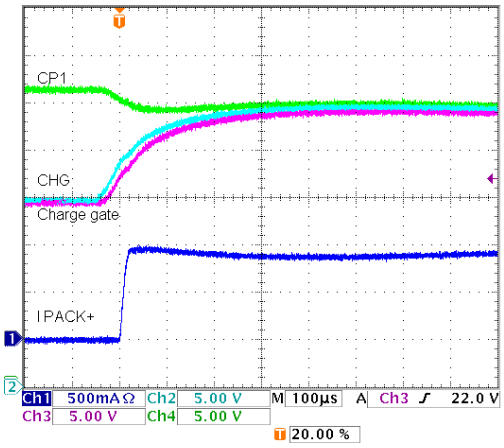

Figure 5-14. CHG Off, 8 FETs, 100 Ω, PNP, 470 nF

In a wider time scale Figure 5-15 and Figure 5-16 show the effect of the charge pump capacitor size on switching 8 FETs.

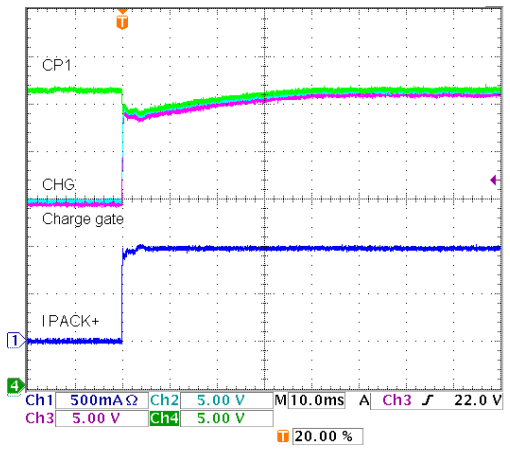

Figure 5-15. CHG On, 8 FETs, 100 Ω, PNP, 470 nF

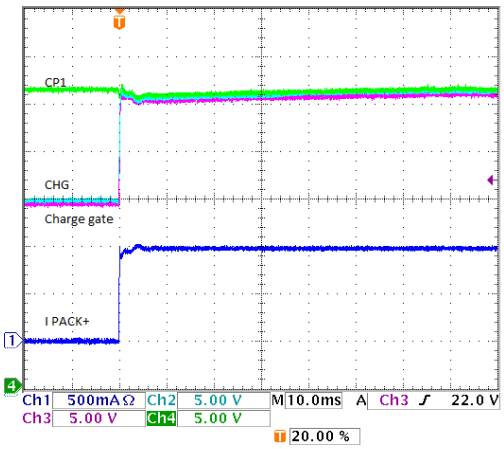

Figure 5-16. CHG On, 8 FETs, 100 Ω, PNP, 2 µF

With 2 µF of CP1 capacitance, Figure 5-17 and Figure 5-18 show turn on and off of 12 FETs with R44 100 Ω and the PNP circuit. Adjusting the turn off speed using the R35 value is not shown in this report.

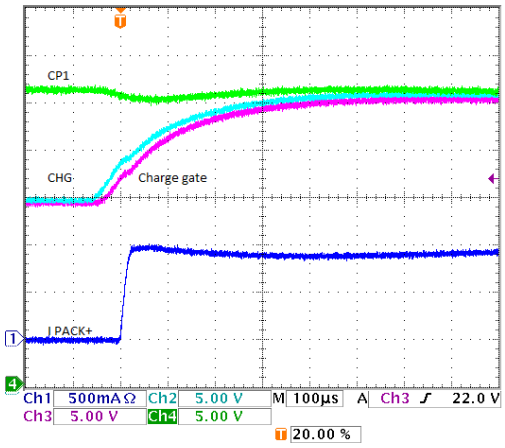

Figure 5-17. CHG On, 12 FETs, 100 Ω, PNP, 2 µF

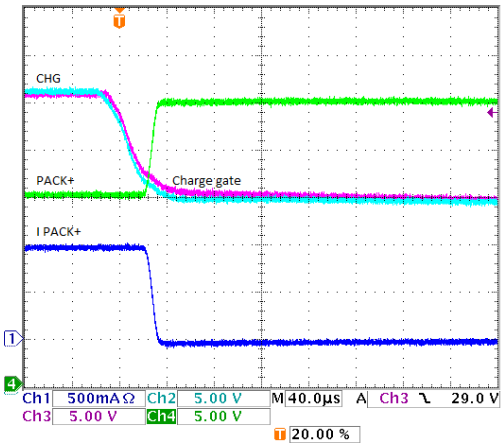

Figure 5-18. CHG Off, 12 FETs, 100 Ω, PNP

6 DSG Driver

The discharge driver operates between PACK- and the CP1 voltage. When the driver turns on, DSG rises toward the CP1 voltage as current flows through R45 and R40 of Figure 4-1. R45 and R40 provide a 10-kΩ turn-on resistance. An example of a single FET turn on is shown in Figure 6-1. As the FET turns on PACK+ rises and current flows in the discharge FET. The gate voltage will lag the DSG voltage with the filter effect of the turn on resistance and the gate capacitance.

When the DSG driver is triggered to turn off, the device will initially begin discharging the DSG pin toward VSS. However, since the PACK+ terminal may not fall to a voltage near VSS quickly, the DSG FET gate should not be driven significantly below PACK+, otherwise the DSG FET may be damaged due to excessive negative gate-source voltage. Thus, the device monitors the voltage on the LD pin (which is connected to PACK+ through an external series resistor) and will stop the discharge when the DSG pin voltage drops below the LD pin voltage. When the discharge has stopped, the pin voltage may relax back above the LD pin voltage, at which point the device will again discharge the DSG pin toward VSS, until the DSG gate voltage again falls below the LD pin voltage. This repeats in a series of pulses which over time discharge the DSG gate to the voltage of the LD pin. This pulsing continues for approximately 200 µs, after which the driver remains in a high impedance state if below the voltage of the LD pin plus approximately 500 mV. The external resistor between the DSG gate and source then discharges the remaining voltage so the FET remains off.

An example turn off is shown in Figure 6-2. DSG pulling low draws current from the gate of the FET through the Schottky diode D7 and R41. Additional current will flow through R40 and R45. Current into the DSG pin is sent to the VSS pin, not out the LD pin. Figure 6-1 and Figure 6-2 show the single FET's gate voltage rather than the common gate net voltage since there is only 1 FET.

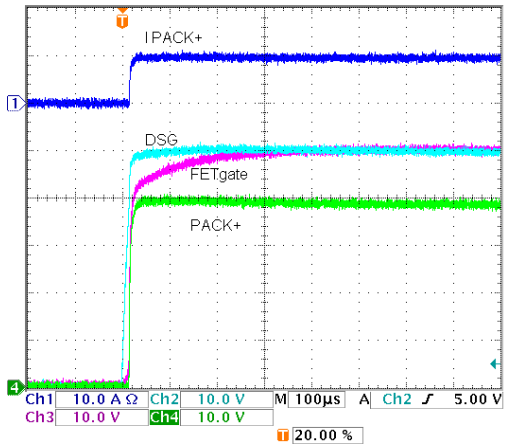

Figure 6-1. DSG On, Single FET, 10 kΩ, 470 nF

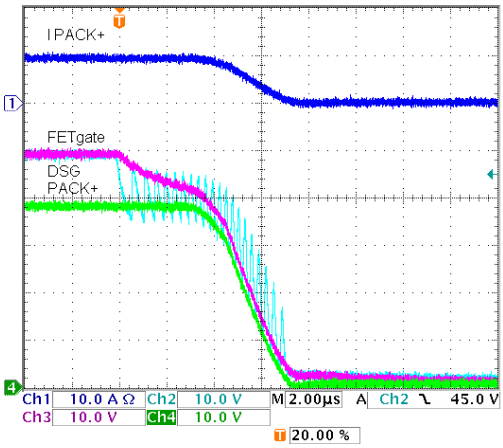

Figure 6-2. DSG Off, Single FET, R41 100 Ω

Inspecting the battery voltage in Figure 6-3 the pulsing acts to avoid a rapid turn off with and the resulting large inductive spike. The designer must select a turn off speed suitable for the battery inductance. With this test current the battery voltage has risen 4 V, a larger R41 value will be used for low FET count comparisons.

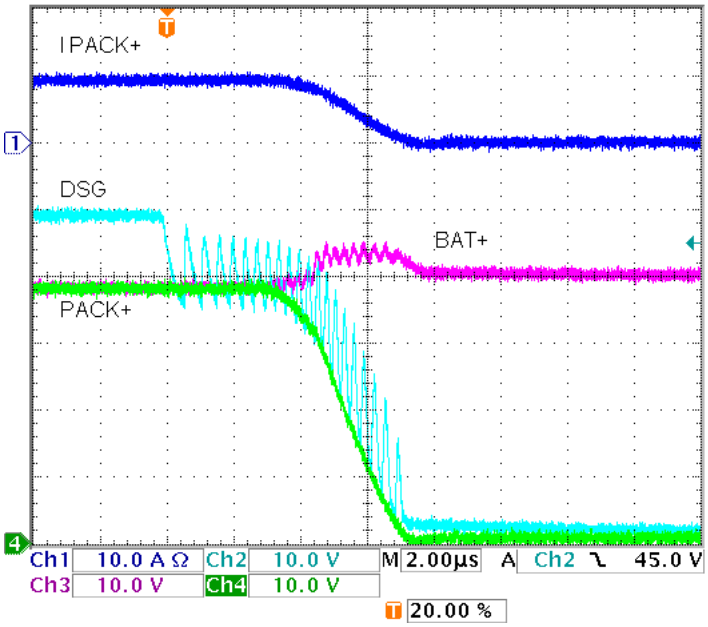

Figure 6-3. Battery Transient With Single FET, R41 100 Ω

Figure 6-4 to Figure 6-9 show example turn on and off with the reverse charge circuit, R41 as 1 kΩ, and 1 to 4 FETs. Turn on for a single FET is similar to the case with R41 100 Ω since the Schottky diode blocks current in R41 during turn on. In Figure 6-4 the common gate net is monitored rather than the single FET gate.

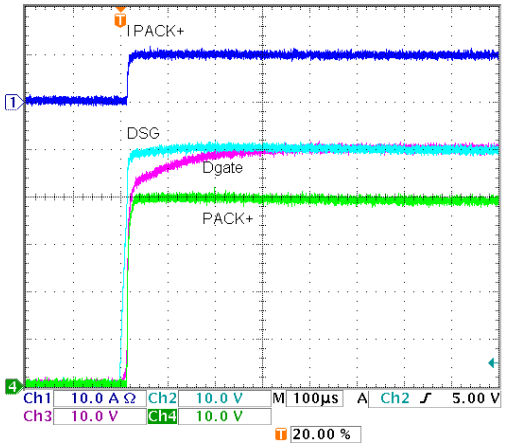

Figure 6-4. DSG On, Single FET, 10 kΩ, 470 nF

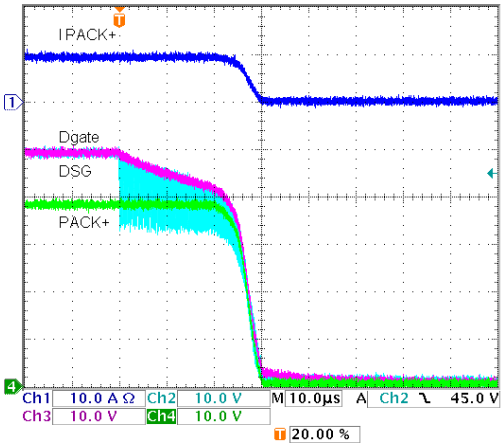

Figure 6-5. DSG Off, Single FET, R41 1 kΩ

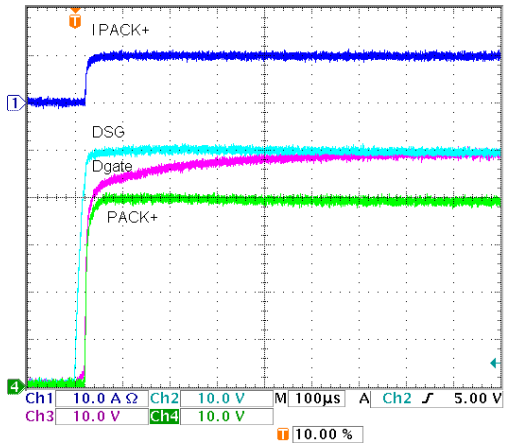

Figure 6-6. DSG On, 2 FETs, 10 kΩ, 470 nF

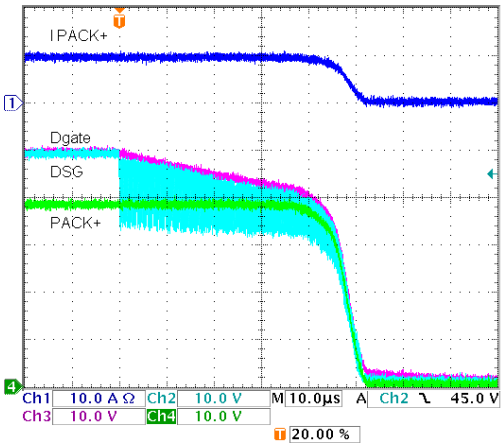

Figure 6-7. DSG Off, 2 FETs, R41 1 kΩ

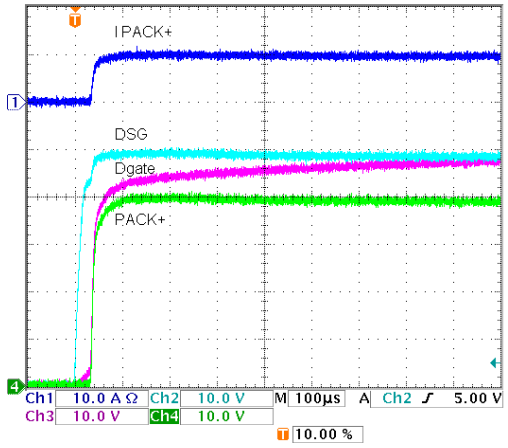

Figure 6-8. DSG On, 4 FETs, 10 kΩ, 470 nF

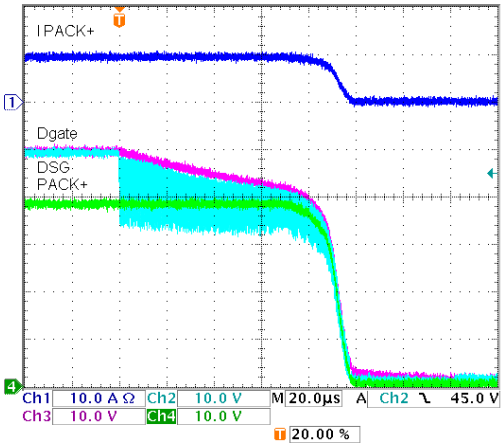

Figure 6-9. DSG Off, 4 FETs, R41 1 kΩ

With 8 FETs gate capacitance has increased the separation of the DSG and Dgate net at turn on and slowed the rise as shown in Figure 6-10. In Figure 6-11 the FETs do not turn off during the pulsing time of the DSG output but later from the weak pull down of DSG. The time to turn off is extended significantly and turn off is slow. This condition should be avoided in a design.

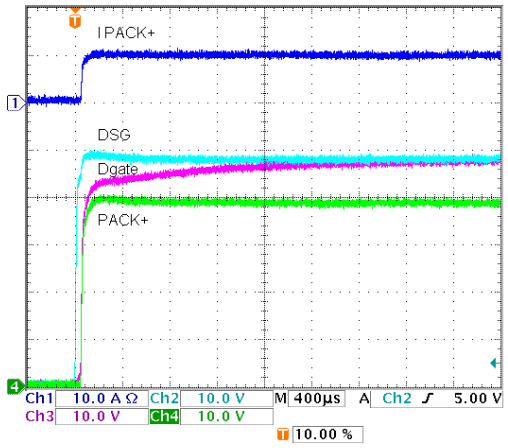

Figure 6-10. DSG On, 8 FETs, 10 kΩ, 470 nF

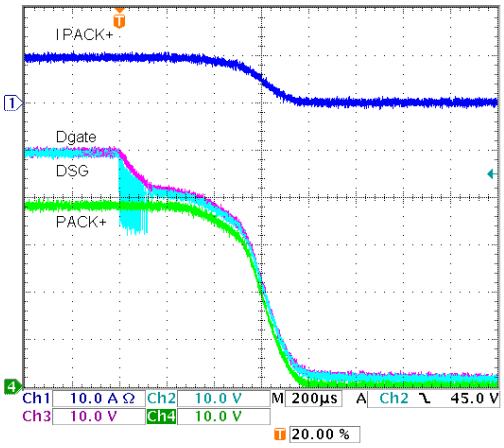

Figure 6-11. DSG Off, 8 FETs, R41 1 kΩ

A smaller pull down resistor for DSG which may have been inappropraite for a smaller number of FETs will increase the turn off time for the larger FET count. In Figure 6-12 and Figure 6-13 R41 is changed back to 100 Ω. Turn on is not changed but turn off is faster. Switching 12 FETs with this configuration is shown in Figure 6-14 and Figure 6-15.

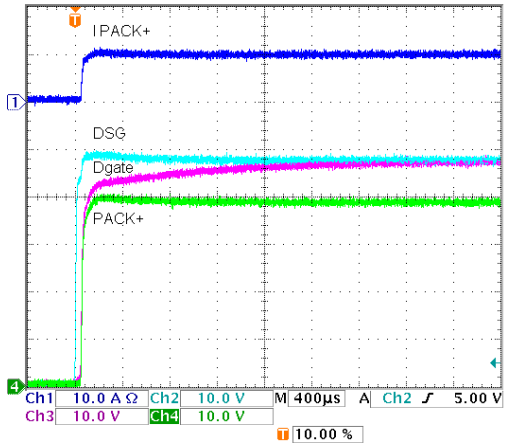

Figure 6-12. DSG On, 8 FETs, 10 kΩ, 470 nF

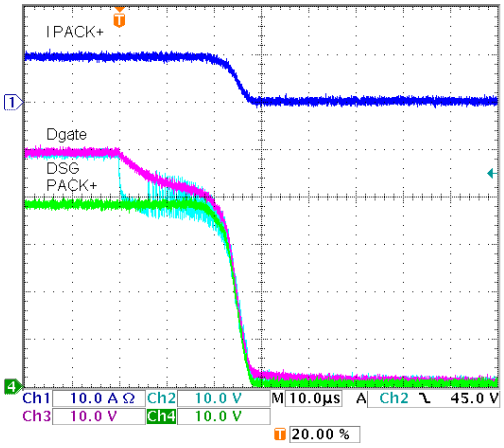

Figure 6-13. DSG Off, 8 FETs, R41 100 Ω

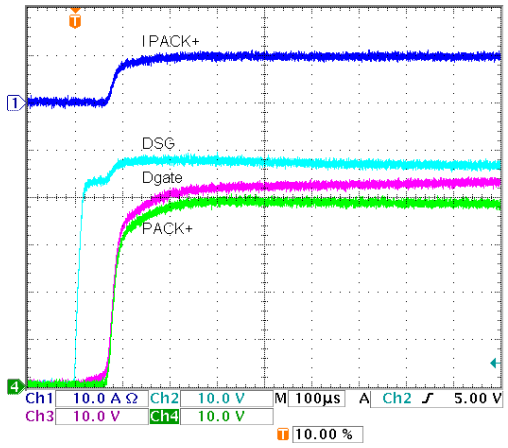

Figure 6-14. DSG On, 12 FETs, 10 kΩ, 470 nF

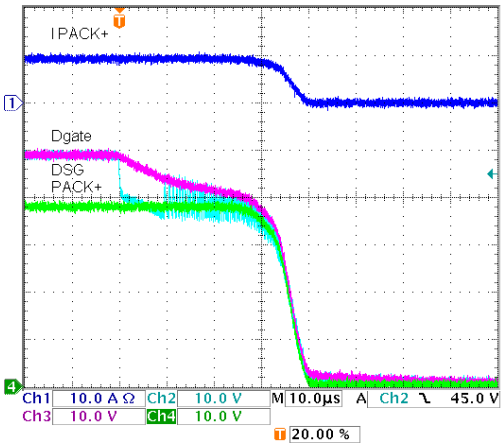

Figure 6-15. DSG Off, 12 FETs, R41 100 Ω

With a given gate pull down resistance, adding FETs increases the capacitance and slows the transition of the DSG pin initial drop due to its internal resistance and the transition of the gate. The effect can be hard to identify with the transition of PACK+. The followng table shows typical values collected for various FET quantities with PACK+ connected to BAT+ using R41 100 Ω. Fall times are 90% to 10%, an example FET gate was measured rather than the Dgate net.

Table 6-1. Fall Times With Various FETs, 100 Ω

Number of FETs	Sum of Ciss, nF	DSG Initial Fall Time, us	Example FET Gate Fall Time, us
1	9.25	0.50	6.4
2	18.5	1.0	9.6
4	37	1.4	16
6	55.5	2.3	21
8	74	5.0	27
10	92.5	6.7	33
12	111	7.2	39

In the above images, the DSG pin discharges the gate capacitance directly. A PNP transistor can be used to discharge the gate capacitance with control by the DSG pin as shown in Figure 4-2. Figure 6-16 and Figure 6-17 show the turn on and turn off with 12 discharge FETs and this circuit.

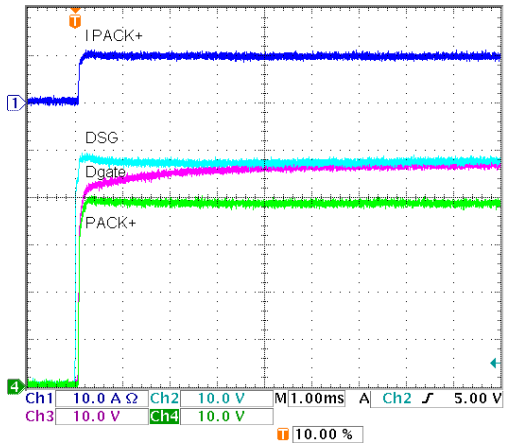

Figure 6-16. DSG On, 12 FETs, 10 kΩ, PNP, 470 nF

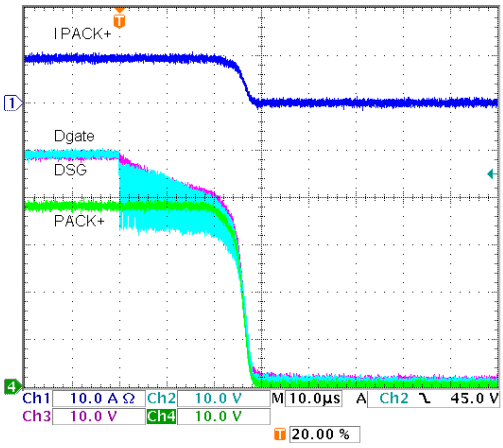

Figure 6-17. DSG Off, 12 FETs, R41 1 kΩ, PNP

The reader has observed that the turn on takes increasing time as the FET count increases. This is because of the 10-kΩ resistance (R40, R45) to keep the power in the resistors at a reasonable level during the reverse charge condition. If the reverse charge circuit is not needed, DSG can be connected to the common gate point with a single resistor replacing the connection network of Figure 4-1. The Schottky diodes, R40 and R45, the reverse charge clamp transistor and related components are omitted. See Figure 6-18. Switching is shown in Figure 6-19 and Figure 6-20.

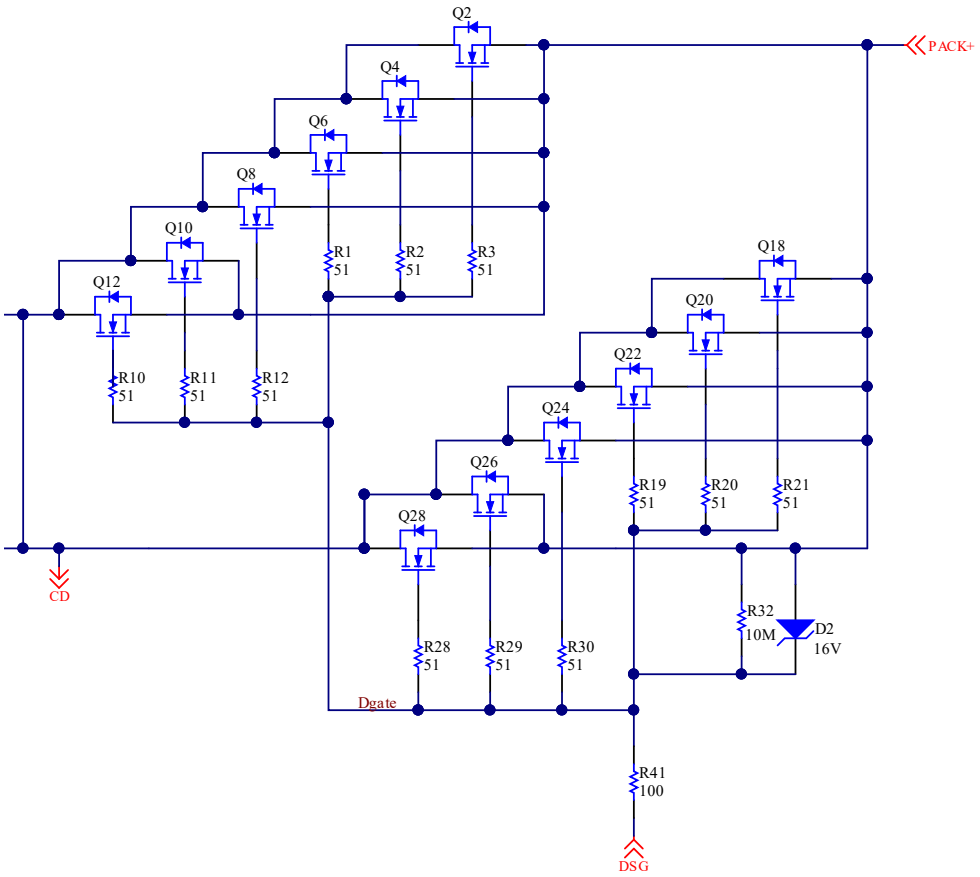

Figure 6-18. DSG Drive Without Reverse Charge Protection Circuit

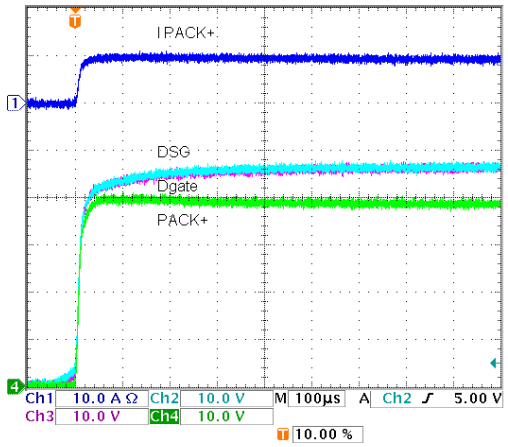

Figure 6-19. DSG On, 12 FETs, 100 Ω, No Reverse Charge Circuit, 470 nF

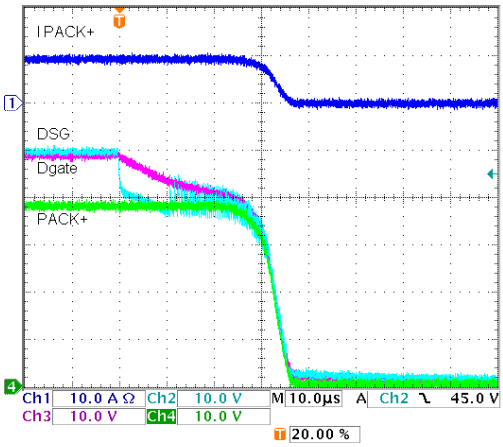

Figure 6-20. DSG Off, 12 FETs, 100 Ω, No Reverse Charge Circuit

If the reverse charge circuit is needed, a P-ch FET may be inserted in place of R45 with the gate referenced to the LD pin as shown in Figure 6-21. The FET will be on when DSG rises, as DSG falls to LD the FET will be on and R40 will help drain the discharge FET gate capacitance, but will turn off allowing the gate pull down resistor R41 to complete turn off. In Figure 6-22 and Figure 6-23 R40 is 1 kΩ. With DSG off the P-ch FET Q32 is off and a reverse charge voltage will drop the Dgate net without current flow in R40. At turn on R40 will act with the gate capacitance and can be adjusted for Dgate to better approach the DSG pin. Remember that the turn on current comes from the CP1 capacitor, the drop in the DSG will depend on the internal resistance and the charge transfer from the CP1 capacitor to the FET gates. This example uses the 470 nF CP1 capacitor and the low voltage after turn on can be observed. At turn off R40 is in parallel with the R41 and Schottky path until voltage is low enough for the P-ch FET to turn off. The user should note that the BQ769x2 does not limit the voltage between DSG and LD at turn on. The intent of the P-ch circuit is to allow using a small R40 so that the FET gates, PACK+ and LD come up quickly with DSG. If a large R40 is used or the discharge FET turn on is slow, a zener on the source-gate connection and large resistor from the Q32 gate to LD connection are desired to protect the Q32 gate.

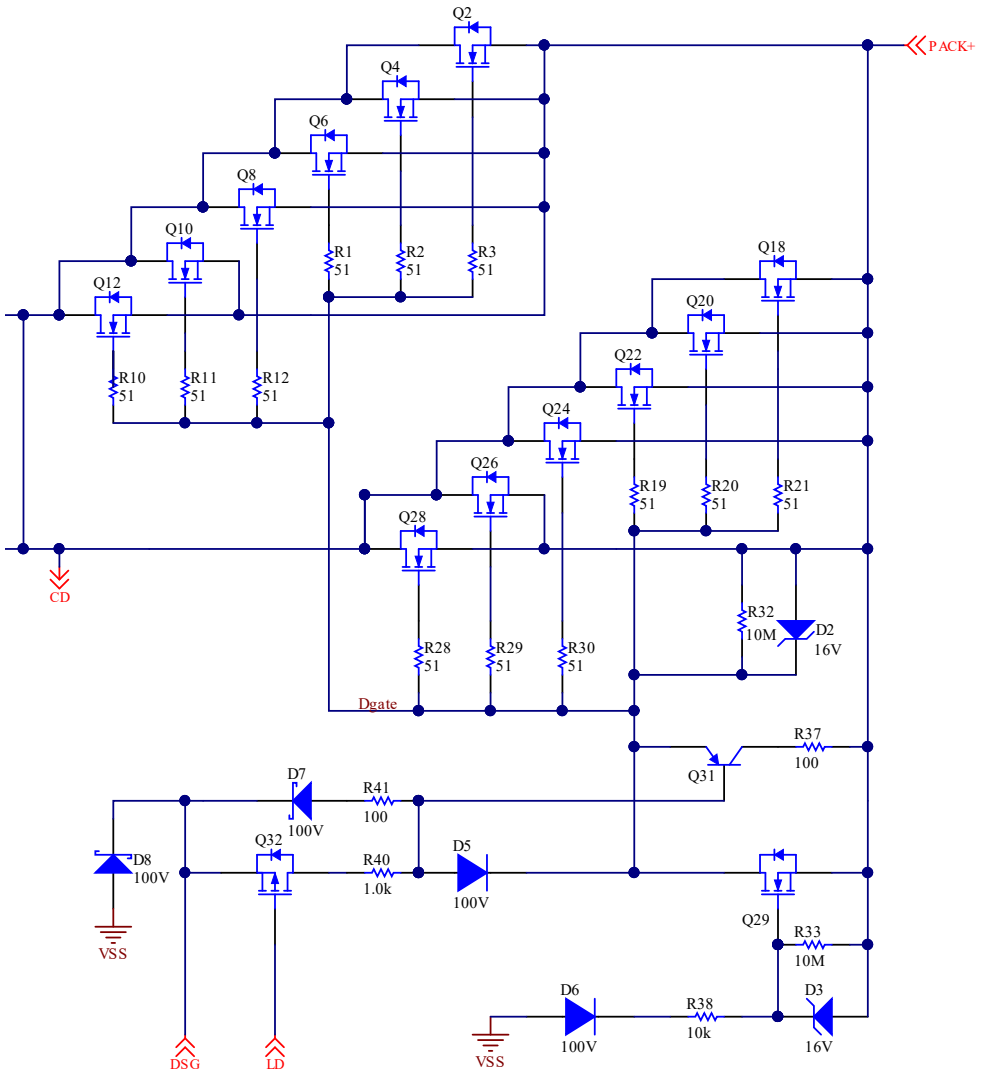

Figure 6-21. P-ch DSG Turn On Circuit

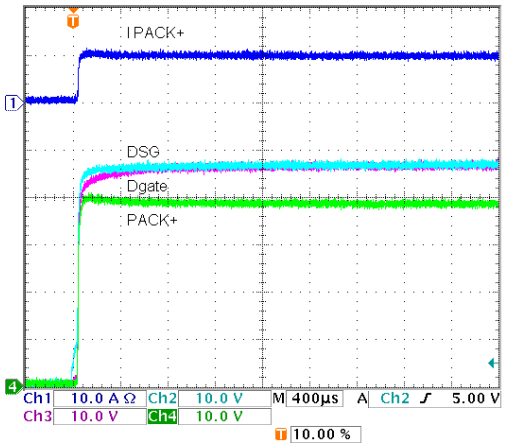

Figure 6-22. DSG On, 12 FETs, P-ch With 1k Turn On Path, 470 nF

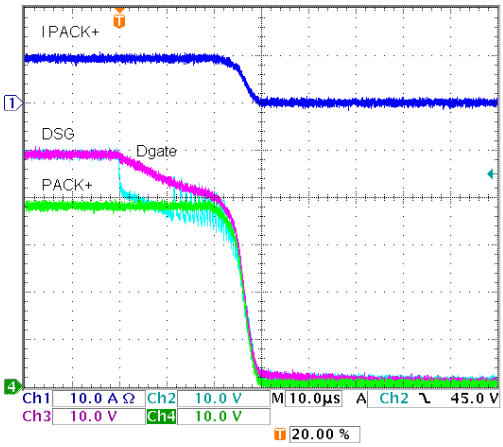

Figure 6-23. DSG Off, 12 FETs, P-ch With 1k Turn On Path, 100 Ω

An example of short circuit is shown in Figure 6-24 using a single FET and several kΩ for R41. When the short circuit is applied BAT+ and PACK+ are held together by the FETs and are pulled down by the load. Discharge of the BAT pin is blocked by the BAT pin capacitor, and the CP1 capacitor holds the charge pump voltage above it as a supply for the CHG and DSG outputs. The gates of the charge and discharge FETs are protected by D1 and D2 in Figure 4-1. CHG and DSG are loaded and drop some due to their internal resistance, but most of the voltage is dropped across the resistors to the gates: R44, R40 and R45. The voltage of DSG will drop as the short circuit event is timed. With longer SCD delays and smaller gate resistors CHG and DSG will drop until D1 and D2 stop conducting. The BQ769x2 times the event using the REG18 supply. When the selected delay is met, DSG is switched off as previously described. R41 turns off the discharge FET and must be selected to turn off the FETs fast enough to avoid excess heating and slow enough to avoid excessive rise of BAT+.

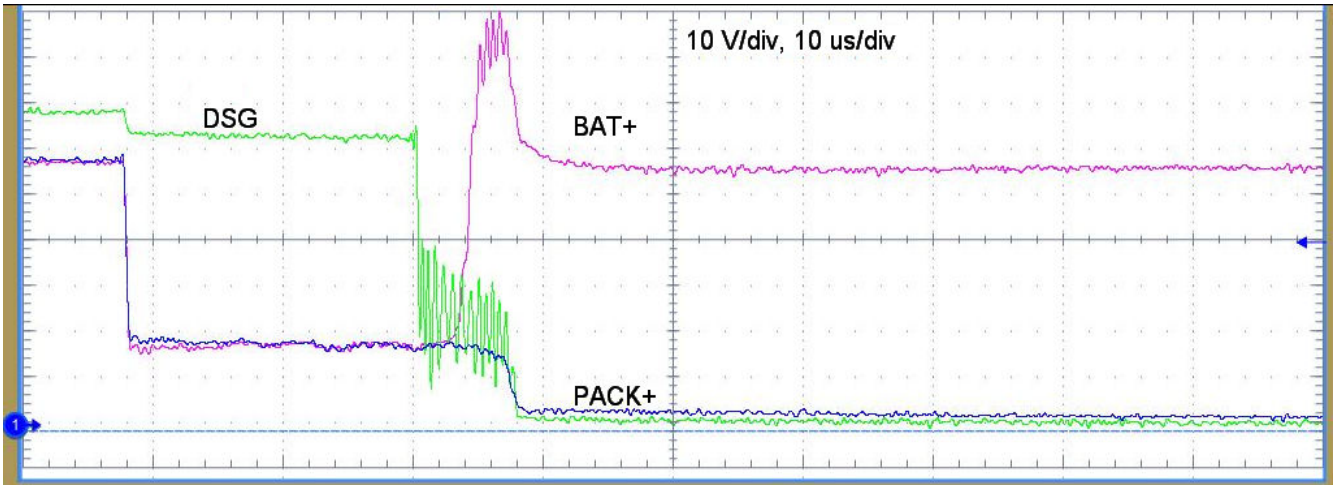

Figure 6-24. Short Circuit Example

7 Conclusion

The BQ76952 family devices provide high-side FET drive and can be used for multiple FET configurations. Size the CP1 capacitor to allow an acceptable droop when FETs turn on. Select resistors in the CHG and DSG pin to gate connections for suitable turn on and turn off of the FETs. When needed, provide accessory turn off or turn on circuits suitable for the application system requirements. The circuits and test results presented in this document will help the designer recognize conditions for consideration in their design. Refer to the data sheets and technical reference manuals for device and configuration information.

8 References

- Texas Instruments, *BQ76952 3S-16S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76942 3S-10S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76952 Technical Reference Manual*
- Texas Instruments, *BQ76942 Technical Reference Manual*
- Texas Instruments, *BQ76952EVM User's Guide*
- Texas Instruments, *BQ76942EVM User's Guide*
- Texas Instruments, *CSD19536KCS 100-V, N-Channel NexFET™ Power MOSFET*

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