National Semiconductor

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Device Marking Conventions

National Semiconductor marks devices sold in order to provide device identification and manufacturing traceablility information. The method of presenting the information marked on the device is dependent on the size of the device package and the area available for marking, as well as the nature and specifications of the device.

The information presented here describes the majority of the device markings a customer will observe. Specific package marking for a given device is given in the datasheet for that device. A package may have up to four lines of marking. The following information is usually contained in each line.

First line: Manufacturing information

- Company logo
- Wafer and/or assembly plant codes (optional) (see *Table 1. Wafer Fab Plant Code* and *Table 2. Assembly Plant Code*)
- Date code (see *Table 3. Year Code*, *Table 4. Six-Week Period Code*, and *Table 5. Date Code Examples*)
- Die run (wafer lot) code

Second Line: Device part number

- Device family (see *Table 6. Device Family*)
- Device type
- Options
- Package code (see *Table 7. Package Type*)

Third or fourth line: Optional, depending on device, package size, and customer

- Continuation of device identification (if too long for the second line)
- "Stampoff" number as required by specific customer request and specification
- Notice(s) related to copyright or trademarks

Very small packages, such as SOT-23, SOT-223, SC70, and SC90, are too small to contain all the information discussed above. Device identification marking is assigned differently, consisting of a four-character code:

- Device type (see *Table 9. Device Type Code*)
- Device identification code
- Grade

These small packages also have a date code mark on the underside of the package. This is a one-character alpha code that represents a particular 6-week period during a 3-year span.

The specific marking for a given device can be found in the device datasheet. Other date code information, which would be typically found in the "first line" marking, is identified on the container labels.

Figure 1, *Figure 2*, and *Figure 3* show the typical arrangement of marking on large, medium, and very small packages. Codes that are most often used in the device marking are listed in the following tables. For chip scale packaged devices and all other recent updates, please refer to www.national.com/packaging.

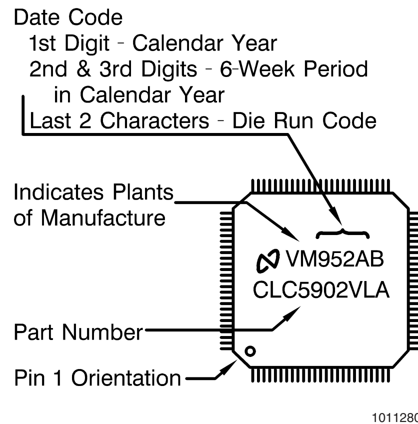

FIGURE 1. Marking Convention for Larger Packages

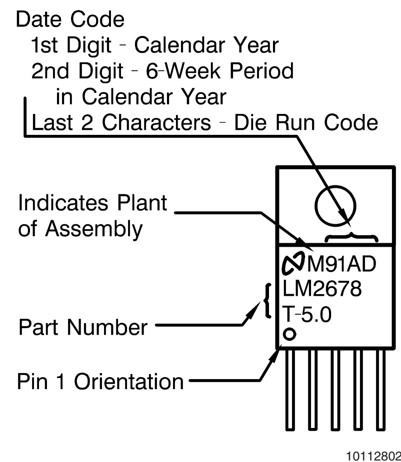

FIGURE 2. Marking Convention for Smaller Packages

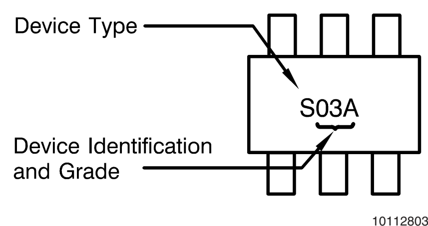

FIGURE 3. Marking Convention for Very Small Packages

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Wafer Fab and Assembly Plant Codes

Table 1. Wafer Fab Plant Code lists single-letter codes for National Semiconductor's wafer fabrication plants. Letters that are not in this list indicate wafer fabrication at one of National Semiconductor's approved sub-contractors.

TABLE 1. Wafer Fab Plant Code

Code	Fab Location
E	Arlington, TX
H	Greenock, UK
J	Greenock, UK
R	Santa Clara, CA
V	South Portland, ME
X	Arlington, TX
0	Multiple Fab Origin
1	USA (Sub-con)
2	Taiwan (Sub-con)
3	USA (Sub-con)
8	Singapore (Sub-con)
M	USA (Sub-con)
N	Israel (Sub-con)
P	China (Sub-con)
W	Japan (Sub-con)
Z	USA (Sub-con)

Table 2. Assembly Plant Code lists single-letter codes for National Semiconductor's device assembly plants. Letters that are not in this list indicate device assembly at another of National Semiconductor's approved sub-contractors.

TABLE 2. Assembly Plant Code

Code	Assembly Location
F	Santa Clara, CA
M	Malacca, Malaysia
S	Singapore
B	Thailand (Sub-con)
D	Philippines (Sub-con)
E	Korea (Sub-con)
G	Canada (Sub-con)
H	Philippines (Sub-con)
I	Indonesia (Sub-con)
J	Japan (Sub-con)
K	Hong Kong (Sub-con)
N	Malaysia (Sub-con)
P	Malaysia (Sub-con)
T	Taiwan (Sub-con)
V	Malaysia (Sub-con)
X	USA (Sub-con)
Y	Malaysia (Sub-con)

Date of Manufacture Codes

Marks indicating the date of manufacture occur in four, three, two, or one digit versions. The date code represents a six-week period in which the device was assembled. The one-digit code is an alpha code for the very small packages, such as SOT, SC70, and SC90, and ranges from A to Z plus the character @, representing a 6-week period during a 3-year span. For the four, three, and two digit codes, the allocation of digits between year and week information in each scheme is summarized in *Table 3. Year Code*:

TABLE 3. Year Code

Version	Year Digits	Week Range Digits
Four-digit (YYWW)	2	2
Three-digit (YWW)	1	2
Two-digit (YW)	1	1

Year: The year code is the last one or two digits of the calendar year of manufacture. For example, a device manufactured in 1999 would have a one-digit code of "9" or a two-digit code of "99".

Week: The week code is based on the starting calendar week of the six-week period during which the device was assembled. *Table 4. Six-Week Period Code* summarizes the six-week date code schedule for one- and two-digit codes.

TABLE 4. Six-Week Period Code

Six-Week Period		Two-Digit Code	One-Digit Code
From Week	To Week		
52	05	52	9
06	11	06	1
12	17	12	2
18	23	18	3
24	29	24	4
30	35	30	5
36	41	36	6
42	47	42	7
48	51	48	8

Some example date codes are shown in *Table 5. Date Code Examples*:

TABLE 5. Date Code Examples

Date of Manufacture	4-Digit Code	3-Digit Code	2-Digit Code
Calendar week 48, 1999	9948	948	98
Calendar week 6, 2000	0006	006	01
Calendar week 14, 2000	0012	012	02
Calendar week 32, 2001	0130	130	15

Die Run (Wafer Lot) Codes

The die run code is a two letter alpha code, ranging from AB through ZZ for each device, that is automatically assigned to each lot by an internal manufacturing system. When the date code is combined with the die run code, a unique identifier is created. In case of any problems with a device, this identification facilitates backward traceability to manufacturing processes where containment and corrective actions can be defined. These actions, in turn, minimize, and eventually eliminate, any negative impact on customers.

Device Family and Package Codes

TABLE 6. Device Family

ADC, ADCV	Data Conversion
CLC	Comlinear Products
COP	Control Oriented Processor
DAC	Data Conversion
DS, DSV	Interface Products
FPD	Flat Panel Devices
LF	Linear (Bi-FET™)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LMF, MF	Linear Monolithic Filter
LMH	Linear Monolithic High Speed
LMS	Linear Second Source
LMV	Linear Low Voltage
LMX	Wireless
LP	Linear Low Power
LPC	Linear CMOS (Low Power)
LPV	Linear Low Power, Low Voltage
SC	Digital Cordless Telephony
SCAN	JTAG Products
TP	Telecom Products

TABLE 7. Package Type

BP	Micro Surface-Mount Device (MicroSMD)
D, DA, DH	Ceramic Sidebrazed Dual-In-Line Package
DT, TD	Molded D-Pak (TO-252)
EA, E	Ceramic Leaded Chip Carrier (LCC)
EL	Ceramic Quad Flatpack (CQFP, CQJB)
H, HA	3-Lead Metal Can (TO-46,TO-39)
J, JA	Ceramic Dual-In-Line Package (CerDIP)
K, KA, KC, KS	TO-3 Metal Can (Steel)
LD, LQ, LQA	Leadless Leadframe Package (LLP)
M, MA	Molded Small Outline Package (SO, SOT)
M3, M5, M6, MF	Molded Small Outline Package (SOT-23)
M7, MG	SC70
MB, MBH, MBS, MDA, MDB	Thin Small Outline Package (TSOP)
MC	Ceramic Small Outline Package (CSOP)
MEA, MEB, MEC, MED, MQ, MQA, MS, MSA, MSC	Molded Shrink Small Outline Package (SSOP)
MH, MXP	TSSOP with exposed pad
MJ	Molded surface mount with J-bend (SOJ)
MM	Miniature Molded Small Outline Package (MSOP, Mini SO)
MP	Molded Small Outline Package (SOT-223)
MTB, MTC, MTD, MTE	Molded Thin Shrink Small Outline Package (TSSOP)
MW, WM	Wide Body Molded Small Outline Package (SO, SOT)
MWA	Power Small Outline Package (PSOP)
N, NA	Molded Dual-In-Line Package (DIP)
P, PA, TB	Molded TO-202 Power Package
S, TS	Molded Power Surface Mount Package (TO-263)
SL, SLB	Chip Scale Packaging (CSP) Laminate
SM, SLC	Ball Grid Array (BGA)
T, TA	Molded TO-220 Power Package
TF	Molded TO-220 Power Package With Isolated Tab
U, UA, UC	Ball Grid Array (BGA)
U, UE	Ceramic Pin Grid Array (CPGA)
UP	Plastic Pin Grid Array (PPGA)
V, VA	28 & 44-Lead Molded Plastic Leaded Chip Carrier (PLCC)
V, VV, VW, VY	Leaded Quad Flat Pack (LQFP)
VC, VD, VE, VF, VH, VI, VJ, VK, VM, VN, VO, VP	Molded Plastic Quad Flat Package (PQFP)
VS, VT, VU	Molded Plastic Thin Quad Flat Package (TQFP)
W, WA	Ceramic Flatpack
W, WQ	Ceramic Quad Flatpak
WG	Ceramic Small Outline Package and Quad Flatpak with Gullwing Lead Form
YA	TQFP with exposed pad
Z, ZA,R	Molded 3-Lead Transistor Package (TO-92)

Device Family and Package Codes
(Continued)

TABLE 8. Package Type — CLC Products

E	Molded Small Outline Package (SO, SOT)
Q	Molded Plastic Leaded Chip Carrier (PLCC)

Small Surface-Mount Package Marking

For packages such as SOT23 (3-, 5-, and 6-lead), SOT223, and MSOP, there is insufficient space to mark the entire part number, so a four-character code is used instead. The first character represents the device type (see *Table 9. Device Type Code*). The second two characters are a code relating to the device part number and options. The fourth character relates to device performance grade. This four-character “top mark” is usually fully specified in the device datasheet, for all options and grades of the product.

TABLE 9. Device Type Code

A	Amplifier
B	Buffer
C	Comparator
D	Driver
H	Comlinear
L	Low-Dropout Linear Regulator
R	Voltage Reference
S	Switched-Capacitor Voltage Converter
T	Temperature Sensor
Z	Audio

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