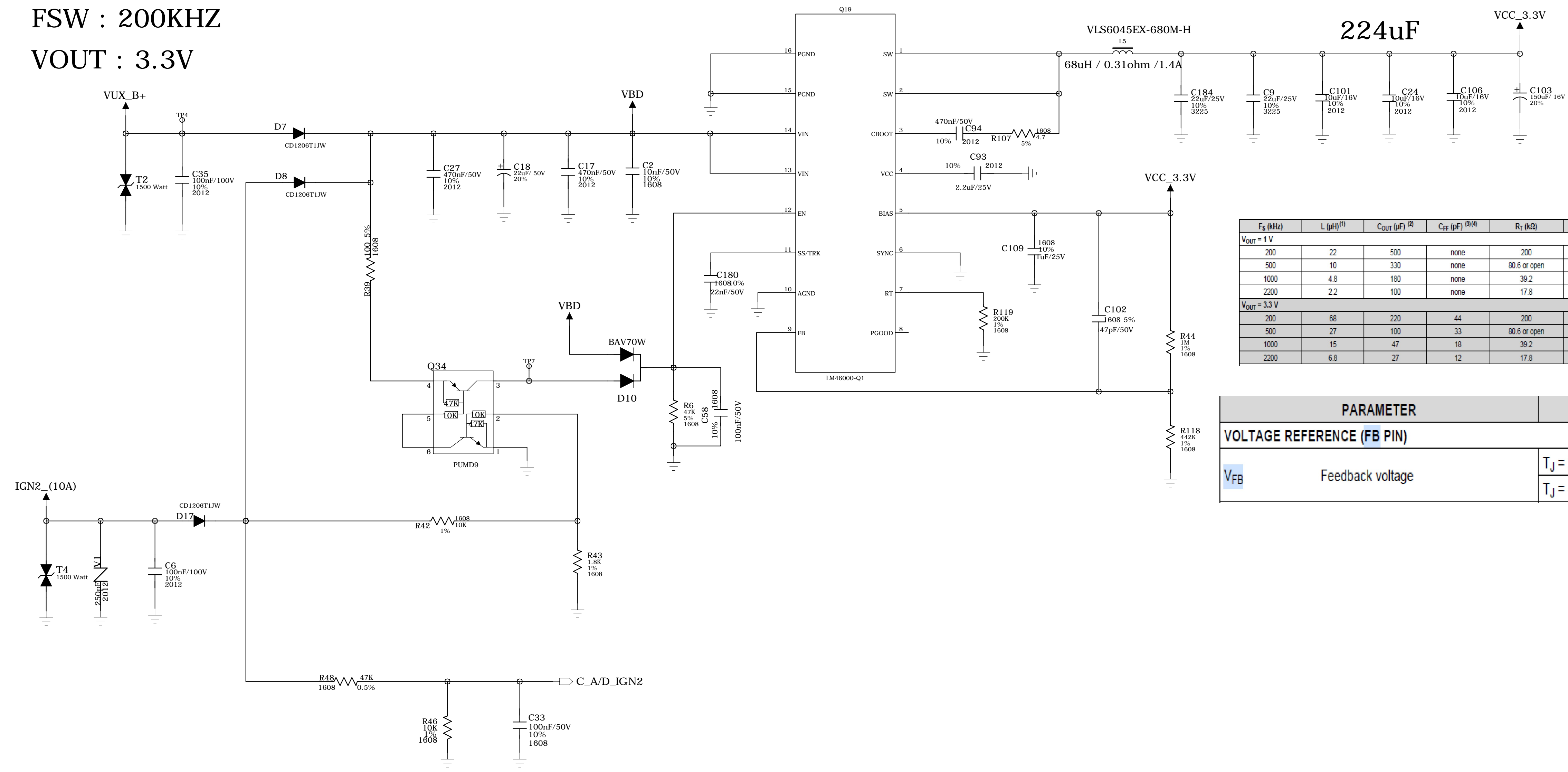


VIN 8~ 16V
 FSW : 200KHZ
 VOUT : 3.3V

REVISION RECORD			
ITR	ECD NO.	APPROVED	DATE



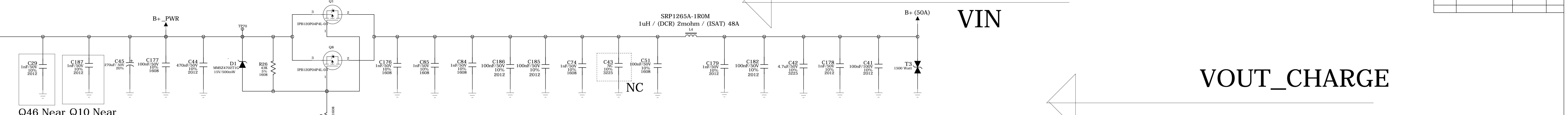
Fs (kHz)	L (μH) ¹⁾	Cout (μF) ²⁾	Cin (μF) ³⁾	Rz (mΩ)	Rzmin (mΩ)
Vout = 1 V					
200	22	500	none	200	100
500	10	100	none	50.6 of open	100
1000	4.8	100	none	39.2	100
2200	2.2	100	none	17.8	100
Vout = 3.3 V					
200	68	220	44	200	442
500	27	100	33	50.6 of open	442
1000	15	47	15	39.2	442
2200	6.8	27	12	17.8	442

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE (FB PIN)					
V _{FB}	Feedback voltage				V
		T _J = 25°C	1.009	1.016	
		T _J = -40°C to 125°C	0.999	1.016	1.039

DRAWN: JH CHO		DATED: 18.02.28		COMPANY:	
CHECKED: JH CHO		DATED: 12.06.18		TITLE: BMS	
QUALITY CONTROL: <QC By>		DATE: <QC Date>		CODE: < Code >	SIZE: E
RELEASED: <Released By>		DATE: <Release Date>		DRAWING NO. REVISION 2.00	
DRAWN: <Scale>				SHEET 1 OF 3	

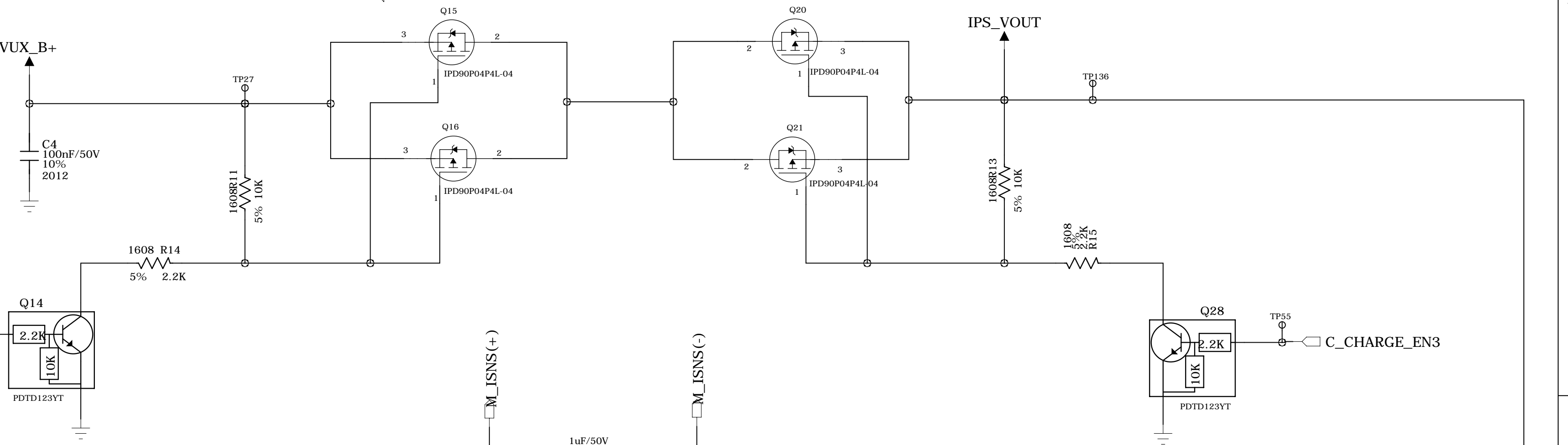
REVISION RECORD			
ITR	ECO NO.	APPROVED	DATE

ID (FET) = Square ((175-75) / (4.4mohm * 40)) = 23.8A (23.8*2 = 47.6A)

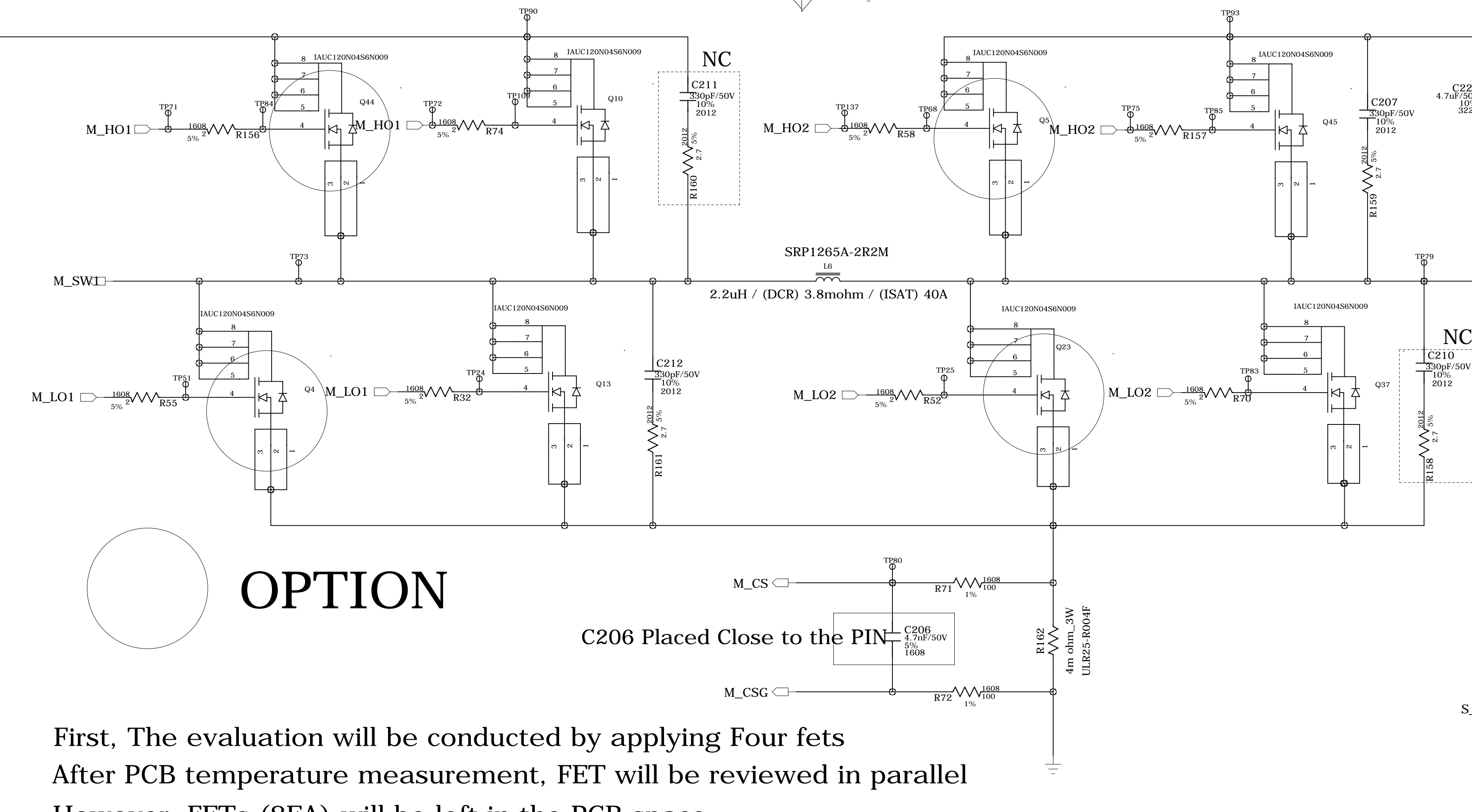


- Q46 Near Q10 Near
- ∅ VIN : 8~ 16V (Charging starts from 10V)
- ∅ FSW : 300KHZ (Master / Slave)
- ∅ 2Phase Max Charging Current Limit 33A : 16.5A Per 1Phase
- ∅ Charging Voltage : 12.6V
- ∅ LM5176 2EA Applications : Master 1EA / Slave 1EA
- ∅ CC (Constant Current) Variable Control
- ∅ NC : (NOT Connect) Debugging point

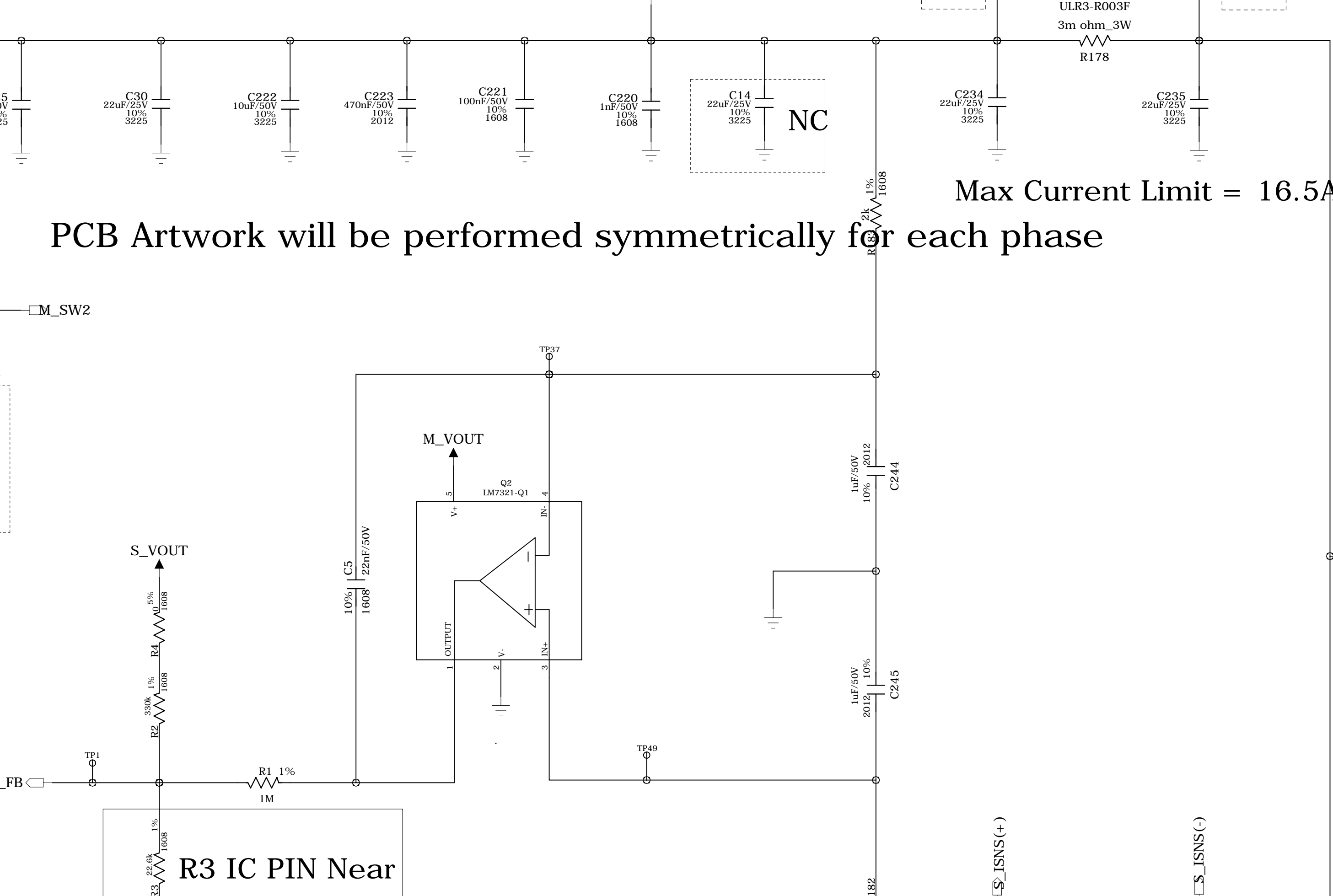
I (INPUT A) = 12.6V * 33A / (10V*0.9) = 46.2A



Master Control_ 12.6V / 16.5A



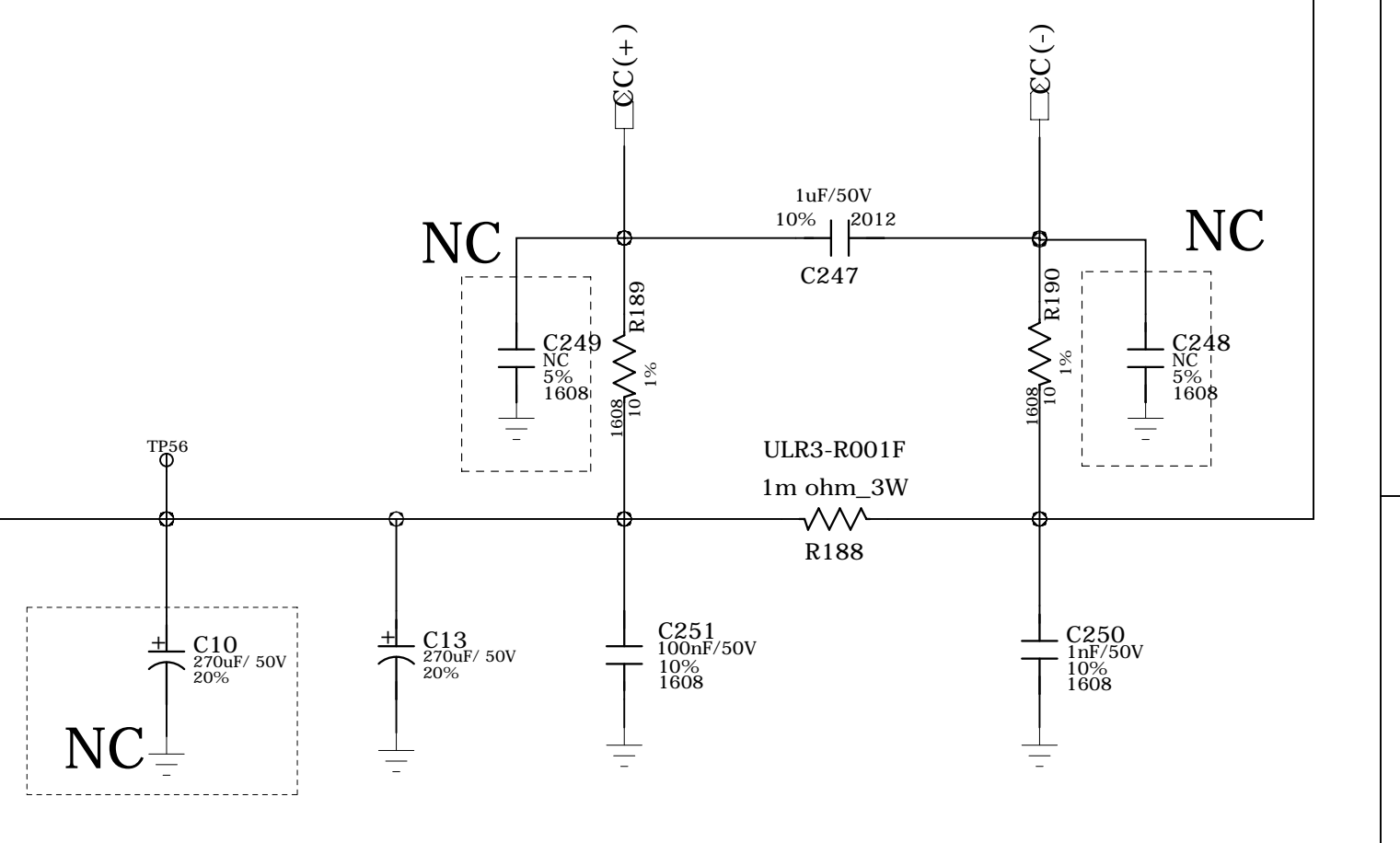
Master Load_ 12.6V / 16.5A (20A Pattern width)



Max Current Limit = 16.5A

PCB Artwork will be performed symmetrically for each phase

CC (Constant Current Variable Control)

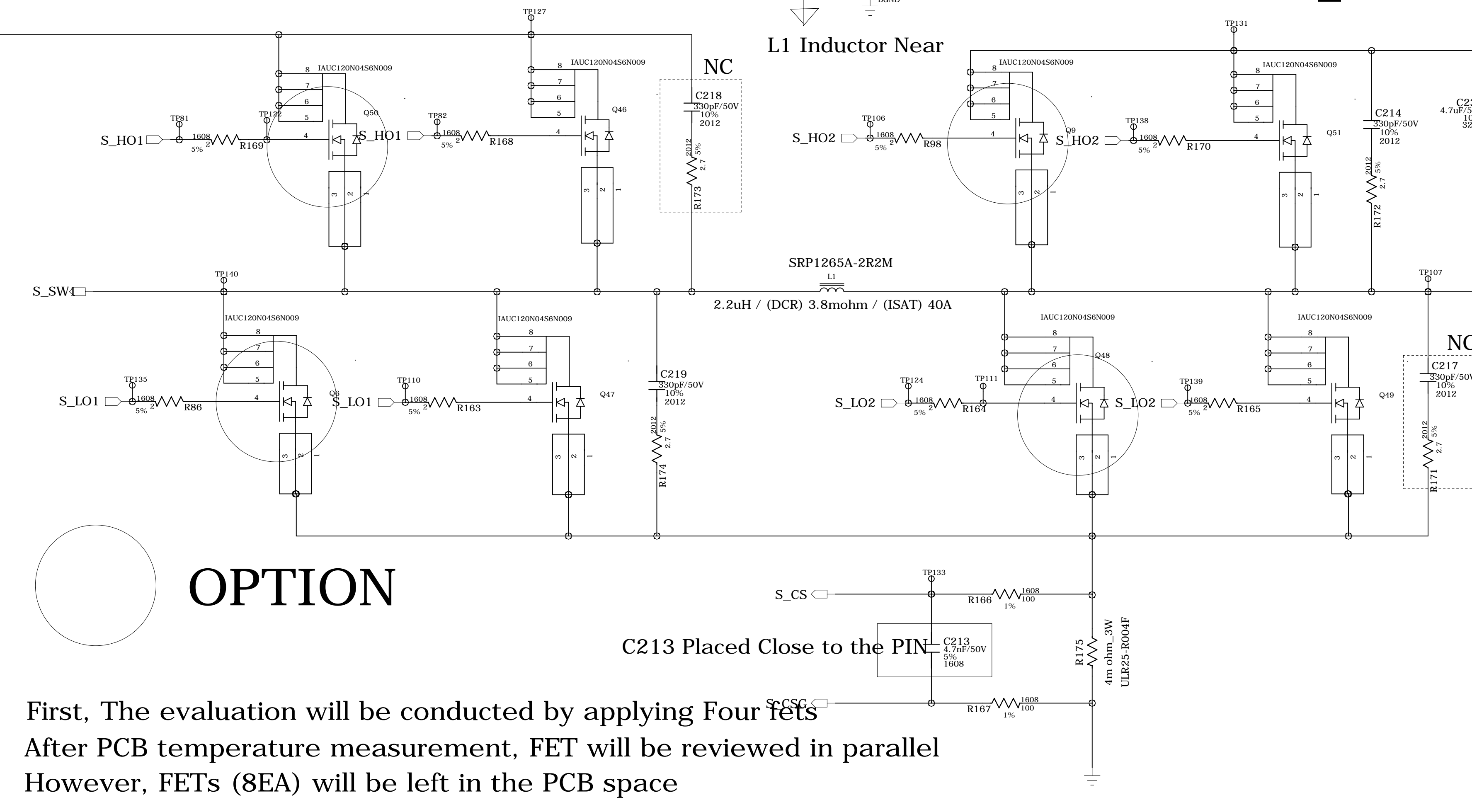


Total Current Limit 33A (12.6V) : 35A Pattern width

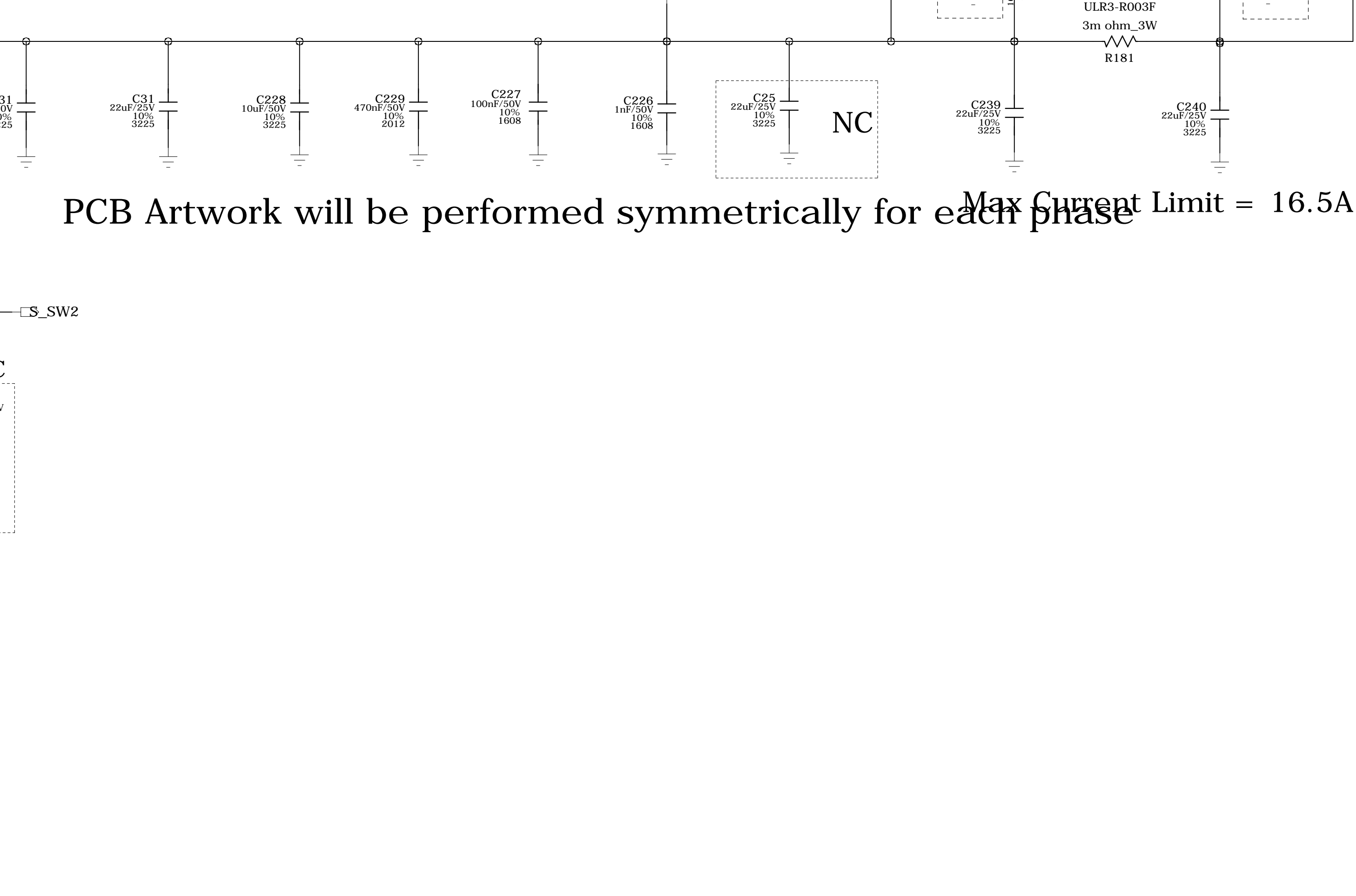
OPTION

First, The evaluation will be conducted by applying Four fet's
After PCB temperature measurement, FET will be reviewed in parallel
However, FETs (8EA) will be left in the PCB space

Slave Control_ 12.6V / 16.5A



Master Load_ 12.6V / 16.5A (20A Pattern width)



Max Current Limit = 16.5A

PCB Artwork will be performed symmetrically for each phase

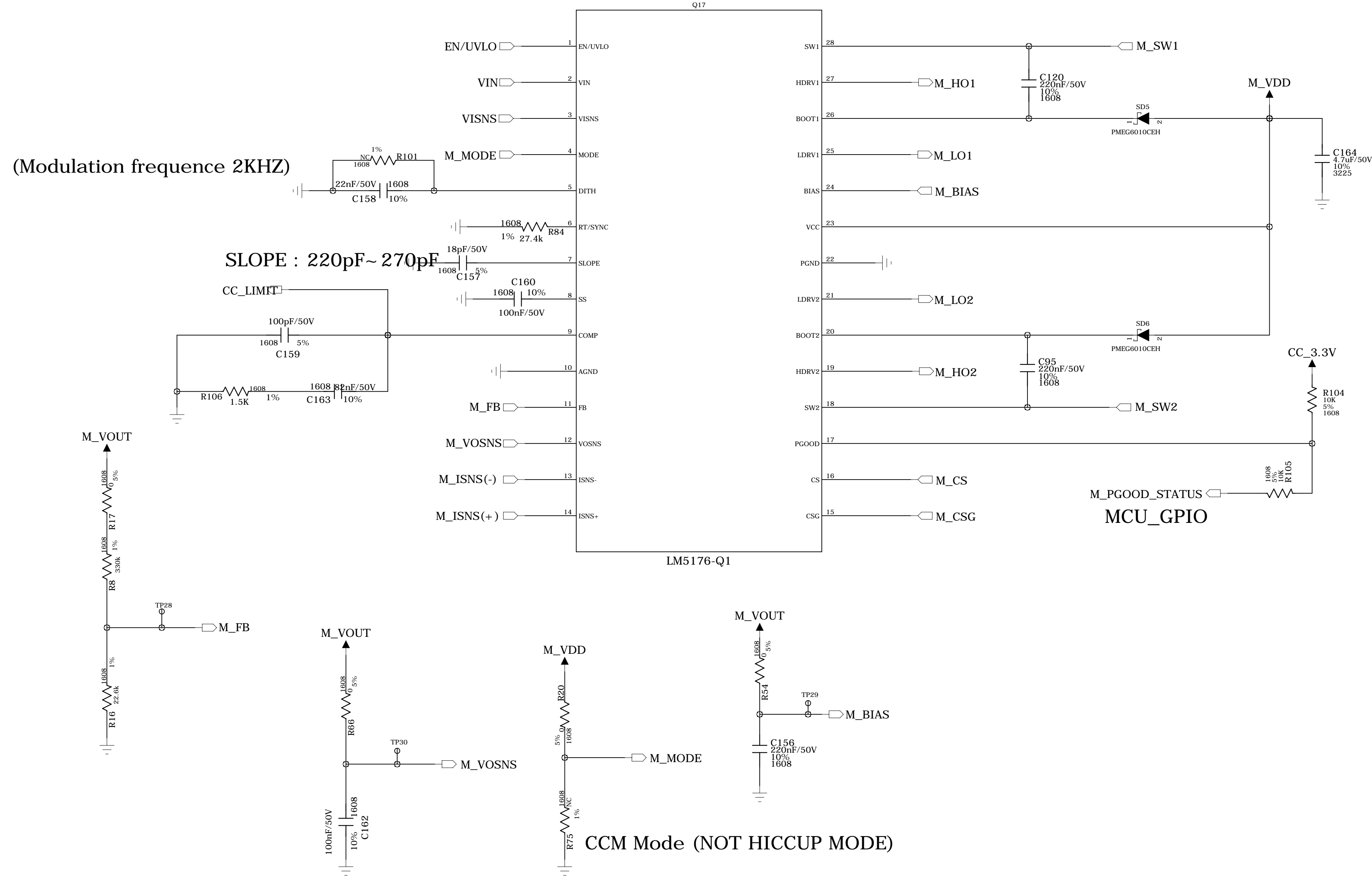
OPTION

First, The evaluation will be conducted by applying Four fet's
After PCB temperature measurement, FET will be reviewed in parallel
However, FETs (8EA) will be left in the PCB space

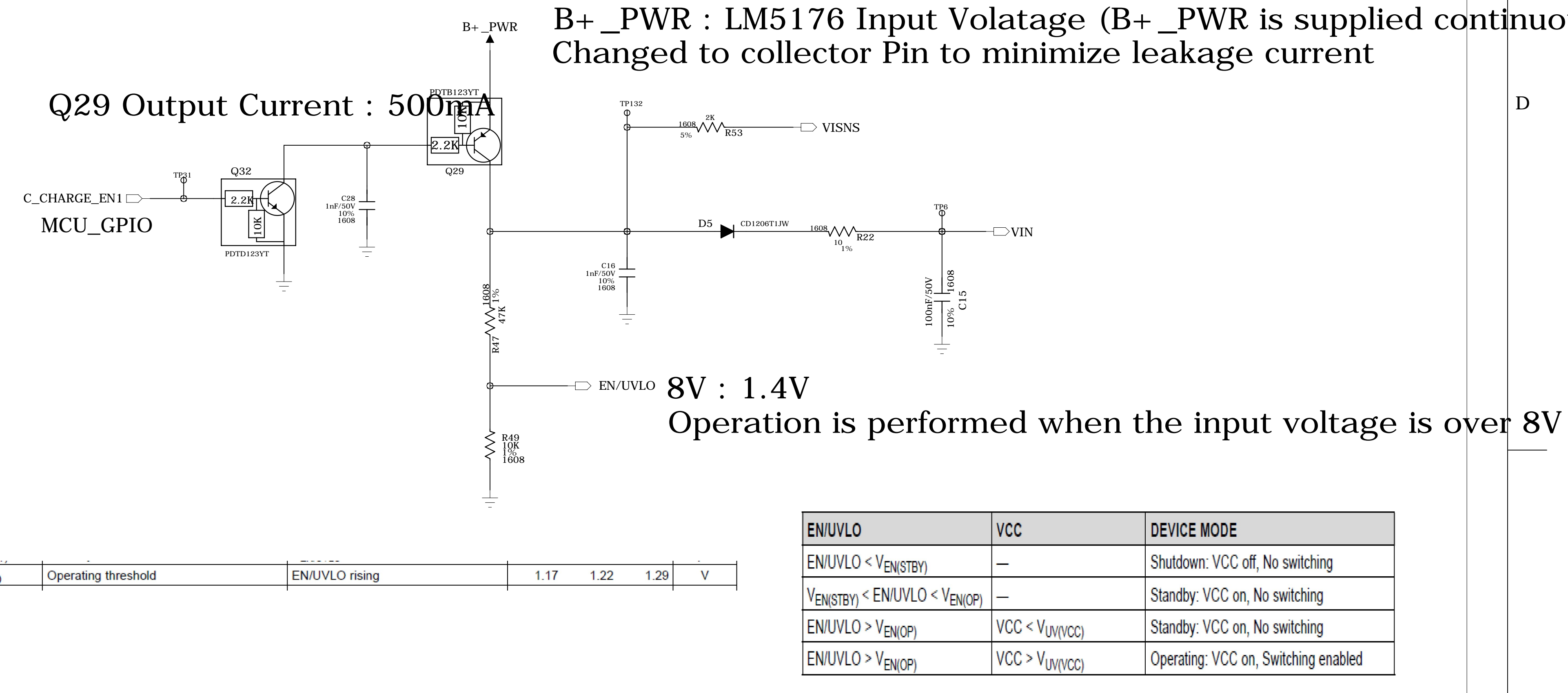
COMPANY:		TITLE:		BMS	
DRAWN: JH CHO	DATED: 18.02.28	CHECKED: JH CHO	DATED: 12.06.18	CODE: < Code >	SIZE: E
QUALITY CONTROL: < QC By >	DATE: < QC Date >	RELEASED: < Released By >	DATE: < Release Date >	REVISION: 2.00	REV: 2.00
DRAWN: < Scale >				SHEET: 2 OF 3	

REVISION RECORD			
ITER	ECD NO.	APPROVED	DATE

MASTER #1 LM5176



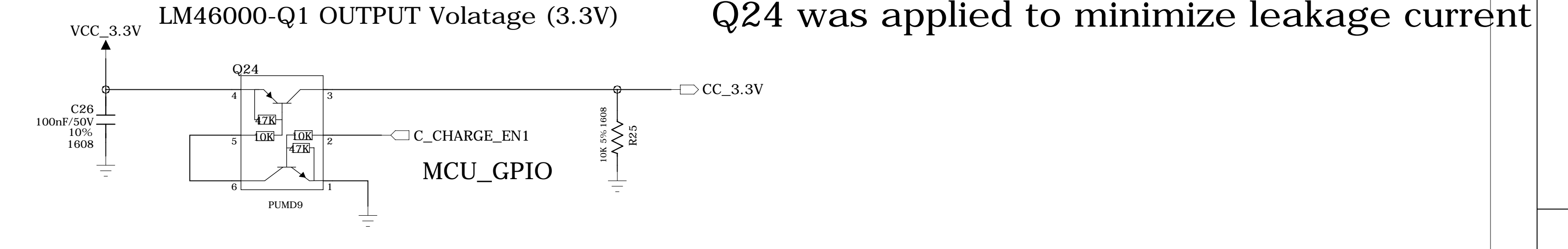
Power Supply of Master and Slave



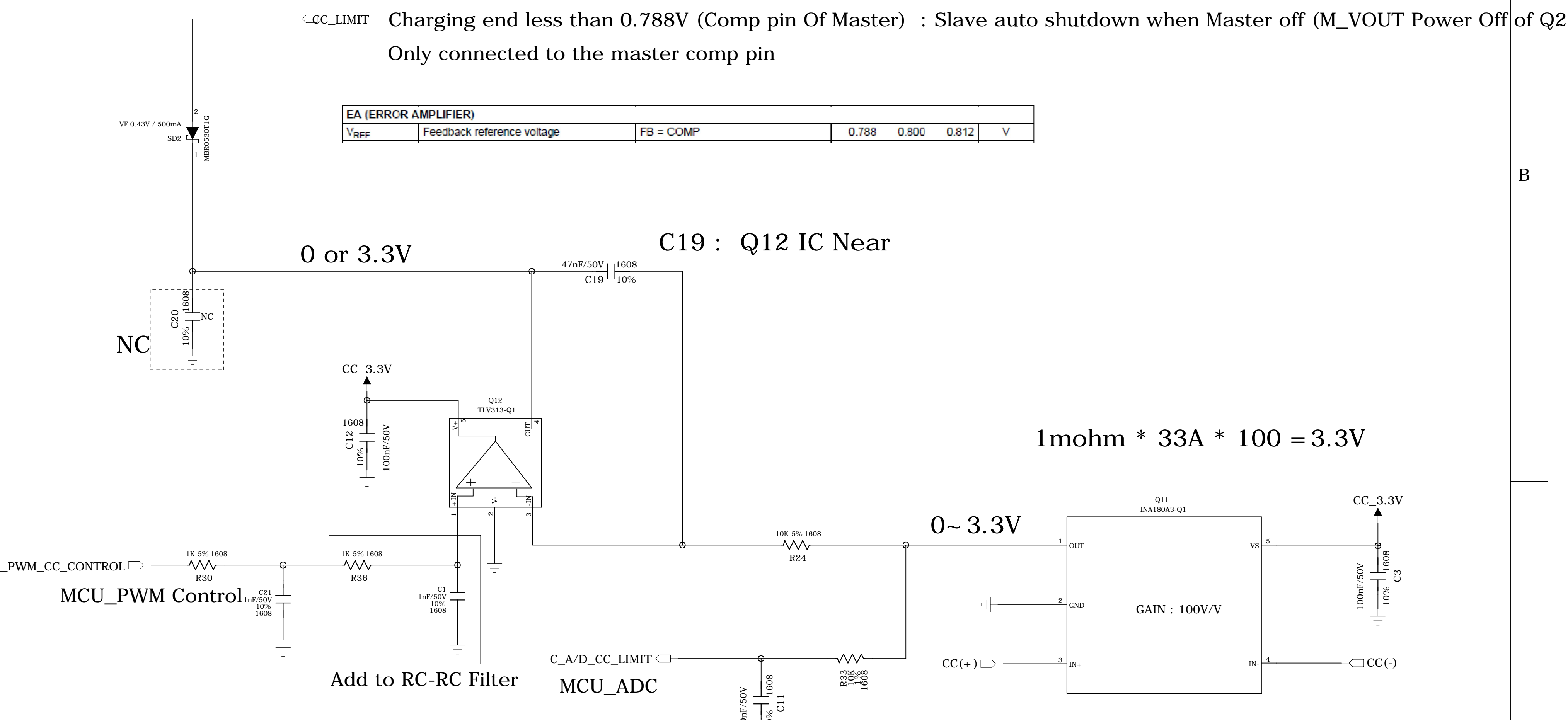
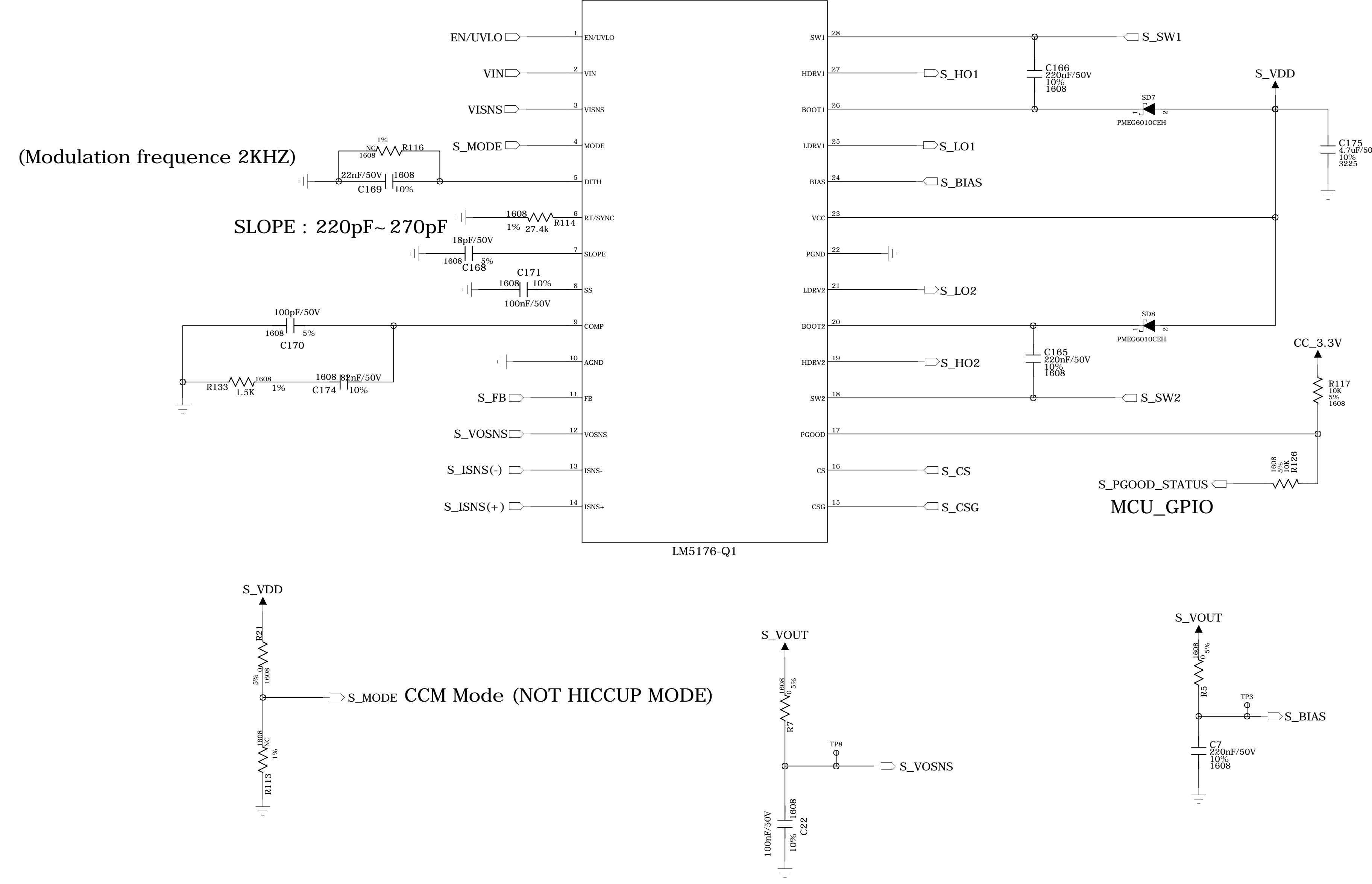
EN/UVLO	VCC	DEVICE MODE
$V_{EN(UP)} < V_{EN(STBY)}$	—	Shutdown: VCC off, No switching
$V_{EN(STBY)} < V_{EN(UP)} < V_{EN(OP)}$	—	Standby: VCC on, No switching
$V_{EN(UP)} > V_{EN(OP)}$	$VCC < V_{UV(VCC)}$	Standby: VCC on, No switching
$V_{EN(UP)} > V_{EN(OP)}$	$VCC > V_{UV(VCC)}$	Operating: VCC on, Switching enabled

CC (Constant Current) Variable Control

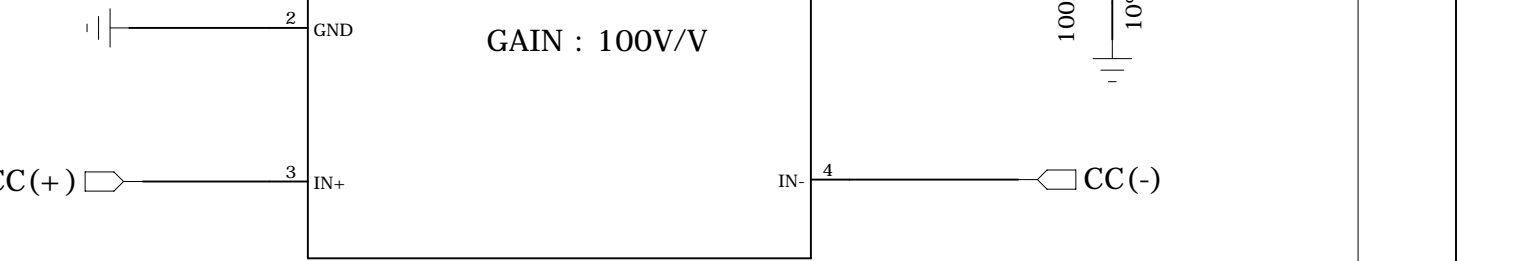
(3.3V Power is supplied continuously)



SLAVE #2 LM5176



$$1\text{mohm} * 33\text{A} * 100 = 3.3\text{V}$$



COMPANY		TITLE	
		BMS	
DRAWN: JH CHO	DATED: 18.02.28	CORE: E	SIZE: 2.00
CHECKED: JH CHO	DATED: 12.06.18	REVISION: 2.00	
QUALITY CONTROL: <QC By>	DATE: <QC Date>		
RELEASED: <Released By>	DATE: <Release Date>		