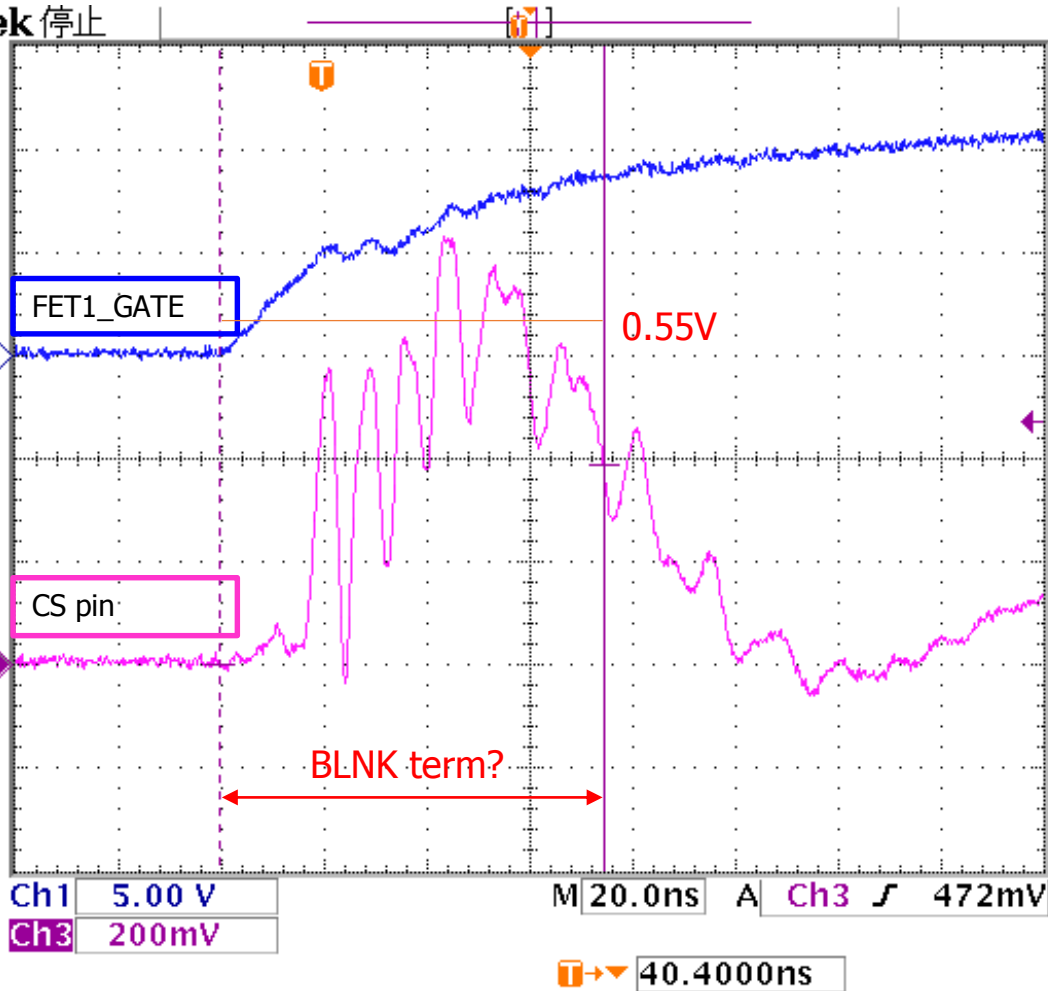


Tek 停止



Δ: 388mV
 @: 388mV
 Δ: 74.8ns
 @: 54.8ns

BLNK						
Blanking delay	In addition to t_1					
	BLNK = RTN	35	52	75		
	$R_{BLNK} = 49.9 \text{ k}\Omega$	41	52	63		
CS						
V_{CSMAX}	Maximum threshold voltage	$V_{CTL} = V_B, V_{CS} \uparrow$ until GATE duty cycle drops	0.50	0.55	0.60	V
t_1	Turn off delay	$V_{CS} = 0.65 \text{ V}$	25	41	60	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referred to CS	90	118	142	mV
I_{SL_EX}	Peak slope compensation current	$V_{CTL} = V_B, I_{CS}$ at maximum duty cycle (ac component)	30	42	54	μA
	Bias current (sourcing)	Gate high, dc component of CS current	2	3	4.2	μA

(1) The hysteresis tolerance tracks the rising threshold for a given device

<Question1>
 What does t_1 indicate(mean)? Does it mean deglitch time in case of $V_{cs}=0.65\text{V}$?
 Or, for example on the left side figure, after BLNK term 52ns with over V_{CS} ,
 Does the gate operation stop after T_1 (Turn off delay)?

BLNK						
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	Bias current (sourcing)	Gate high, dc component of CS current	2	3	4.2	μA

(1) The hysteresis tolerance tracks the rising threshold for a given device

<Question2>
 Our customer would like to know Blanking time which is $R_{BLINK}=92\text{kohm}$.
 And then, how much will the tolerance of Blanking time in case of $R_{BLINK}=92\text{kohm}$?
 If you have some formula for the tolerance, could you let us know?

11 Apr 2018
 12:47:21