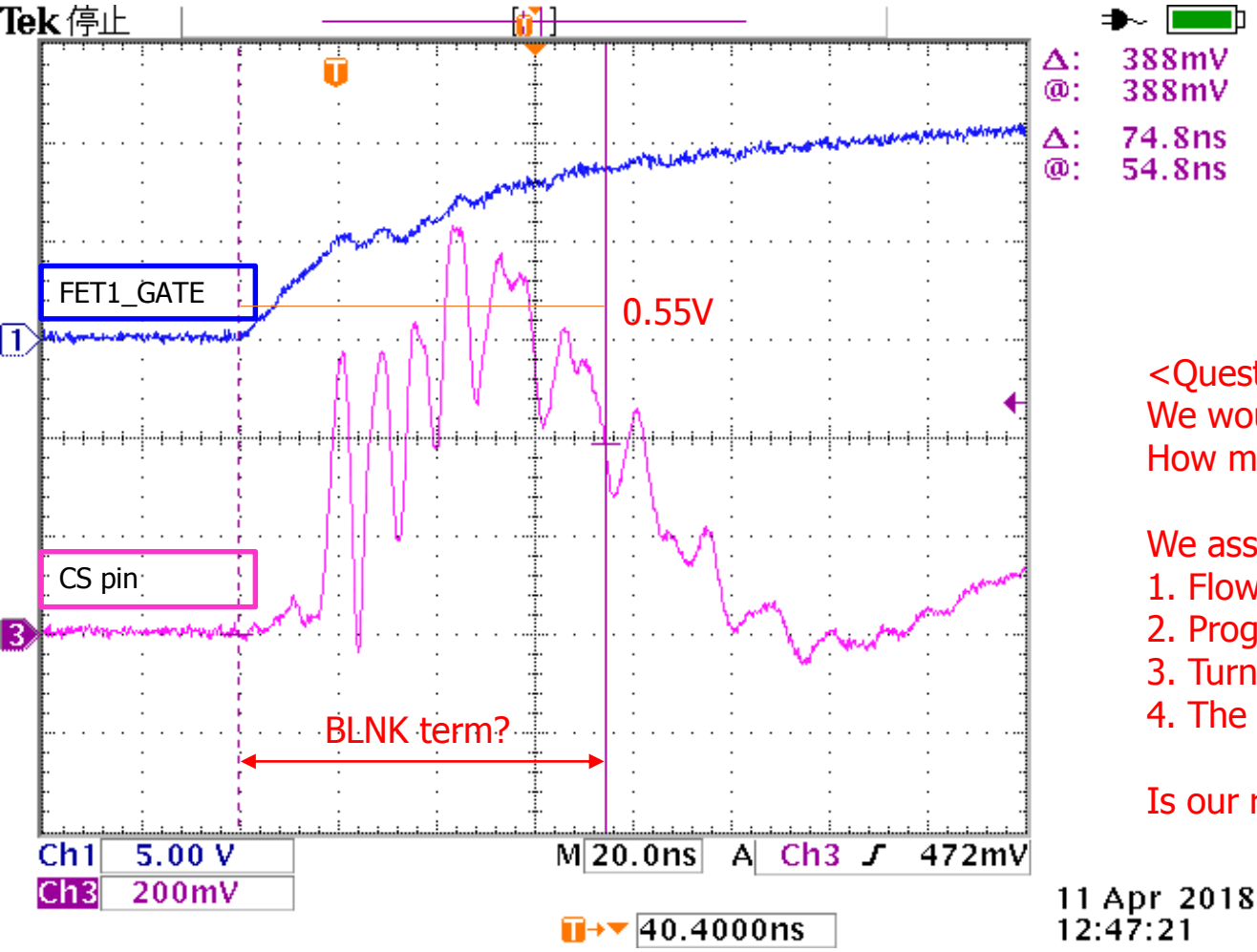

BLNK						
	Blanking delay	In addition to t_1 BLNK = RTN	35	52	75	ns
		R_{BLNK} = 49.9 kΩ	41	52	63	
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL} = V_B, V_{CS} ↑ until GATE duty cycle drops	0.50	0.55	0.60	V
t_1	Turn off delay	V_{CS} = 0.65 V	25	41	60	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referred to CS	90	118	142	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL} = V_B, I_{CS} at maximum duty cycle (ac component)	30	42	54	µA
	Bias current (sourcing)	Gate high, dc component of CS current	2	3	4.2	µA

(1) The hysteresis tolerance tracks the rising threshold for a given device

<Question1>
We would like to confirm operation of CS pin.
How much is the time until which FET gate turning off after CS sensing?

We assume following;
1. Flowing current over VCS threshold(0.50V～0.60V)
2. Progress of Blanking time(41ns～63ns@RBLUNK=49.9kohm)
3. Turn off delay(25ns～60ns)
4. The FET gate stops.

Is our recognition correct? If you have some advice, could you let us know?