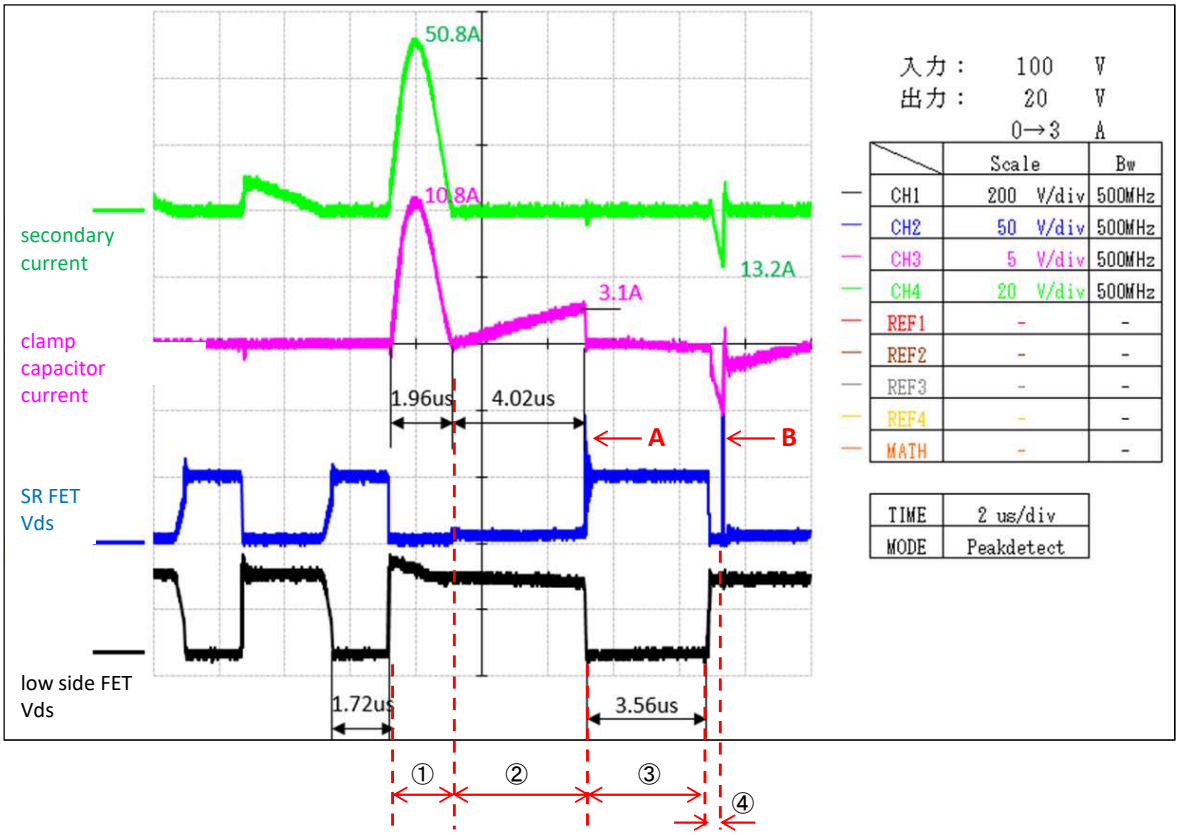

① The high-side FET turns on and the voltage accumulated in the clamp capacitor flows to the secondary-side rectifying capacit
② Since the high-side FET is ON as it is, an exciting current flows through the transformer. (Minus side)
Due to the exciting current, the charge of the clamp capacitor is pulled out and the voltage drops.
② → ③ Since the Coss of the low-side FET is pulled out by a large exciting current, the voltage change becomes steep.
The Vds surge of the synchronous rectifying FET becomes large. (Point A of the upper waveform)
③ The low-side FET turns on and the exciting current flows through the transformer. (Plus side)
④ During the minimum ON time of the synchronous rectifier FET (about 420 nsec), a current flows from the secondary rectifier capacitor to the clamp capacitor side.
After that, the synchronous rectification FET turns off, so a large Vds surge occurs. (Point B of the upper waveform)

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