TI Designs

90- to 265-V AC, 91% Efficiency, >0.94 PF Buck-PFC Plus 24-V, 30-W Brushless DC Motor Drive Reference Design

Design Overview

For achieving energy efficiency, ceiling fans and ventilation fans are moving from simple AC induction motors to brushless DC (BLDC) motors. Operation of BLDC motors from an AC supply requires AC-DC conversion with high efficiency and power factor. This operation also requires an inverter, which is efficiently controlled for low-noise operation of the motor. The TIDA-00652 reference design meets these challenges of higher efficiency and power factor in a simple way by using a single-stage power supply to convert the AC mains input into a low-voltage DC output. The design also combines a fully integrated and well protected single-chip, sensorless, sinusoidal brushless motor controller for low-noise operation.

Design Resources

TIDA-00652	Tool Folder Containing Design Files
UCC28180	Product Folder
DRV10983	Product Folder
MSP430G2231IPW14	Product Folder

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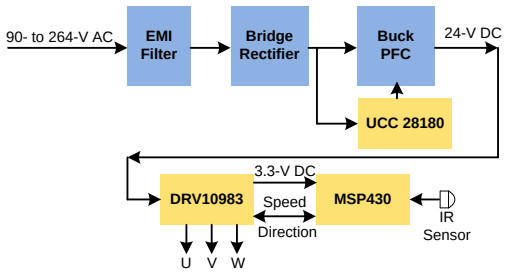
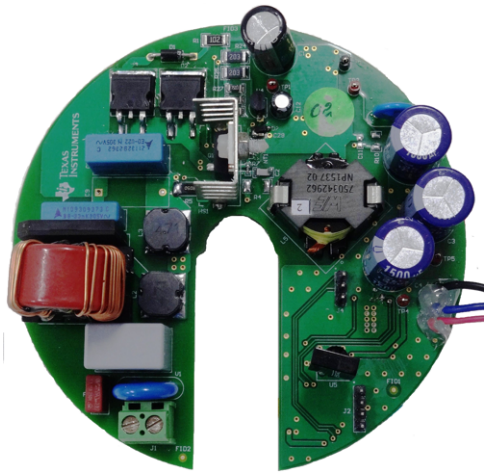
Design Features

- High Efficiency, Single Power Stage to Convert 90- to 265-V AC to 24-V DC
- Buck PFC Topology to Achieve High Input Power Factor (> 0.94) and High Efficiency (> 91%)
- Universal Input Capability (50/60 Hz, 90- to 265-V AC) With Minimum Variation in Efficiency
- Startup and Full-Speed Operation Even at 90-V AC Input
- Highly Integrated and Protected Single-Chip, Sinusoidal Brushless Motor Controller Reduces External Parts Count to Help Avoid Programming Overhead of Motor Control
- Infrared (IR) Remote-Based Speed Control

Featured Applications

- Energy Efficient Ceiling Fans
- Energy Efficient Ventilation Fans
- Blowers





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1 AC-DC Power Supply Specifications

Table 1. AC-DC Power Supply Specifications

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics						
V_{IN}	Input voltage		90	230	265	V AC
f_{AC}	Input frequency		47		63	Hz
I_{IN}	Input current	V_{IN} = nom, I_{OUT} = max			0.15	A RMS
V_{IN_UVLO}	Input UVLO	I_{OUT} = min to max			80	V AC
V_{IN_OV}	Input OV	I_{OUT} = min to max	265			
PF	Power factor	V_{IN} = nom, 100% load	0.94			
Output Characteristics						
V_{OUT}	Output voltage	V_{IN} = nom, I_{OUT} = nom	23.5	24	24.5	V
Reg_LN	Line regulation	V_{IN} = min to max, I_{OUT} = nom			5%	
Reg_LD	Load regulation	V_{IN} = nom, I_{OUT} = min to max			5%	
V_{OUT_RIPPLE}	Output voltage ripple	V_{IN} = nom, I_{OUT} = max			11.5	V_{PP}
I_{OUT}	Output current	V_{IN} = min to max	0		1.2	A
I_{OCP}	Output overcurrent	V_{IN} = nom	2.5			A
System Characteristics						
f_{SW}	Switching frequency				100	KHz
Eff_Peak	Peak efficiency	V_{IN} = nom, I_{OUT} = min to max			> 91%	
Eff_FL	Full load efficiency	V_{IN} = nom, I_{OUT} = max			= 90.8%	
Top	Operation temperature	V_{IN} = min to max, I_{OUT} = min to max	–25		65	°C

2 System Description

The use of brushless DC (BLDC) motors has been steadily increasing in applications where a wide range of speed variation is required, because BLDC motors are highly efficient as compared to induction motors. For very-low power applications, using low voltage motors offers several advantages, such as operation over universal voltage input conditions, cost savings on motors and passives, compact printed circuit board (PCB), and so forth. Moreover, highly integrated and protected low-voltage motor-driver integrated circuits (ICs) make the motor easier to control and more efficient. However, the use of a low voltage motor does require an efficient and low-cost AC-DC conversion stage. The TIDA-00652 design addresses this application requirement in a simple and efficient manner. The PCB also integrates an efficient and feature-rich motor controller stage, which enables customers to use this platform for applications such as ceiling fans, exhaust fans, ventilation fans, oven fans, and other low-power BLDC drives used in home and industrial appliances.

As Figure 1 shows, a buck power factor correction (PFC) power stage converts the 90- to 265-V, 50/60-Hz AC input to a regulated 24-V DC output. This design utilizes a UCC28180 PFC IC to control this power stage. The 24-V DC generated by the power stage is used to power the three-phase, sensorless BLDC motor controller DRV10983, which in turn drives the motor to control its speed. The DRV10983 controller also generates a 3.3-V supply, which powers the microcontroller (MCU). The MCU transmits the speed reference to the DRV10983 controller in the form of a 1.5-KHz pulse-width modulation (PWM) signal (producing a duty cycle proportional to the desired speed). This 1.5-KHz PWM signal is based on the signal received from the infrared (IR) sensor, which in turn is activated by a general-purpose IR remote control. Customizing the firmware of the MCU is easy for any given remote control data format.

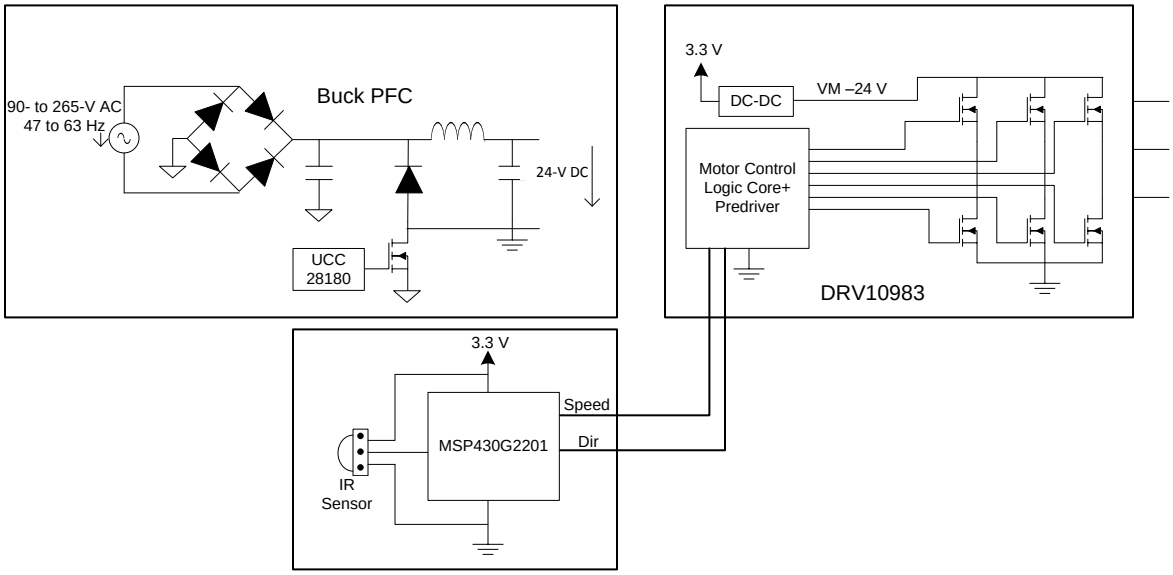


Figure 1. Top-Level Diagram Describing System Components

3 Block Diagram

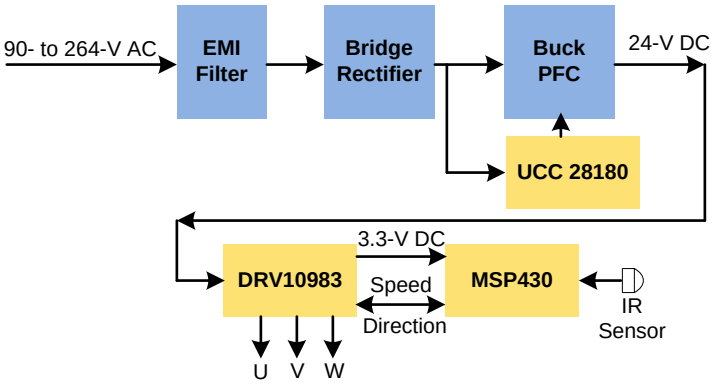


Figure 2. TIDA-00652 Block Diagram

3.1 Highlighted Products

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. Refer to the respective product datasheet for complete details on any highlighted device.

3.1.1 DRV10983 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver

The DRV10983 is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive current capability up to 2 A continuous. The device is specifically designed for low-noise, low external component count, 12- to 24-V motor drive applications. The device is configurable through a simple I2C interface to accommodate different motor parameters and spin-up profiles for different customer applications.

A 180° sensorless control scheme provides continuous sinusoidal output voltages to the motor phases to enable ultra-quiet motor operation by keeping the electrically induced torque ripple small.

The DRV10983 features extensive protection and fault detect mechanisms to ensure reliable operation. Voltage surge protection prevents the input V_{CC} capacitor from overcharging, which is typical during motor deceleration. The device provides overcurrent protection without the requirement for an external current sense resistor. Rotor-lock detect is available through several methods. These methods can be configured with register settings to ensure reliable operation. The device provides additional protection for under voltage lockout (UVLO) and for thermal shutdown.

The commutation control algorithm continuously measures the motor phase current and periodically measures the V_{CC} supply voltage. The device uses this information for back electromotive force (BEMF) estimation and the information is also provided through the I^2C register interface for debug and diagnostic use in the system, if desired.

A buck switching regulator efficiently steps down the supply voltage. The output of this regulator provides power for the internal circuits and can also be used to provide power for an external circuit such as an MCU. If providing power for an external circuit is not necessary (and to reduce system cost), configure the buck switching regulator as a linear regulator by replacing the inductor with a resistor.

Texas Instruments (TI) designed the interfacing to the DRV10983 device to be flexible. In addition to the I^2C interface, the system can use the discrete FG pin, DIR pin, and SPEED pin. SPEED is the speed command input pin. This pin controls the output voltage amplitude. DIR is the direction control input pin. FG is the speed indicator output, which shows the frequency of the motor commutation.

EEPROM is integrated in the DRV10983 device as memory for the motor parameter and operation settings. EEPROM data transfers to the register after power on and exit from sleep mode.

The DRV10983 device can also operate in register mode. If the system includes an MCU communicating through the I^2C interface, the device can dynamically update the motor parameter and operation settings by writing to the registers. In this configuration, the EEPROM data is bypassed by the register settings.

The DRV10983 has features that are highly useful for fan applications, such as:

- Programmable motor parameters for optimal working conditions with different motors
- Current limit, lock detection, and fault handling
- Thermal shutdown
- 180° sensorless control scheme
- Reliable starting of motor under different initial conditions
  - Motor stationary
  - Motor spinning in forward direction
  - Motor spinning in reverse direction
- Commutation control angle advance
- Motor initialization
  - Align
  - Initial position detect (IPD)
- Acceleration settings
- Figure 3 and Figure 4 show the start-up and operation waveforms of the DRV10983 device driving a fan load.

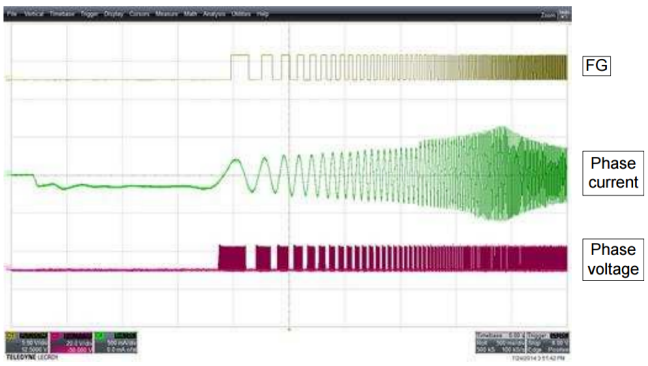


Figure 3. DRV10983 Start-Up Waveform

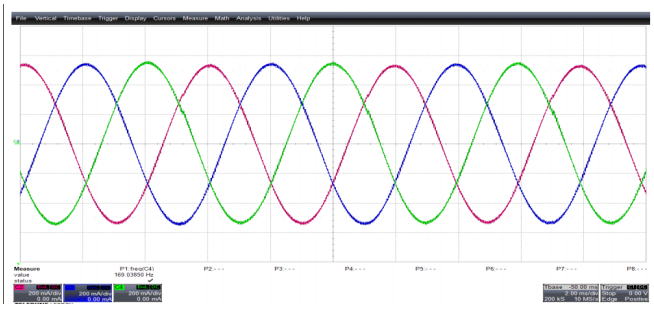


Figure 4. DRV10983 Operation Waveform

3.1.2 UCC28180—PFC Controller

Although the primary use of a UCC28180 targets boost PFC applications, the user can easily adapt it to control a variety of power topologies. This design highlights its usability to control a buck PFC topology.

The UCC28180 is a high-performance, compact eight-pin programmable frequency PFC controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. A reduced current sense threshold enables the UCC28180 device to utilize a 50% smaller shunt resistor, resulting in lower power dissipation. The UCC28180 also consists of an integrated fast gate driver, with a drive of 2-A source current and −1.5-A sink current, which eliminates the requirement for an external gate driver.

The UCC28180 device also has a complete set of system protection features that greatly improve reliability and further simplify the design, as the following list shows:

- Cycle-by-cycle peak current limit
- Output overvoltage
- V_{CC} undervoltage lockout (UVLO) protection
- Transconductance amplifiers enable the bypassing of current loop by using a simple Zener circuit

3.1.3 MSP430G2231—16-Bit MCU

The TI MSP430™ family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The device features a powerful 16-bit reduced-instruction-set-computing (RISC) central processing unit (CPU), 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430G2x21/G2x31 series is an ultralow-power mixed-signal MCU with a built-in 16-bit timer and ten input and output (I/O) pins. The MCUs of the MSP430G2x31 family have a 10-bit A-D converter and built-in communication capability using synchronous protocols, which consists of a serial peripheral interface (SPI) or I^2C.

Typical applications include low-cost sensor systems that capture analog signals, convert the signals to digital values, and then process the data for display or for transmission to a host system. The following features apply to the MSP430G2231:

- Low supply-voltage range: 1.8 V to 3.6 V
- 16-bit RISC architecture, 62.5-ns instruction cycle time
- 16-Bit Timer_A with two capture/compare registers
- Universal serial interface (USI) supporting SPI and I^2C
- 10-bit, 200-ksps A-D converter with internal reference, sample-and-hold, and autoscan
- Serial onboard programming, no external programming voltage required, and programmable code protection by security fuse
- On-chip emulation logic with Spy-Bi-Wire interface

4 System Design Theory

4.1 Overview

The PFC stage converts the incoming rectified line voltage to a DC voltage on the output capacitor bank C_o. The power transfer occurs during instances when the line voltage is greater than the output voltage. The resulting conduction angle is a function of both the incoming line and output voltages. In the current TIDA-00652 design, the output voltage is set to 24-V DC. This output voltage is low enough to allow conduction angles sufficient to achieve a power factor (PF) of at least 0.94 over a wide-input voltage range from 90-V AC to 265-V AC. Other output voltage levels (below 26 V) can be set by altering the voltage sensing network at the V_{SENSE} pin (see Section 4.4). Figure 5 shows a basic buck PFC power stage. This low-side switched buck stage has the same performance as the more commonly used high-side switched buck converter. The incoming AC line is fed through a rectifier and filter stages (not fully shown in this figure). The resulting unipolar voltage is then fed into the power stage. The MOSFET is switched at a constant frequency of 100 KHz. The output voltage (V_o) is developed across capacitor C_o. The system is operated in discontinuous conduction mode (DCM) to achieve good input current THD and power factor. Figure 6 and Figure 7 show an abstract of the current and voltage waveforms at various locations in the converter under DCM operation. For clarification purposes, note that the switching frequency in the figures is deliberately shown to only be a few times higher than the line frequency (50 Hz to 60 Hz). However, in practice, the switching frequency is usually selected to be many times higher than the line frequency.

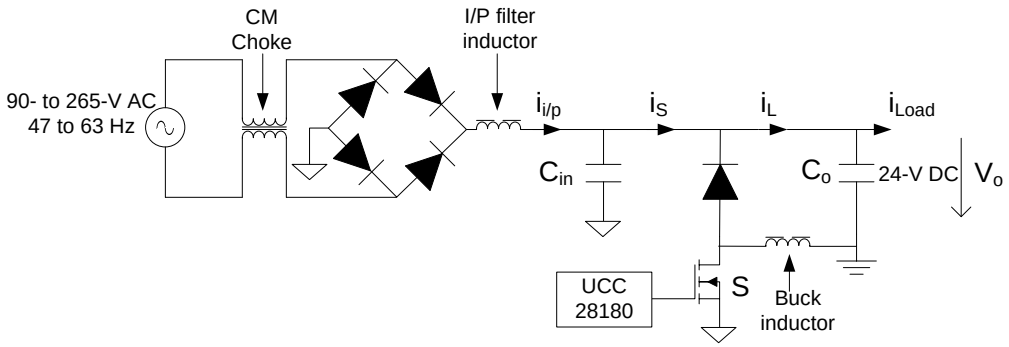


Figure 5. Buck PFC Circuit

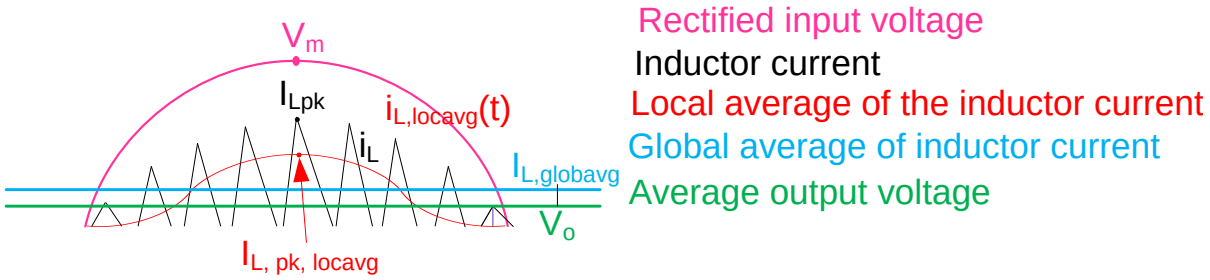


Figure 6. Waveforms Showing Inductor Current, Rectified Input Voltage, and Output Voltages of Buck Converter

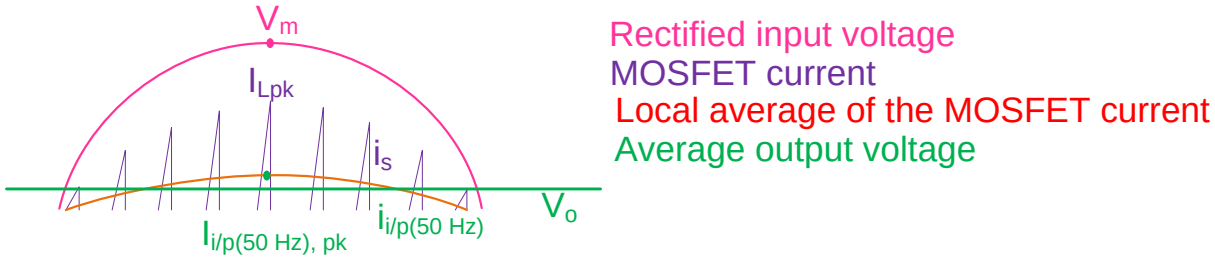


Figure 7. Waveform Showing Rectified Input Voltage and MOSFET Current

4.2 Buck Converter Inductor and Capacitor Calculation

The PFC inductor is designed for an inductance value that ensures DCM operation at the lowest input line voltage, above which good power factor and THD are desirable (that is, > 90-V AC) right up to the full-peak load. With an appropriate value of inductance, operation at higher loads, especially under low-line conditions then results in CCM operation, especially towards the peak of the input voltage waveform. Equation 1 calculates the inductance required for a design:

$$L = \frac{1}{2 \times f_{sw} \times I_{in,pk}} \times \left(\min\left(V_m\right) - V_o\right) \times \left(\frac{V_o}{\min\left(V_m\right)}\right)^2 \quad (1)$$

For the present design, with a 24-V output and a minimum input voltage of 90 V, the period of non-conduction can be neglected for all practical purposes, resulting in Equation 2:

$$I_{IN\_PK} \approx \frac{P_{IN\_AVG} \times \pi}{2 \times \min\left(V_m\right)} \quad (2)$$

Refer to the following seminar *Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations* (SLUP264) for a detailed calculation of $I_{in,pk}$ [1].

Using Equation 3 and assuming an AC-DC conversion efficiency of 0.9, output power of 36 W, and min (V_m) = 90 $\sqrt{2}$ V:

$$L = \frac{1}{2 \times 100 \times 10^3 \times 0.41} \times \left(90\sqrt{2} - 24\right) \times \left(\frac{24}{90\sqrt{2}}\right)^2 = 37\ \mu H \quad (3)$$

An inductor of 34 µH has been selected to guarantee operation in DCM, even under slight overload conditions.

4.3 Calculation of Output Capacitance

Assuming that the percentage of non-conducting period is minimal, the required output capacitance can be calculated as Equation 4 shows:

$$C_o \approx \frac{2 \times P_{LOAD}}{\pi \times V_o \times \Delta V_o \times 2 \times f_{LINE}}$$

where

- ΔV_o = the peak-to-peak voltage ripple on the output (**specification** of < 2 V)
- f_{LINE} = the input line frequency
- P_{LOAD} = the output load power (all in SI units) (4)

Insert the values into the preceding Equation 4 to obtain the following result in Equation 5:

$$C_o \approx \frac{2 \times 30}{\pi \times 24 \times 2 \times 2 \times 50} = 3.9\ mF \quad (5)$$

A capacitance of 4.5 mF has been selected to accommodate overload conditions and effects caused by aging.

4.4 Voltage Sensing Circuit

A high-voltage PNP transistor can be connected across the high-side bus voltage to provide a collector current that varies in proportion to the bus voltage (see Figure 8). This current can be converted to a sense voltage by feeding into a ground-referenced resistor. With this connection, the voltage sense is also referenced to ground. This circuit is low cost and contains only a few more components than a typical resistor divider. The PNP transistor must be rated for at least 500 V for high line-voltage operation; however, these transistors are available in suitable, small surface-mount packages and leaded packages. Equation 6 shows the relation between the sense voltage V_{SENSE} and the bus voltage, assuming that the bus voltage is sufficient to forward bias the transistor and neglect its base current as compared to its collector current.

$$V_{SENSE} \approx \frac{V_o \times \frac{R_1}{R_1 + R_2} - V_{EB}}{R_3} \times R_{SENSE} \tag{6}$$

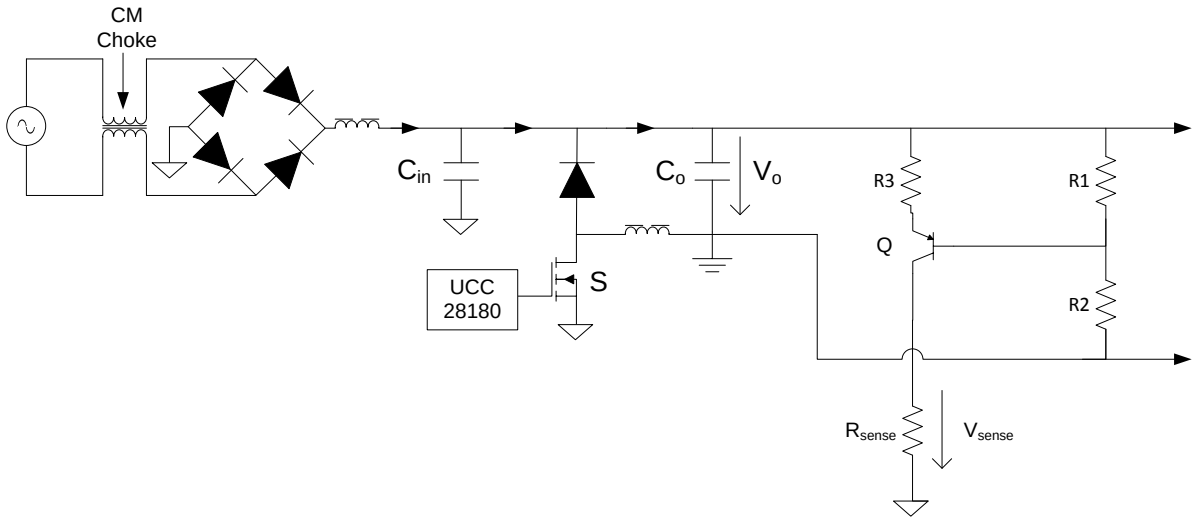


Figure 8. Voltage Sensing Circuit

Refer to the following seminar (SLUP264) for a more detailed equation that includes the effect of the transistor current gain. Adjusting the value of R_{SENSE} sets the V_o voltage under closed-loop operation [1].

4.5 Control

The UCC28180 is a boost PFC IC by design; however, the flexibility offered by the IC makes it easily adaptable to control a buck PFC topology. This adaptation is possible by bypassing the current loop by placing a Zener-based constant voltage source at the I_{COMP} pin of the UCC28180 device. The user must be careful to ensure that the potential of the I_{COMP} pin is kept above 3 V.

The voltage at the V_{COMP} pin is automatically adjusted by the closed-loop operation such that desired ramp slope is achieved, which in turn produces the desired duty cycle to maintain the output voltage at the desired level (24 V in this design).

From the datasheet of UCC28180, the ramp slope is provided by Equation 7:

$$M \approx \frac{f_{sw}\ KHz}{65\ KHz\mu s} \times 0.1223 \times (V_{COMP} - 0.5)^2\ \frac{V}{}; \quad \text{for } 0.5 \le V_{COMP} \le 4.6\ V$$

$$\Rightarrow \frac{dM}{dV_{COMP}} = \frac{f_{sw}\ KHz}{65\ KHz} \times 0.1223 \times 2 \times (V_{COMP} - 0.5)\ \frac{V/\mu s}{V}; \quad \text{for } 0.5 \le V_{COMP} \le 4.6\ V \tag{7}$$

The peak of the ramp voltage is given by Equation 8:

$$V_{RAMP\_PEAK} \approx \frac{M}{f_{sw}} \tag{8}$$

For an I_{COMP} voltage of 3.3 V, the duty cycle D can be calculated by using Equation 9:

$$D \approx \frac{V_{RAMP\_PEAK} - 3.3}{V_{RAMP\_PEAK}} \quad (9)$$

Also, assuming a 100% conduction angle, the operating duty cycle D can be calculated using Equation 10:

$$D \approx \frac{1}{V_m} \times \sqrt{\frac{P_{IN} \times 4 \times L}{T_{sw}}} \quad (10)$$

When V_{IN} = 90-V AC (assuming an efficiency of 0.9), the maximum expected value of duty cycle D can be calculated using Equation 11:

$$D \approx \frac{1}{127.26} \times \sqrt{\frac{\left(\frac{36}{0.9}\right) \times 4 \times 34 \times 10^{-6}}{10 \times 10^{-6}}} = 0.183 \quad (11)$$

This result from Equation 11 corresponds to a V_{RAMP_PEAK} of 4.038, which in turn corresponds to an M of approximately 0.4038 V/µs and a V_{COMP} of 1.86 V. Having established these corresponding values, the user can place a Zener diode at the V_{COMP} pin (D_{ZCOMP} in Figure 9) to limit the voltage to 1.9 V (if required). This Zener diode placement also limits the minimum input voltage at which the rated voltage output is guaranteed.

The compensation network is almost the same as that used for a boost PFC circuit, except for the value of the capacitor C_{COMP2}, which must be adjusted so that the output voltage ripple has a minimal effect on the duty cycle and sufficient time is allowed for a soft-start operation. The capacitor cannot be made too small because during overload conditions the IC may connect a 4-kΩ resistor in parallel to this capacitor (soft overcurrent limit). A capacitor with a large enough value stabilizes the voltage at the V_{COMP} pin, in spite of the soft overcurrent limit, which occurs only in transients in the case of controlling a buck converter.

The user can add a high value resistor (between 300 kΩ to 1 MΩ) in parallel to the capacitor C_{COMP2}, if voltage droop characteristics with increase in load and decrease in input voltage is desired.

A small signal diode, D_{ST}, is required to bias the V_{SENSE} pin to a positive voltage during start-up, which is required for the IC to begin operation.

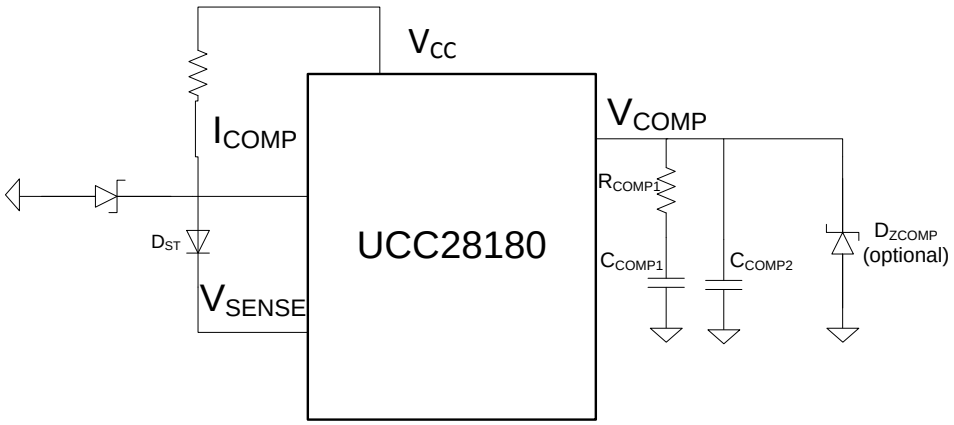


Figure 9. Control Circuit Diagram

5 Getting Started Hardware

1. Connect the single-phase AC power supply between pins 1 and 2 of connector J1 and turn on the power supply switch. A multimeter connected between TP5 (+ve) and TP7 (–ve) must read approximately 24-V DC. The user can tune the voltage between 10 V and 26 V by changing the resistors R17 and R20. The higher the value of the equivalent sense resistor is (R17 in parallel to R20), the lower the set point of the output voltage. The user can check the performance of the system by connecting a resistive load between TP5 (+ve) and TP7(–ve), specified as < 35 W. The DRV10983 device solely accounts for short circuit and overload protection; therefore, do not perform any short circuit or extreme overload tests on the 24-V DC output (between TP5 and TP7). Also, avoid start up when resistive load is connected.
2. Connect a 24-V external DC power supply between TP4 (+ve) and TP6 (–ve) before programming the DRV10983 device. The DRV10983 device can be programmed through the J4 connector. Refer to the schematic and layout for pin assignments (located in the *Tools & software* section). Refer to the DRV10983 webpage for more information regarding programming the DRV10983 device: http://www.ti.com/product/drv10983.
3. The MSP430 controller is programmable through connector J2. The following Section 6 details programming the MSP430G2231. Unlike the DRV10983 device, programming the MSP430 controller does not require an external power supply. The power supply from the programmer can be used.
4. After programming the DRV10983 and MSP340G2231IPW14 devices, short TP5 to TP4 and TP7 to TP6. Connect the U, V, and W outputs of the board to the motor U, V, and W phases respectively. Connect and turn on the input power, which enables the fan to run. Press the appropriate button on the remote control to change the fan speed. Ensure that the rated power consumption of the fan selected is < 35 W.

6 Getting Started Firmware

6.1 Motor Speed Control Firmware

The firmware for motor speed control consists of a remote that is based on the NEC IR transmission protocol running at a carrier frequency of 38 KHz. The TIDA-00652 design utilizes a firmware developed for the MSP430G2231 device to provide a three-step PWM duty cycle command to the DRV10983 device. This firmware consists of the following features:

- A PWM duty cycle command is generated at 1.5 KHz.
- Each time the user presses the increment key, the duty cycle increases. When the user presses the decrement key, the duty-cycle is reduced. The maximum duty cycle is 90% and the minimum duty cycle is limited at 50%.
- By changing the key codes in the software, the firmware can be used with any IR remote that supports the NEC IR transmission protocol.

6.2 Instruction to Change IR Remote Key Codes for Speed Control

Important downloads:

- The firmware for this design has been developed for MSP430G2231 using the TI Code Composer Studio™ (CCS) IDE version 5.5.0. The user must ensure to have CCS version 5.5.0 or any other later version installed as a first step. For details on downloading CCS, refer to http://www.ti.com/tool/ccstudio-msp430.
- Download the TIDA-00652 firmware project files from the reference design webpage (TIDA-00652).

Hardware setup:

To obtain the remote key codes, do not apply the main AC power to the board. The onboard connector J2 provides a four-pin JTAG Spy-Bi-Wire interface. J2 has a pin for 3.3 V and any utility that provides SPI-programming support J2 is capable of providing 3.3 V to onboard devices MSP430G2231 and IR senor TSOP31338.

Steps to change remote key codes:

1. Launch the CCS software. Select *Import Project* from the menu toolbar. Browse to the file directory containing the firmware in the subsequent pop-up window. Check the CCS project found and click the *Finish* button (see Figure 10). The user can copy the project into the workspace, if desired.

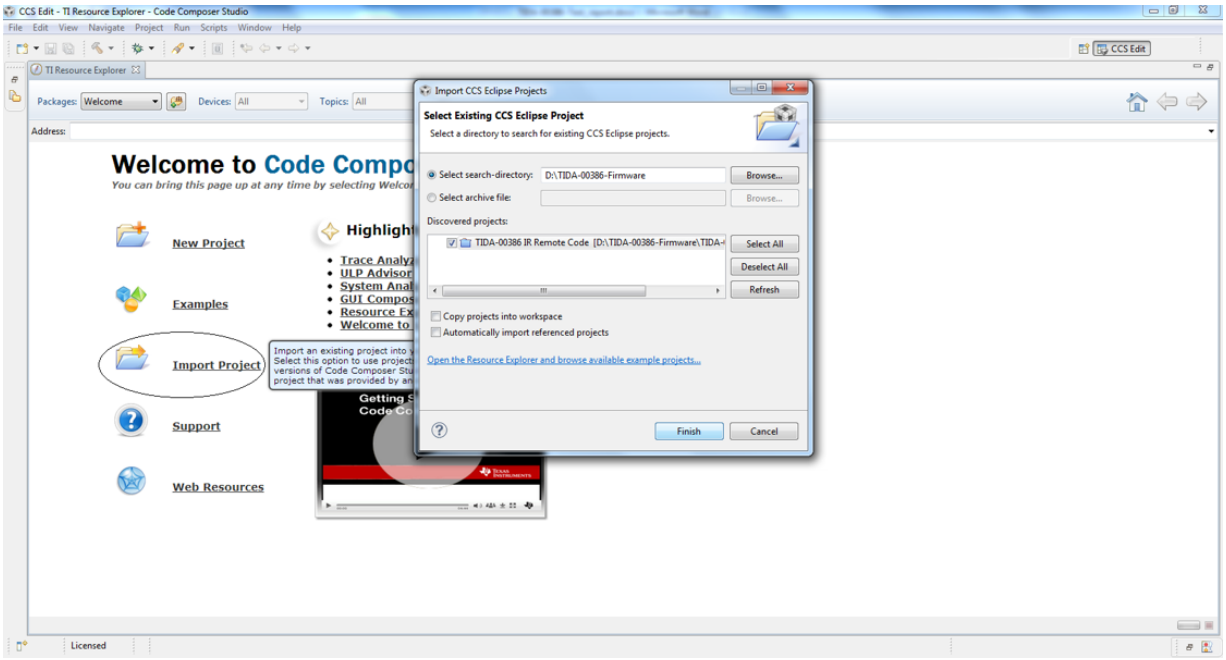


Figure 10. Changing Remote Codes in Software—Step 1

2. Build the project, by first left-clicking the project title and then clicking the *Build* button, as the following Figure 11 shows. Close the TI resource explorer window.

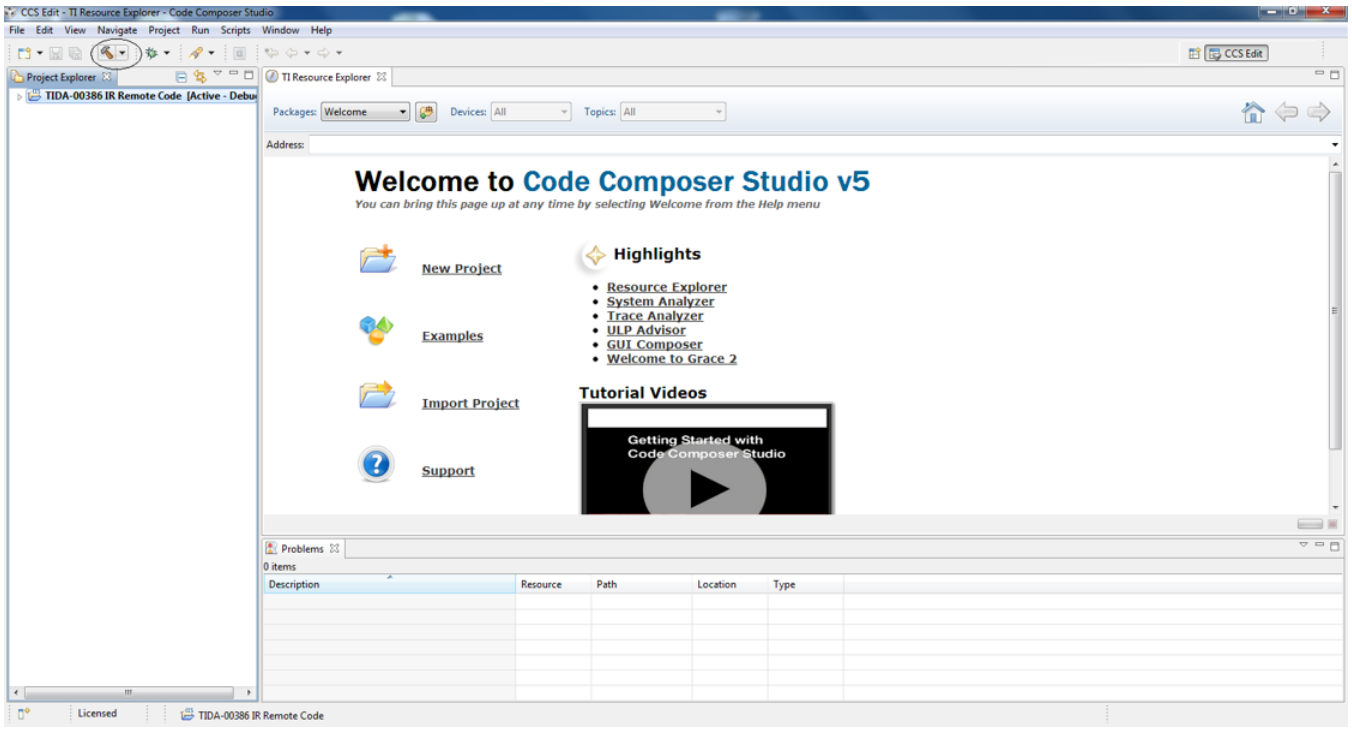


Figure 11. Changing Remote Codes in Software—Step 2

3. Download the code by clicking the *Debug* button (bug icon). If the “ULP Advisor™” window appears, click the *Proceed* button (see Figure 12). The user can choose to enable the option “Do not show this message again” to avoid its appearance in future launches.

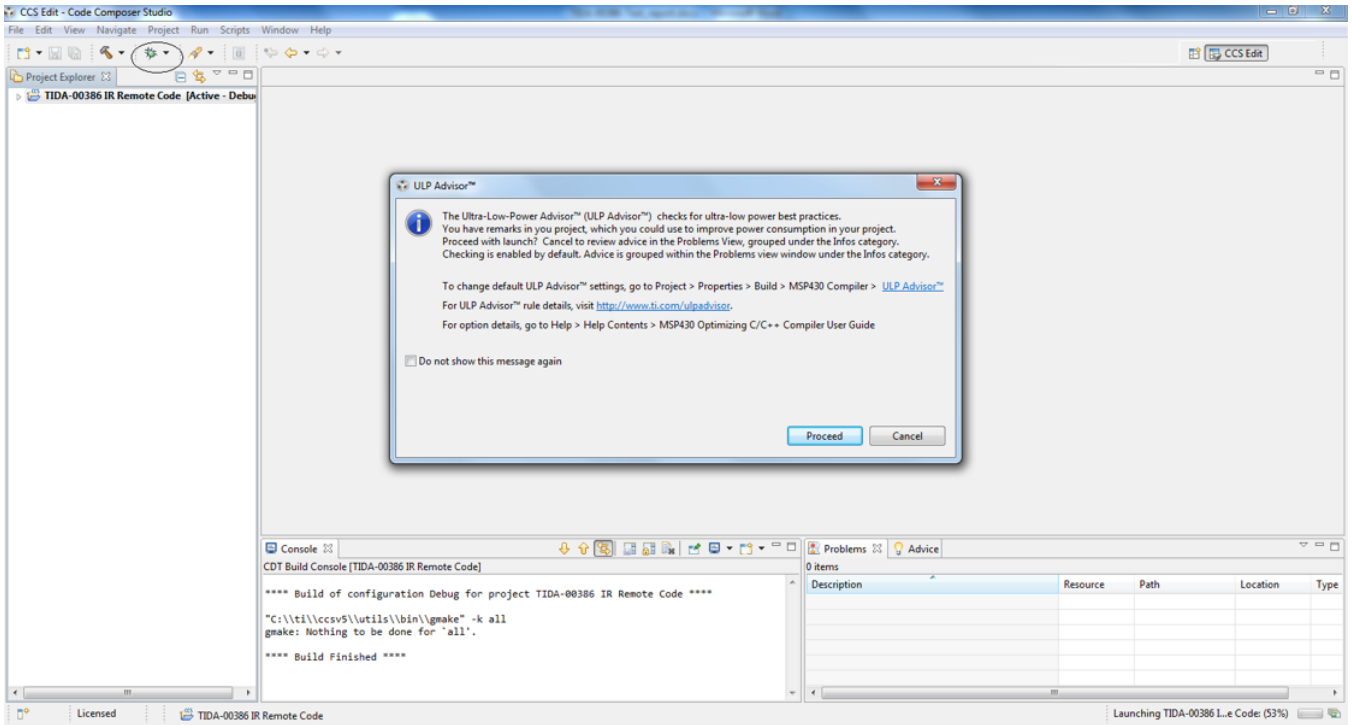


Figure 12. Changing Remote Codes in Software—Step 3

4. After successfully downloading the code, the following window in Figure 13 appears. Match the console message and click the *Resume* button (the “play” arrow icon in the taskbar).

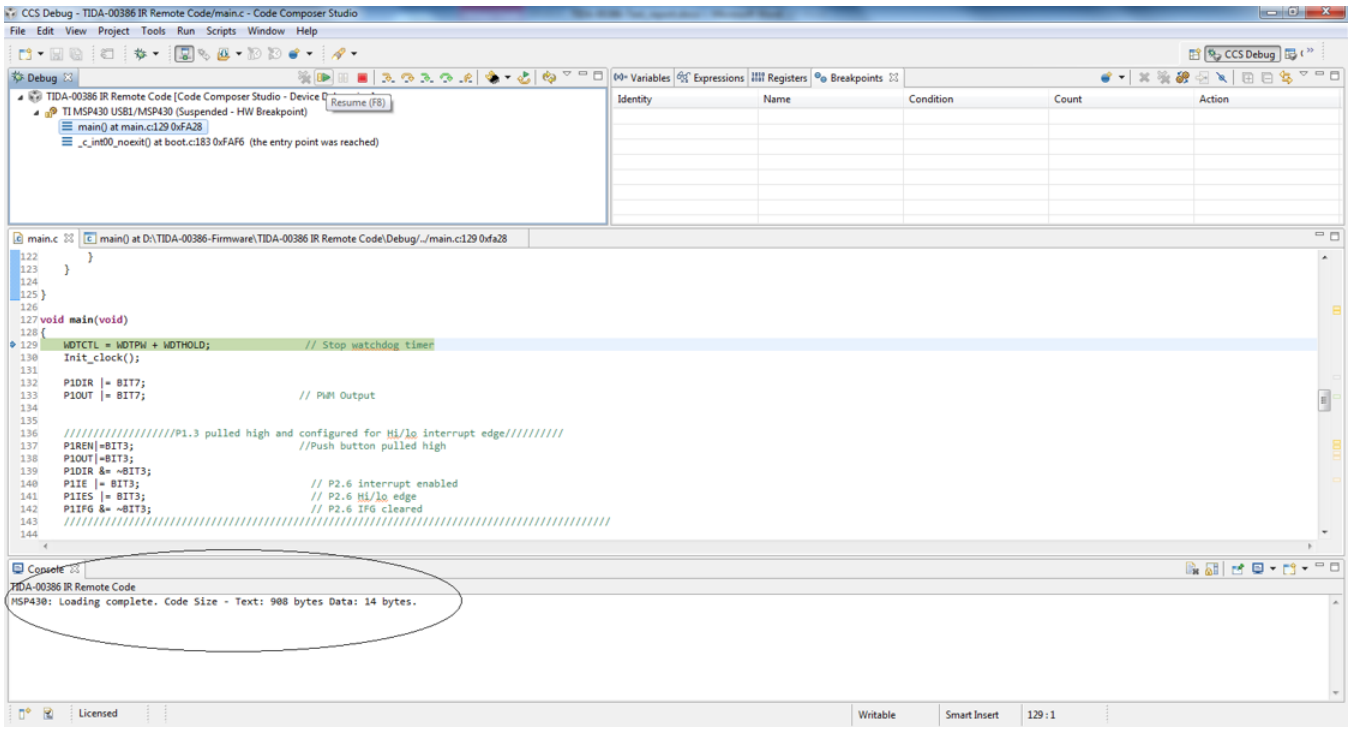


Figure 13. Changing Remote Codes in Software—Step 4

5. Insert a breakpoint by right-clicking at line 112 (right side of 112) and then selecting the *Breakpoint (Code Composer Studio)* option from the cursor prompt (see Figure 14).

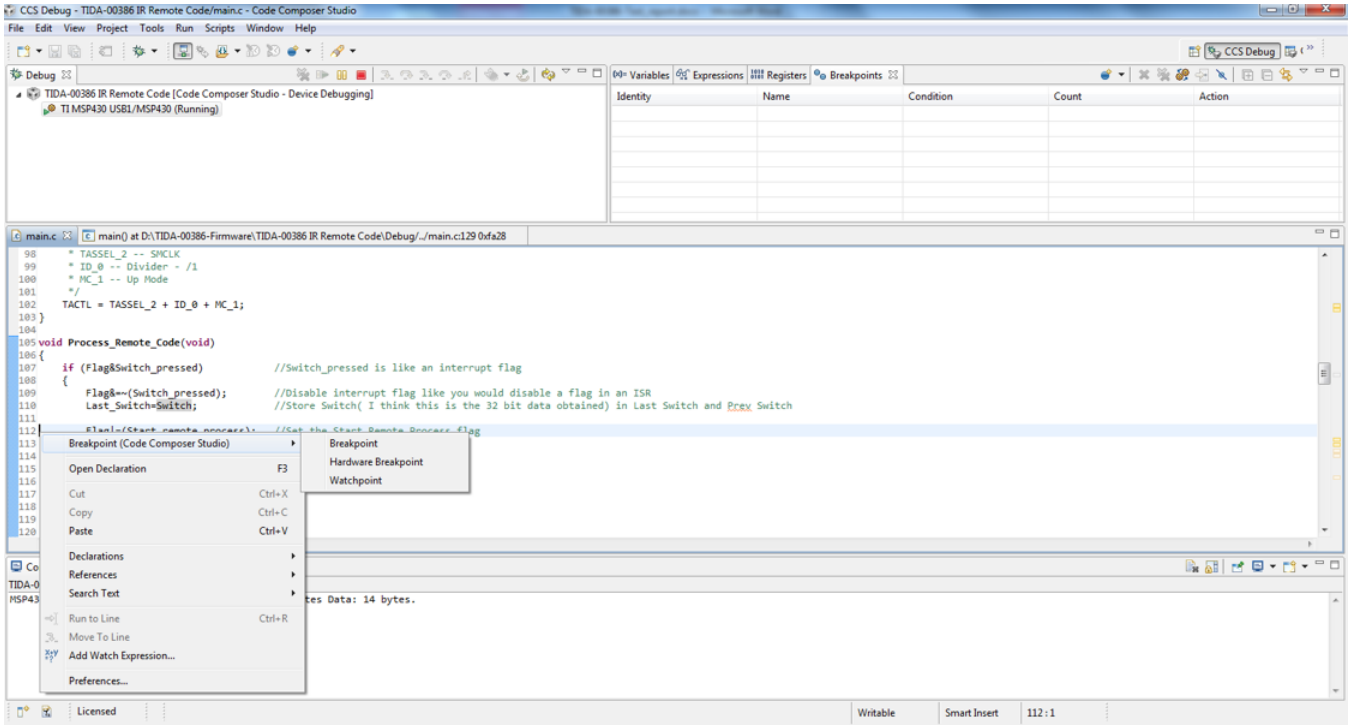


Figure 14. Changing Remote Codes in Software—Step 5

6. Point the remote toward the IR sensor and press the increment key. If the previous steps have been performed correctly, the code halts at line 112. Move the cursor to the “Switch” variable on line 110 and a pop-up window appears as the following Figure 15 shows. Note the hex code as this is the code for the increment key of the remote in use.

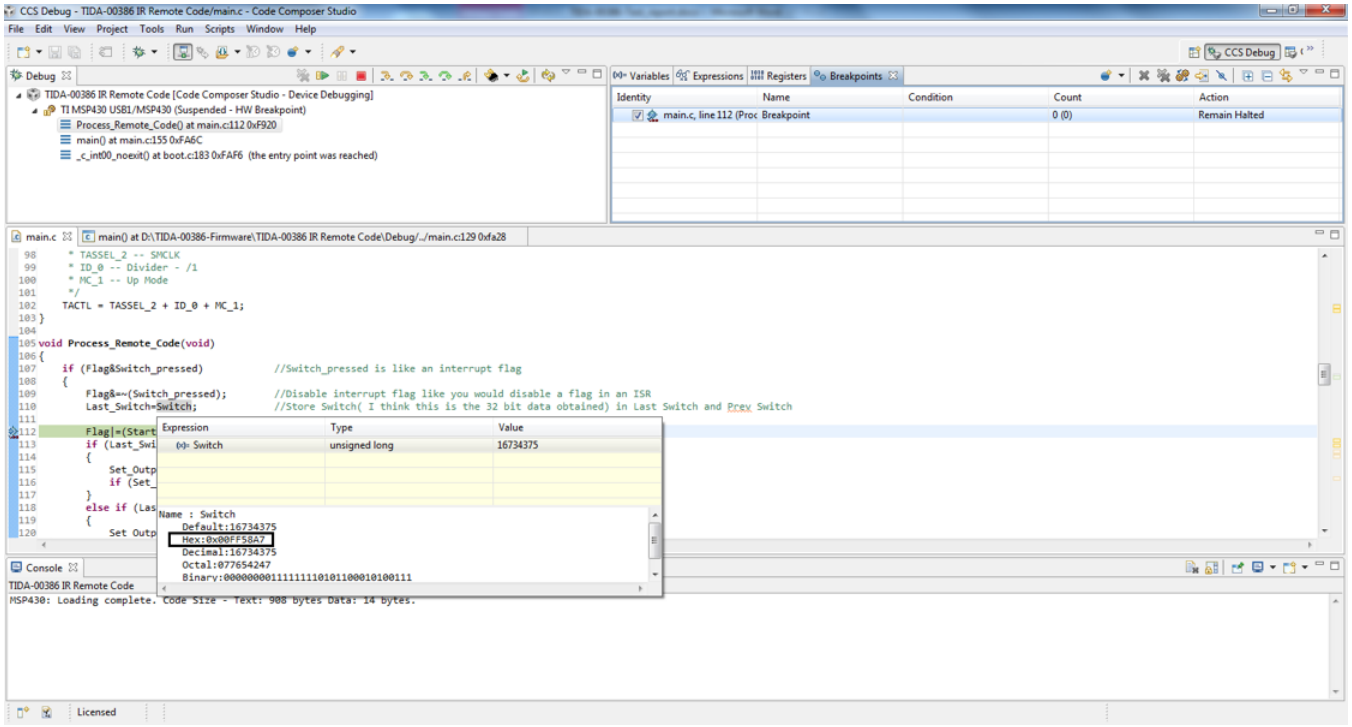


Figure 15. Changing Remote Codes in Software—Step 6

7. Resume the code as outlined in Step 4. Point the remote toward the IR sensor and press the decrement key. Repeat the process in Step 6.

8. Repeat Step 6 and Step 7 two to three times and ensure that both key codes are the same every time. Upon successful repetition, move the cursor to line 112 and disable the breakpoint by right-clicking exactly at the breakpoint (left side of line 112) and selecting the *Toggle Breakpoint* option from the pop-up window (see Figure 16). Terminate the debug launch by clicking the *Stop* button (red square icon) next to the *Resume* button.

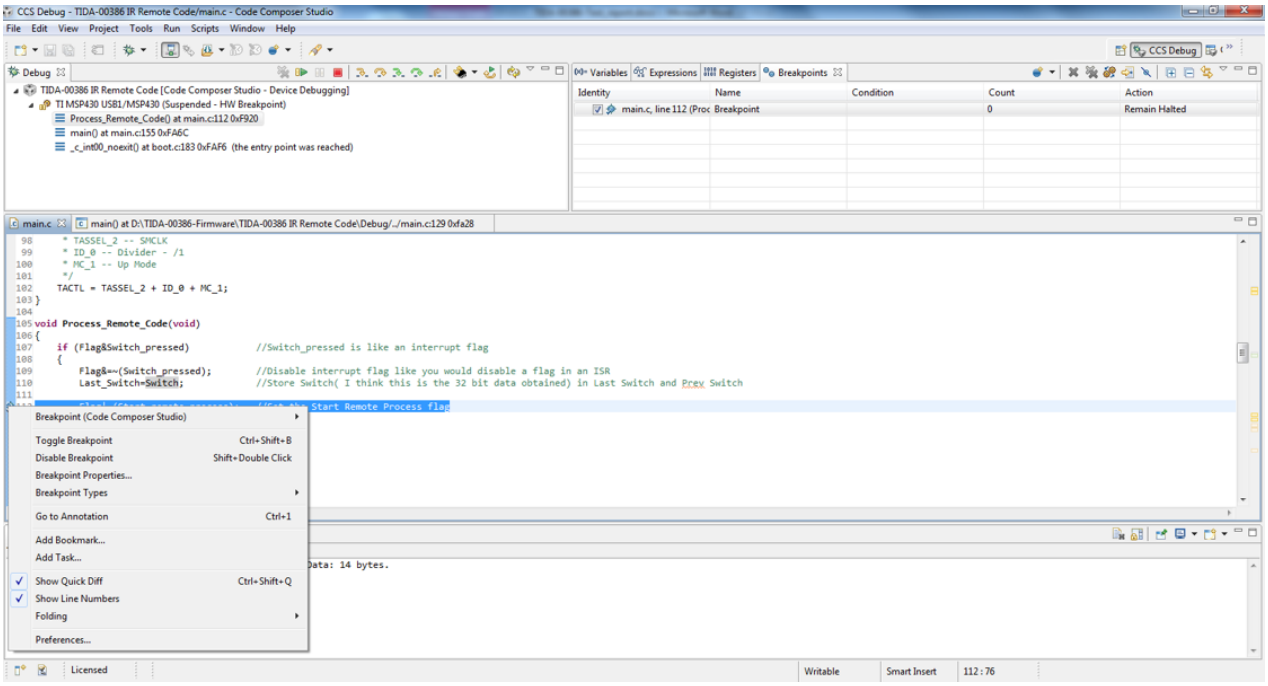


Figure 16. Changing Remote Codes in Software—Step 8

9. Navigate to the *main.c* file under the main taskbar pane and change the key codes at line 64 and 65. Re-flash the new code as Step 3 and Step 4 outline. The new code is now ready to use for speed control with the remote (see Figure 17).

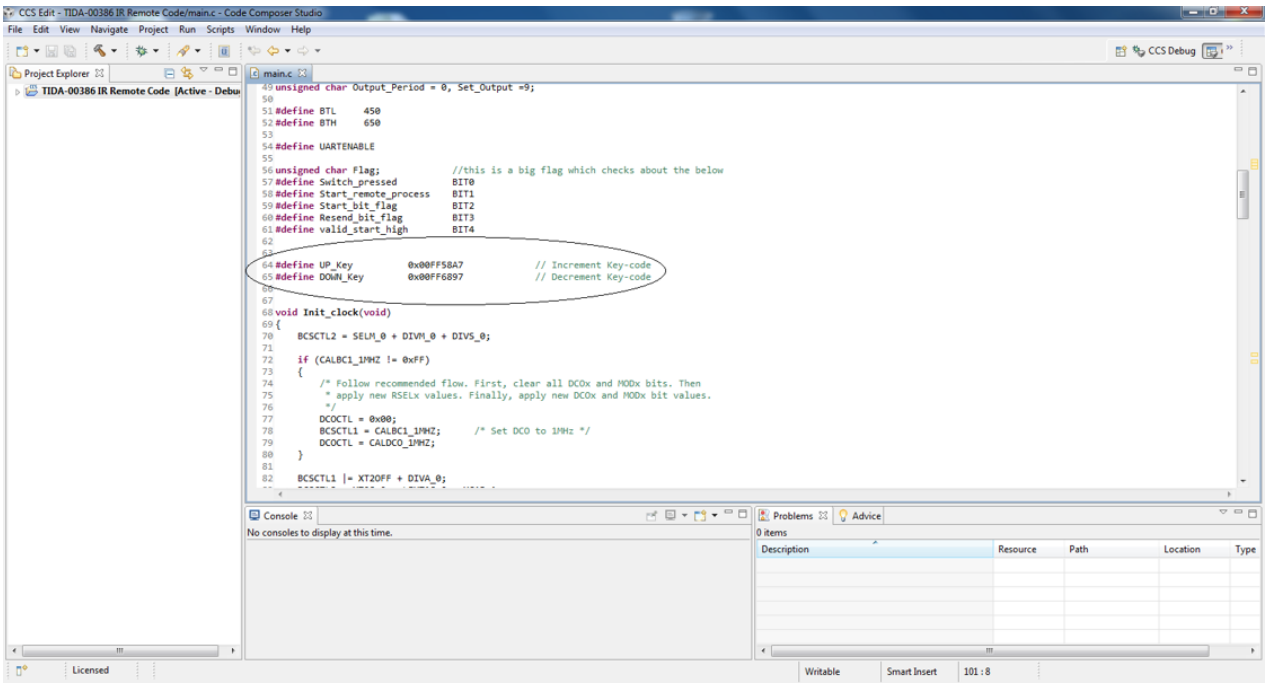


Figure 17. Changing Remote Codes in Software—Step 9

7 Test Setup

Testing of the TIDA-00652 design was performed with a resistive load on the buck PFC converter. Figure 18 shows the block diagram of the test setup with a resistive load.

Testing of the TIDA-00652 design was also performed with a fan load. Figure 19 shows the block diagram of the test setup with a fan load.

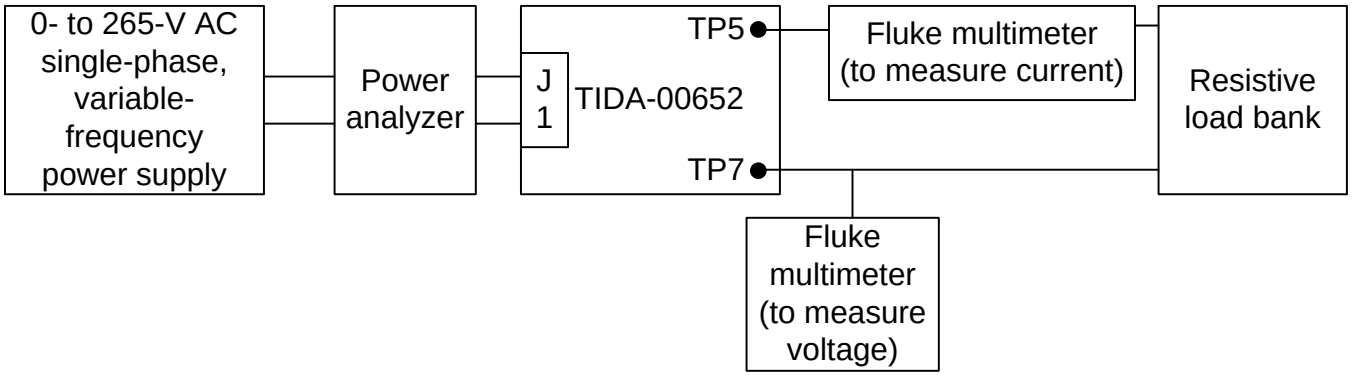


Figure 18. Block Diagram of Test Setup With Resistive Load

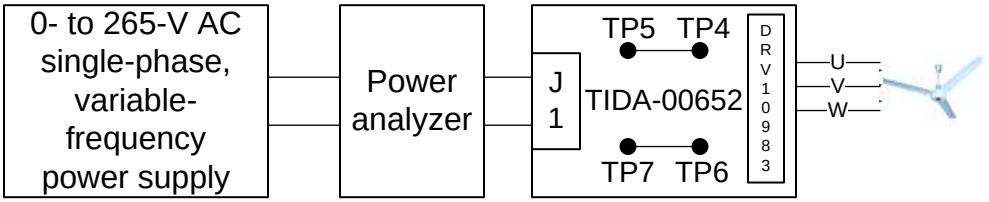


Figure 19. Block Diagram of Test Setup With Ceiling Fan Load

8 Test Data

8.1 Results With Resistive Load Connected to Power Supply

Figure 20 shows the output power versus the efficiency graph of the AC-DC power supply. Figure 21 shows the output power versus the input current THD curves.

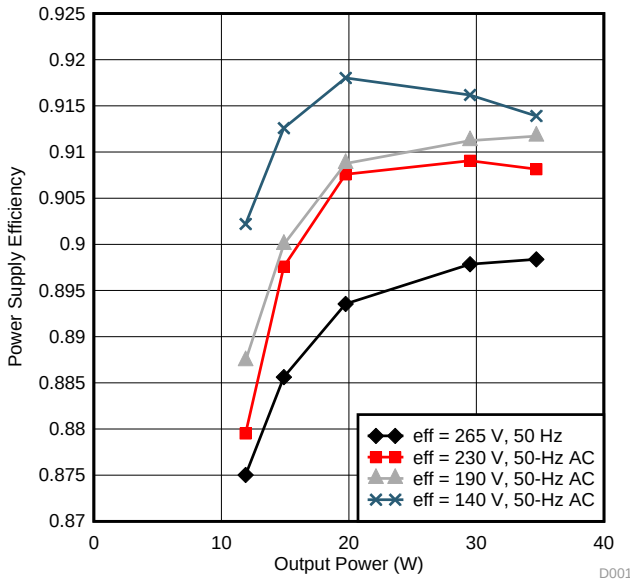


Figure 20. Power Supply Efficiency versus Output Power With Resistive Load

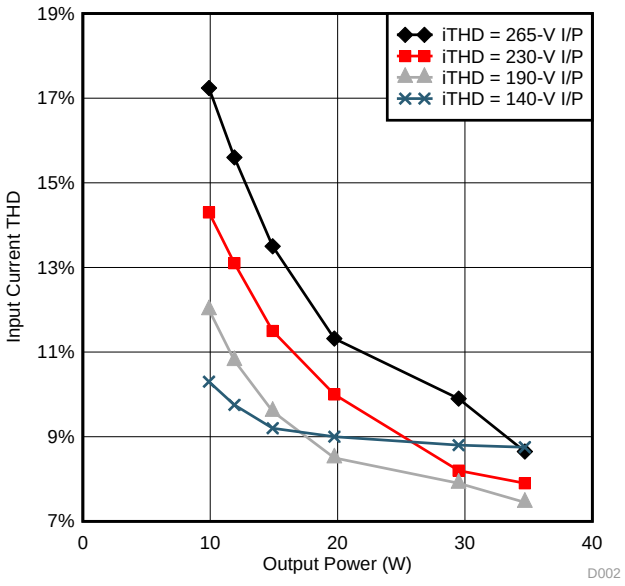


Figure 21. Input Current THD versus Output Power

Figure 22 shows the output power versus the input power factor curves.

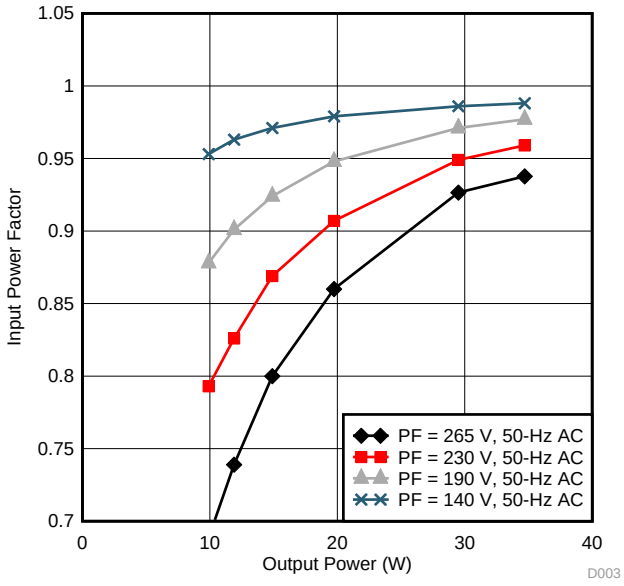
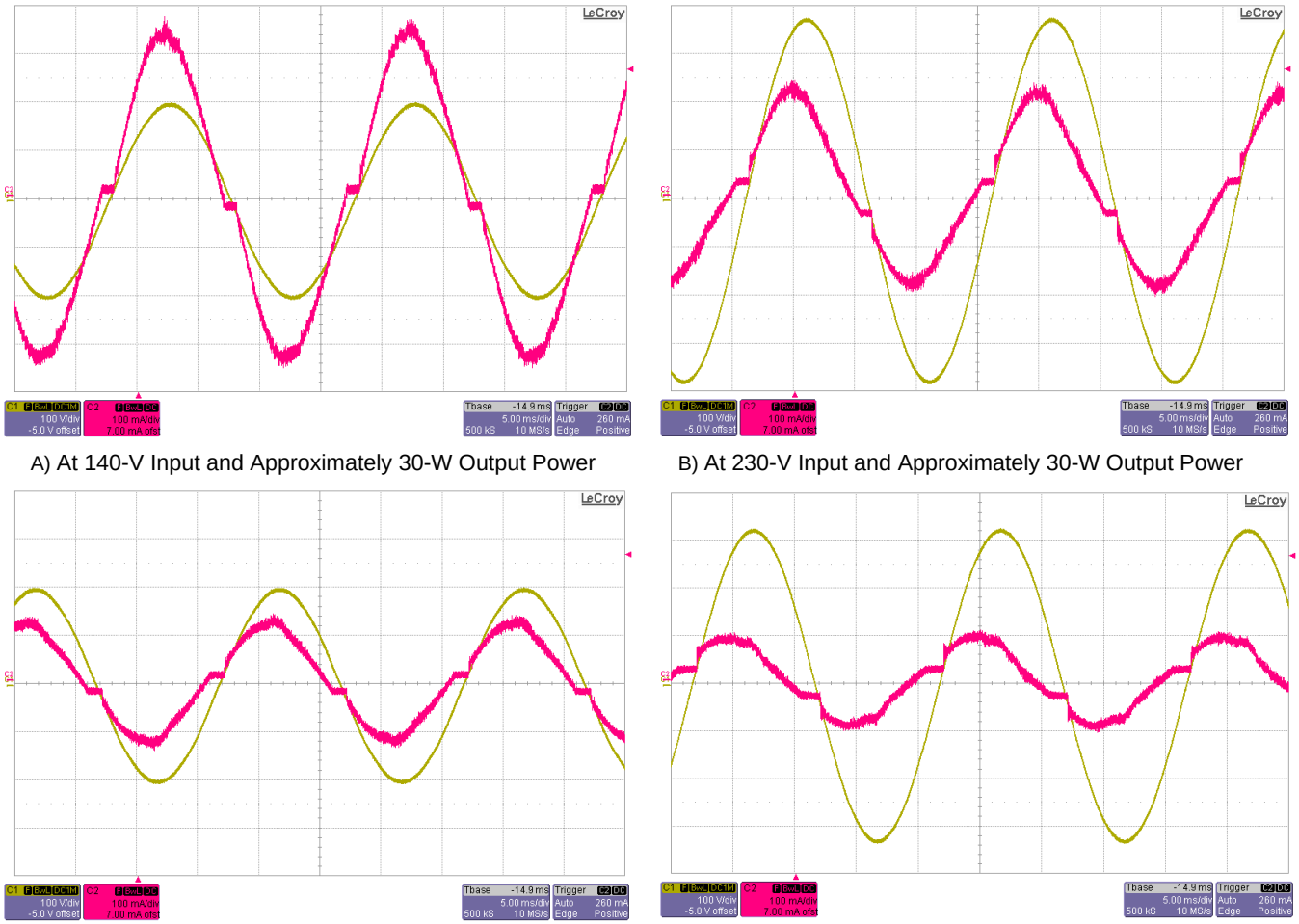


Figure 22. Power Factor versus Output Power

Figure 23 shows the output power versus the input power factor curves.



A) At 140-V Input and Approximately 30-W Output Power

B) At 230-V Input and Approximately 30-W Output Power

C) At 140-V Input and Approximately 10-W Output Power

D) At 230-V Input and Approximately 10-W Output Power

Figure 23. Power Factor versus Output Power

8.2 Results With Fan Load

Figure 24 shows the input power versus the speed with the power supply driving the DRV10983 device, which is subsequently driving a ceiling fan load. This ceiling fan is the same type of fan that the predecessor design TIDA-00386 has used for testing. Because of the time varying nature of output power, obtaining reliable efficiency data under a fan load is not considered possible. The user must rely on the test results with a resistive load for AC-DC converter efficiency. Figure 25 shows the speed versus the input current THD curves.

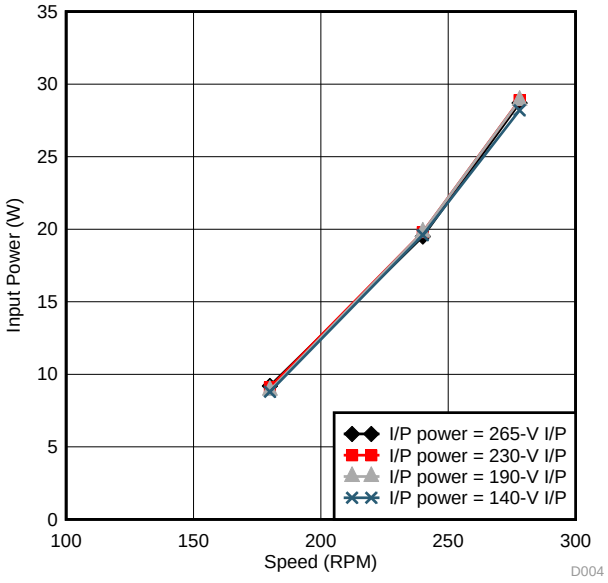


Figure 24. Input Power versus Fan Speed

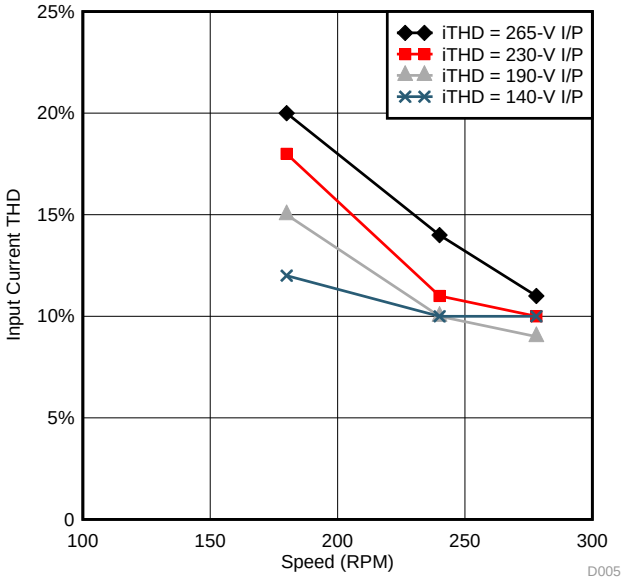


Figure 25. Input Current THD versus Fan Speed

Figure 26 shows the speed versus the input power factor curves.

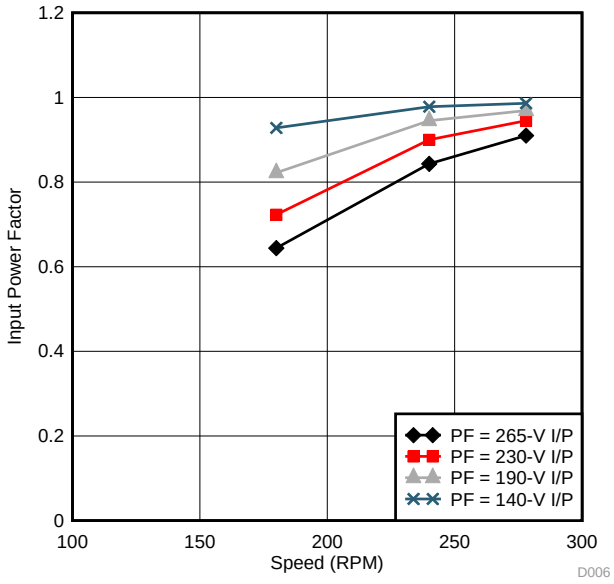


Figure 26. Input Power Factor versus Speed

Figure 27 and Figure 28 show the front and rear thermal images of the board working with the fan load at an ambient of 22.5°C. These images are produced while operating at an input voltage of 230–V AC and the fan running at 280 RPM.

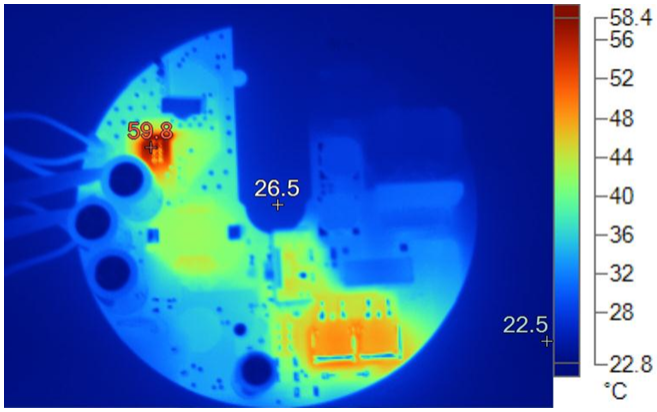


Figure 27. Thermal Image of Front View of Board While Running Fan Load at 280 RPM

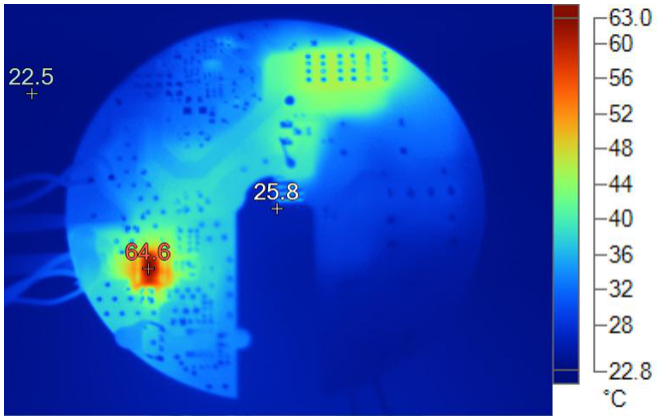


Figure 28. Thermal Image of Back View of Board While Running Fan Load at 280 RPM

9 Design Files

9.1 Schematics

To download the Schematics for each board, see the design files at TIDA-00652.

9.2 Bill of Materials

To download the Bill of Materials (BOM) for each board, see the design files at TIDA-00652.

9.3 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00652.

9.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00652.

9.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00652.

9.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00652.

10 Software Files

To download the software files for this reference design, see the link at TIDA-00652.

11 References

1. Texas Instruments, *Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations*, SEM1900 - Topic 4 Power Supply Design Seminar (SLUP264)
2. Texas Instruments, *Buck PFC Controller*, UCC29910 Datasheet and Application Notes (SLUSAK8)
3. Texas Instruments, *BLDC Ceiling Fan Controller with Sensor-less Sinusoidal Current Control, TIDA-00386*, TIDA-00386 Test Results (TIDU699)

12 About the Author

KRISHNA DORA is a Systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Krishna brings to this role his extensive experience in power electronics and power systems design. His experience ranges from sub 100-W power supplies to 750-KVA UPS systems. Krishna has hands-on development experience in the field of power electronics for space applications, industrial UPS systems, Photovoltaic inverters, and welding power supplies. Krishna earned his Master of Technology in Power Electronics and Power Systems from The Indian Institute of Technology Mumbai.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2015) to A Revision	Page
• Changed title	1

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