Non-linear Slope Compensation of Peak-Current-Mode-Control Switch-Mode-Power-Supplies: An Intuitive Approach

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Current Mode Control, CMC, has become a preferred pulse-width-modulation scheme for switch mode power supplies. This is due to the evolution of IC technologies that allow merging control circuitry with power switches having increasingly higher rated operating currents. The integration of the power switches and the adoption of CMC combine to provide for greater ease of use of a single converter solution across a broad range of applications. Prior to the integration of the power switches, the primary challenges for the CMC designer were the conflicting requirements of accurate current sensing and negligible power loss of the current sense element. These issues are addressed with continual improvement of the sense amplifiers that share the same monolithic circuit with the power switches. The primary advantage to the end user of CMC is simplified system loop compensation. In the simplest form, a single compensation capacitor, Cc, and resistor, Rc, are selected that cancel the predictable pole created by Co and Ro. The resultant switcher's loop acts as a single pole system. Also, line regulation or audio-susceptibility is also inherently excellent with CMC.

Peak current mode control is an extension of classical voltage mode control with the primary difference being the addition of a second loop, where the value of Pulse Width Modulation, PWM, is directly controlled by the peak inductor current for each switch cycle. Mathematical analysis is critical to the modeling and the proper design of CMC. The models are available from several excellent sources [1-4]. The equations used for the waveforms included in this presentation are summarized in an appendix. The goal of this article is to explain the CMC function and the requirements for stable operation without extensive use of equations. Graphical representations derived from the basic CMC circuit equations will

provide an intuitive understanding of the characteristics of CMC that is often lost with mathematical derivations alone.

The information is divided into four sections that provide an overview of basic CMC circuits, a series of inductor current waveform plots for demonstrating the need for ‘slope compensation’, plots of inductor current control for various values of input voltage and slope compensation, and a comparison of the stability of linear and non-linear slope compensation.

1. Basic Block Diagram of Peak CMC in PWM DC-DC Converters

In general, for fixed frequency DC-DC converters, a PWM pulse controls the time duration for which the inductor is energized within each switch period. CMC, in the simplest terms, compares a slow moving output voltage error signal to the relatively fast changing inductor current. The inductor current sense signal can be converted to a ‘sense’ voltage signal for a voltage comparator based CMC design, a method commonly described in the literature. Alternately the error signal can also be converted to a current so that the sum of the three signal currents (error or control, current sense and slope compensation) can be summed at a common node for comparison by an inverter. The two approaches are equivalent. The current summing method is used in the following diagram.

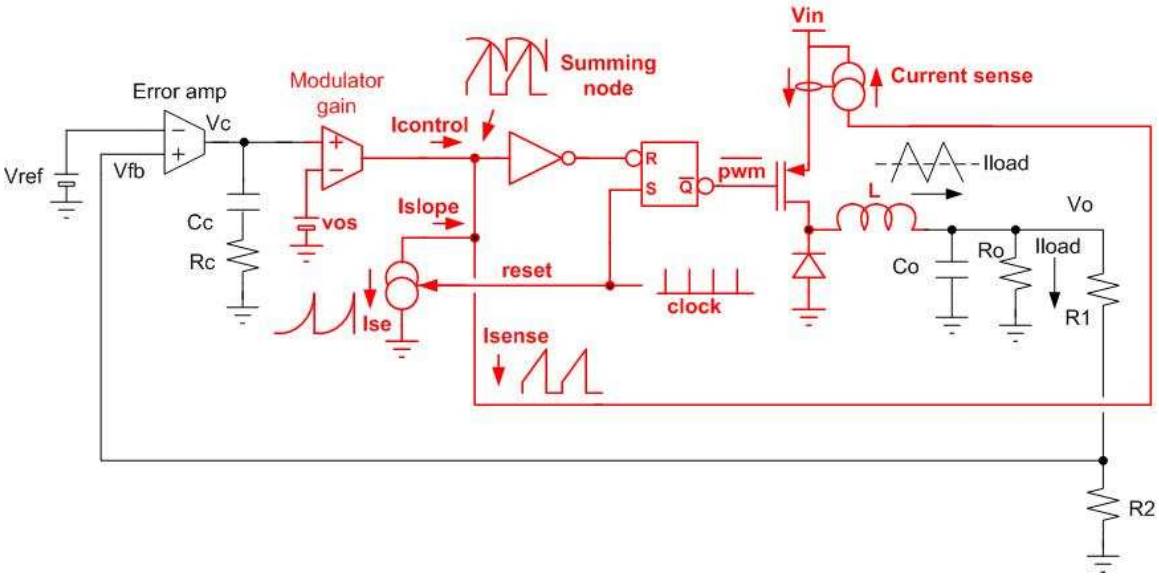


Figure 1. Basic block diagram of a current mode control buck power converter – CMC loop highlighted.

Figure 1 illustrates the entire control loop for a peak CMC buck DC-DC converter. The CMC component of the circuit is highlighted in bold and red. Within the CMC block, the RS block is central to the CMC timing. A fixed frequency clock sets the flip-flop which then turns on the power FET, energizing the inductor. This is the start of the PWM pulse. A current sense feedback signal terminates PWM when the energizing current in the inductor, reflected to the summing node via the sense circuit, reaches a peak control level, (Icontrol – Islope). Icontrol is directly related to the Vout error signal Vc. During the PWM 'on' pulse time, the power FET conducts and inductor current increases. The rate of increase for the inductor current during this period is defined as 'Su' and controlled by the difference between Vin and Vout, the voltage drop in the FET switch, and the value of L. Su increases with increasing (Vin-Vout) and decreases with increasing L. When the PWM pulse is terminated and the FET is turned off, the inductor current flows from the diode. The inductor current decreases linearly until the next cycle. The rate of inductor current change during this 'off' time is defined as 'Sd'. The waveform diagrams that follow will assume the voltage drop in the FET switch and the diode are negligible from the viewpoint of their effect on the shape of the waveforms. The diode is usually replaced with a low power loss synchronous FET switch in high efficiency systems. A

PMOSFET is shown in the diagram, but this switch could be an NMOSFET. In the steady state condition, the starting and ending inductor current within a switching period, Ts, are identical. The average inductor current is the DC-DC converter load current.

Note that the full period of inductor current does not need to be sensed, only the peak current. For this reason sensing the current in the power FET is equally effective as sensing the actual inductor current. Isense is typically 10uA to 100uA per ampere of inductor current.

Current mode control is desirable because the CMC loop in effect forces the peak current to be the same for each switch cycle as long as Vc is constant. Thus, the inductor in combination with the CMC loop in Figure 1 can be thought of as a current source. Unlike voltage mode control, the inductor L and output filter capacitor Co do not contribute a complex pole pair to the overall system loop. The removal of a power pole due to L in the CMC system loop removes the need for a corresponding zero in the overall system compensation network. A single RC network is adequate for optimal CMC system compensation, a significant reduction in complexity for tuning system performance.

Returning to the CMC diagrams, the non-CMC portion of the system loop generates the control voltage Vc and is highlighted in Figure 2.

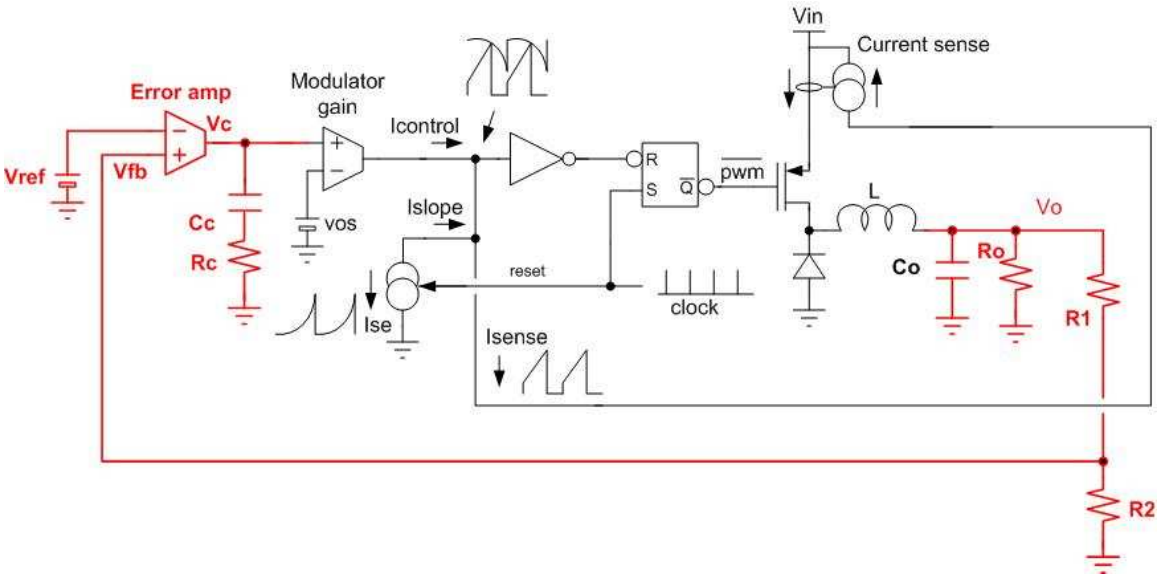


Figure 2. Basic block diagram of a current mode control buck power converter with highlighted voltage regulation control circuitry.

This ‘outside’ loop regulates Vout by providing the control signal Vc to the CMC loop that provides the PWM value that generates the desired output voltage that in turn satisfies the requirement for balance at the error amplifier’s input.

The next figure focuses on the basic summing node signals at the core of the CMC loop.

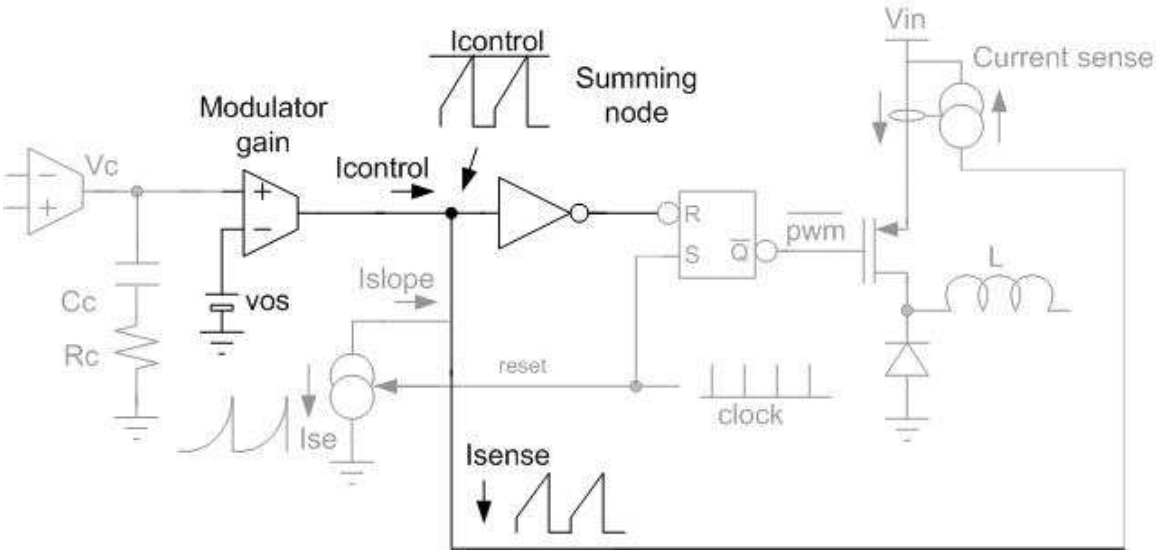


Figure 3. CMC summing node signal without slope compensation

To illustrate the basic CMC loop operation, the waveforms shown at the summing node in Figure 3 excludes the slope compensation current, Islope. Isense is representative of the inductor current during PWM high and returns to zero once Isense exceeds Icontrol and PWM is terminated. The peak current in the inductor is limited by the Icontrol signal which is directly controlled by the output of the error signal, Vc. For reasons that will be described in detail, CMC also requires the addition of Islope to the control signal and this additional signal is shown in Figure 4.

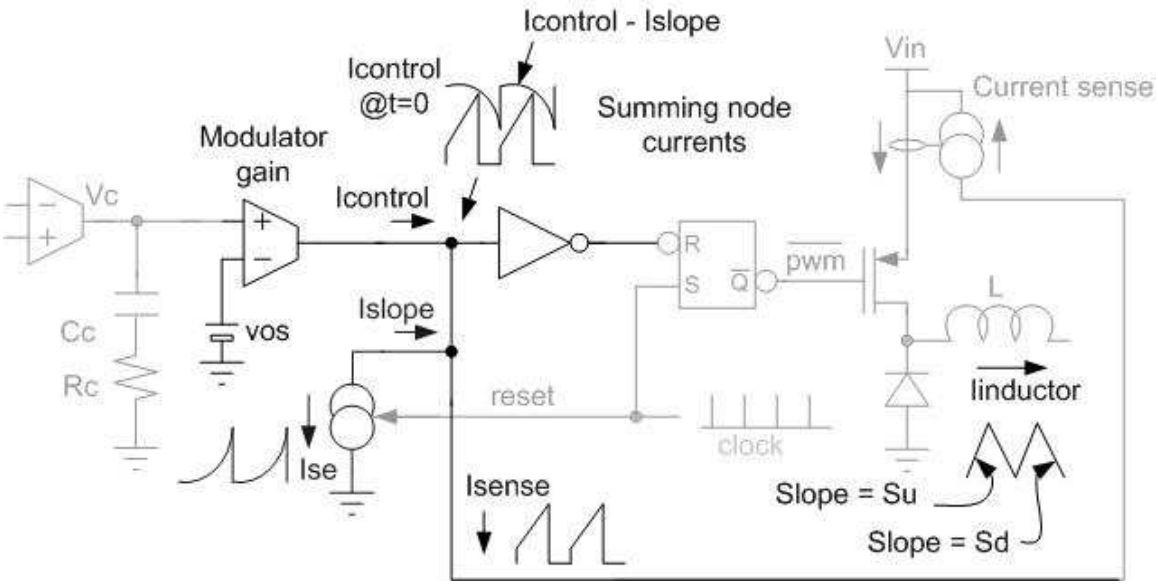


Figure 4. CMC summing node signal with slope compensation

The effect of Islope is to modify the slow moving Icontrol signal so that it has a downward slope for the duration of each switching cycle. Notice the change of the two summing node waveforms with the addition of Islope in Figure 4. This example illustrates a non-linear Islope signal. Islope is often a saw-tooth waveform with linear ramp. The difference between linear and non-linear slope compensation will be emphasized in analysis of the inductor current waveforms.

What role does Islope play in the operation of the CMC loop? This is the topic of the next section where the need for slope compensation is explained from a time domain perspective. Waveforms will be presented without slope compensation, and then with linear and non-linear slope compensation.

2. Time response of the CMC controlled inductor current to a step change in the inductor current.

Significant insight into the need for the addition of slope compensation to CMC is gained by observing the settling of the inductor current loop in response to a theoretical disruption of the inductor current. The exercise of analyzing the loops' recovery to a hypothetical disruption in inductor current demonstrates that it is possible, under certain regions of CMC operation, for the current (and PWM) to take excessive time to settle, or that settling is never achieved and the circuit falls into the sub-harmonic oscillation seen in improperly compensated CMC circuits.

The first three sets of plots show current settling for duty cycles of 25%, 50%, and 66% for a CMC loop that has no Islope. These are Figures 5, 6 and 7. In each case the load current or average inductor current is arbitrarily selected to be 2.5 Amps and the inductor ripple current is adjusted to be 30% of the load current. The desired value of switching frequency, duty cycle, Vout, and ripple current specify the value of inductor for each case. These three examples represent the same control circuit and input supply operating with three different feedback attenuation resistor settings providing three different values of Vout. The first is shown in Figure 5.

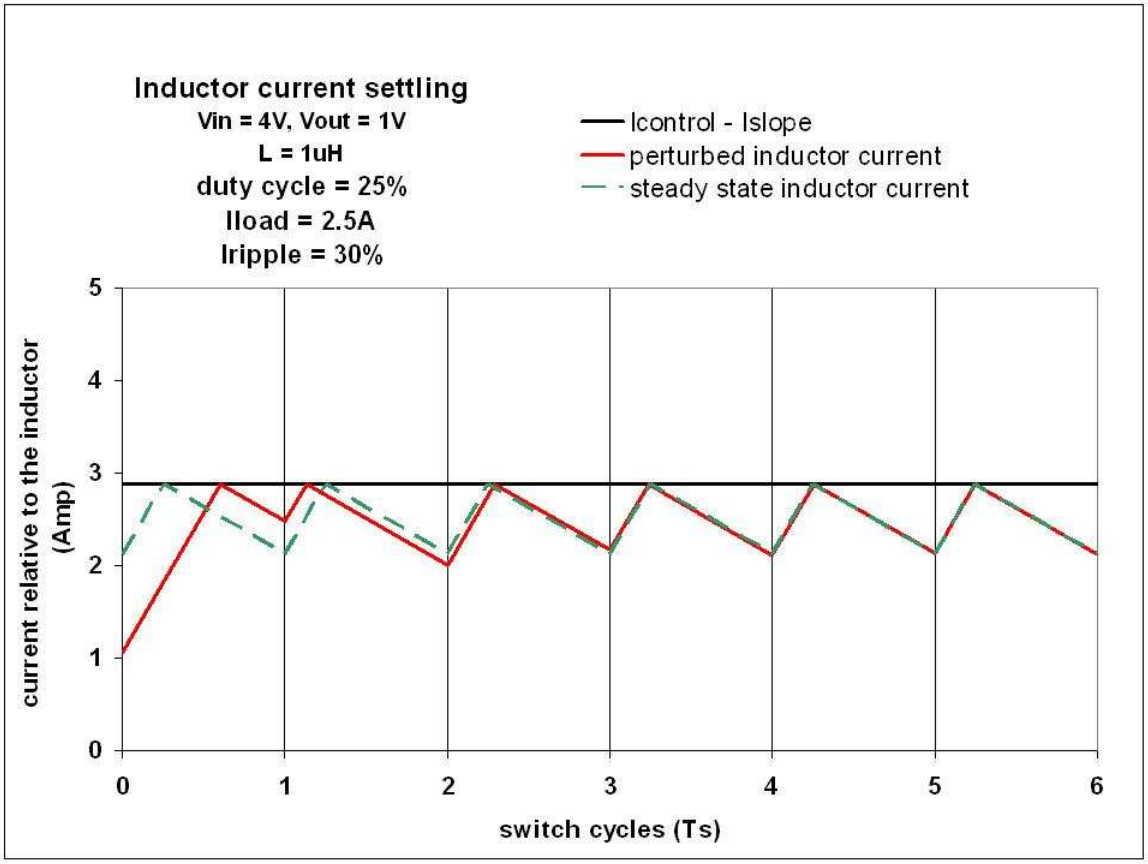


Figure 5. Response to perturbed inductor current - Duty cycle = 25%, Islope = 0.

For all the waveforms in this section, the green dashed triangle waveform is the expected steady state inductor current for the specific applications' duty cycle. The duty cycle in Figure 5 is 25%, therefore the power FET is conducting energizing current from Vin to the load via the inductor for approximately the first 25% of each switching cycle. The solid black lines in Figures 5-7 are the CMC control currents referenced to the inductor current. The control current determines the peak value of the sensed inductor current, so it is convenient to refer the control signal to the level of the inductor current in order to plot the two signals on the same scale. The third waveform in Figures 5-7 in this section drawn in solid red, is a hypothetical perturbed inductor current which at time zero is one half of the steady state inductor current. The perturbed inductor current is still constrained by Vin and Vout to have 'on' and 'off' period slopes of Su and Sd. For 25% duty cycle, the perturbation to the inductor current is able to converge to the desired steady state pattern within

several switching cycles. In the next figure, an application that operates at 50% duty cycle without slope compensation is examined.

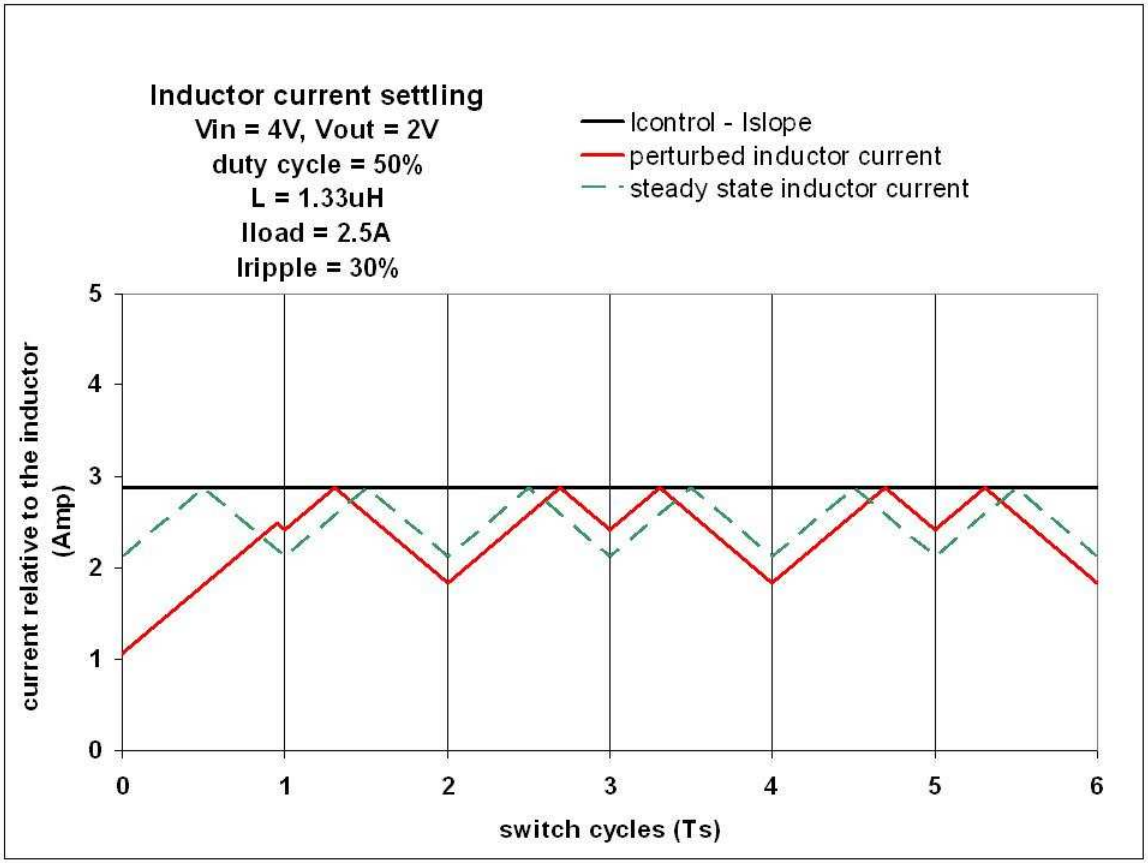


Figure 6. Response to perturbed inductor current - Duty cycle = 50%, Islope = 0.

The effective control current and the steady state current are the same as in Figure 5 and Figure 6. The load and ripple current are adjusted to the same target of 2.5 Amp and 30%. The value of Vin and Vout are adjusted for a duty cycle of 50% and the value of Su and Sd change accordingly. There is now a significant change in the ability of the perturbed inductor current to converge to the desired steady state inductor current. The resulting inductor current and PWM appear to be locked into alternating between two values of duty cycle with the average being 50%. This operation is commonly described as sub-harmonic oscillation because the pattern is often repeated at one half of the switching frequency. 50% duty cycle is the theoretical limit for stable CMC operation without any slope compensation.

Figure 6 illustrates how the instability can become even more significant for duty cycle greater than 50%.

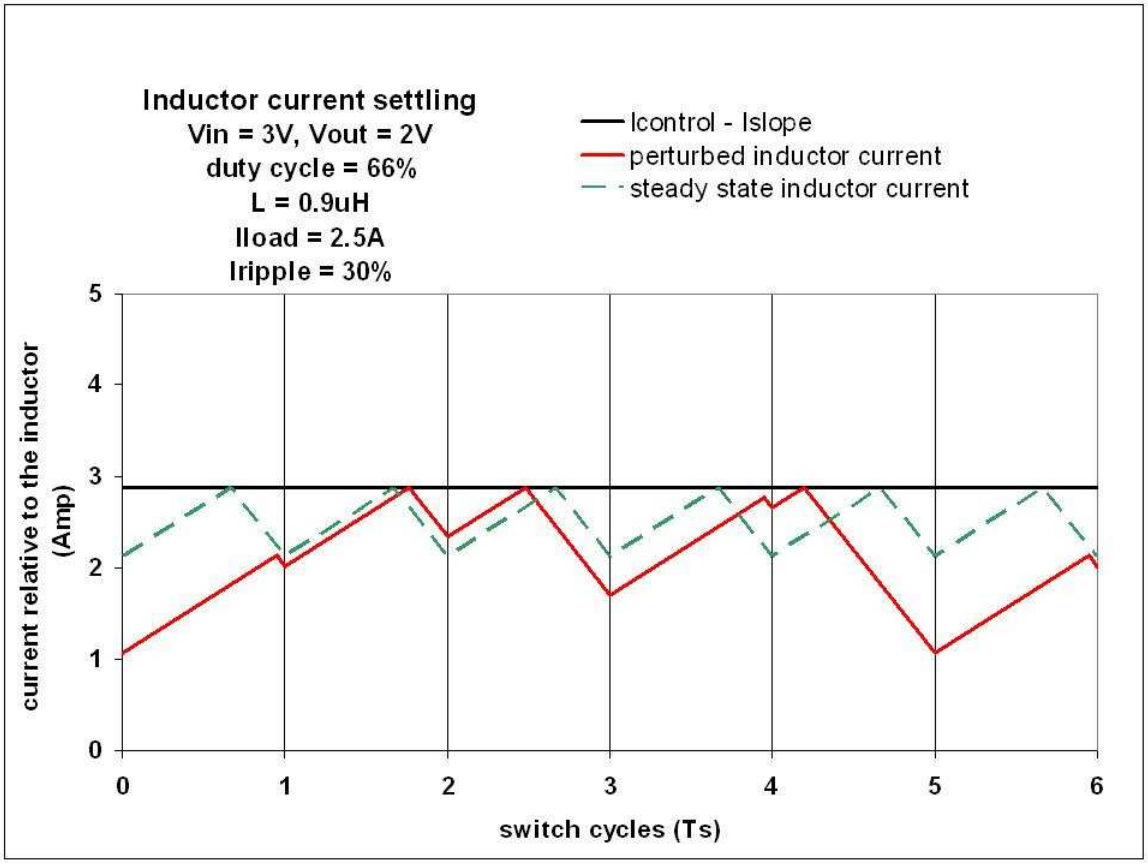


Figure 7. Response to perturbed inductor current - Duty cycle = 66%, Islope = 0.

Figure 7 has the same load and ripple current as before, however with Vout set to 2/3 Vin. Without any slope compensation, this particular example illustrates that the perturbed inductor current is unable to converge to the desired steady state pattern and its variation in PWM is even more erratic than in the 50% example. Mathematical theory predicts that this waveform will eventually settle to a sub-harmonic oscillation as well. Obviously this source of instability requires a remedy.

The next series of plots show the same power converter applications (fixed Vin, Vout, L, and load) with the addition of an artificial slope compensation signal, I-slope, to the summing node of the CMC circuit. How does this additional time dependent bias signal help

avoid the run away condition seen in Figures 6 and 7? Notice that without slope compensation for duty cycles greater than 50%, Sd has a greater magnitude than Su. This means that for perturbed currents, and for higher duty cycles, the downward current moves away from the control signal at a greater rate. The rate of divergence of the downward inductor current from the control signal becomes greater than the rate of convergence of the upward inductor current to the control current in this region of high duty cycle. Intuitively, the higher rate of divergence during the 'off' time leads to overall divergence of the inductor current and therefore instability. The up and down slopes of the inductor current can not be changed for a fixed application, but the apparent rate of convergence and divergence can be artificially modified. The solution for stability at higher values of duty cycle is to change the slope of the control signal to favor a lesser rate of divergence for the downward inductor current from the control signal.

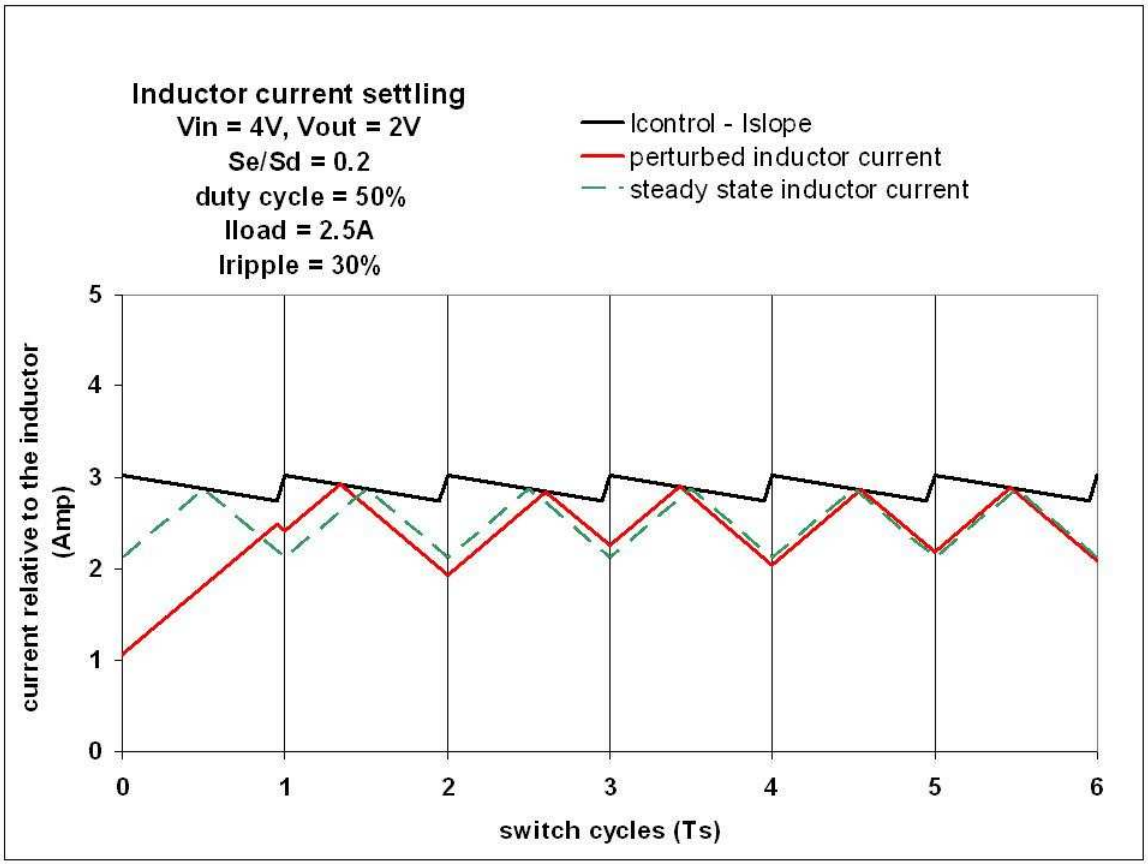


Figure 8. Response to perturbed inductor current - Duty cycle = 50%, Islope = 20% slope of Isense or Se = Sd/5.

In Figure 8, the control signal is modified by the addition of a linear Islope signal. Islope is subtracted from the Icontrol resulting in the (Icontrol – Islope) waveform in Figure 8. We will define the slope of Islope as 'Se'. Even this minor modification provides for a substantial improvement in the recovery time of the perturbed inductor current for 50% duty cycle. The question becomes how much slope compensation is required for stability in all applications? The relative ratio of Islope to inductor current needs to increase for higher duty cycles to have the same stabilizing effect. To illustrate this point, the value of Islope in Figure 8 is not acceptable at 75% duty cycle. See Figure 9.

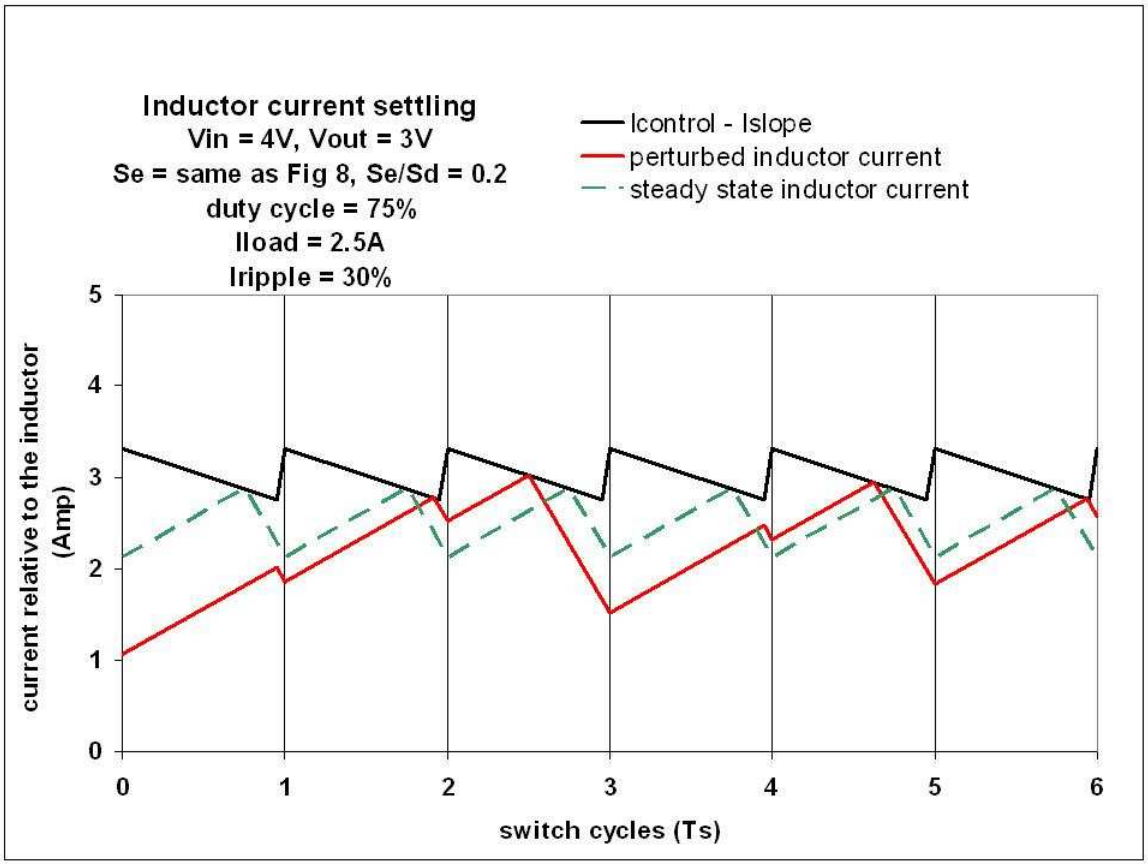


Figure 9. Response to perturbed inductor current - Duty cycle = 75%, Magnitude of Islope is the same as for Figure 8.

Differing contributions of slope compensation are needed for different duty cycle applications, (different values of Vout), and this leads to the next level of compensation technique, non-linear slope compensation. Non-linear compensation increases Islope as the duty

cycle increases. This concept is illustrated by the same perturbed inductor current versus time plots. First it is necessary to consider what is the proper ratio of Islope to Isense for a given duty cycle. Figure 10 illustrates a very special value of Islope, the case where Islope is the same as the downward slope of the inductor current; Se = Sd.

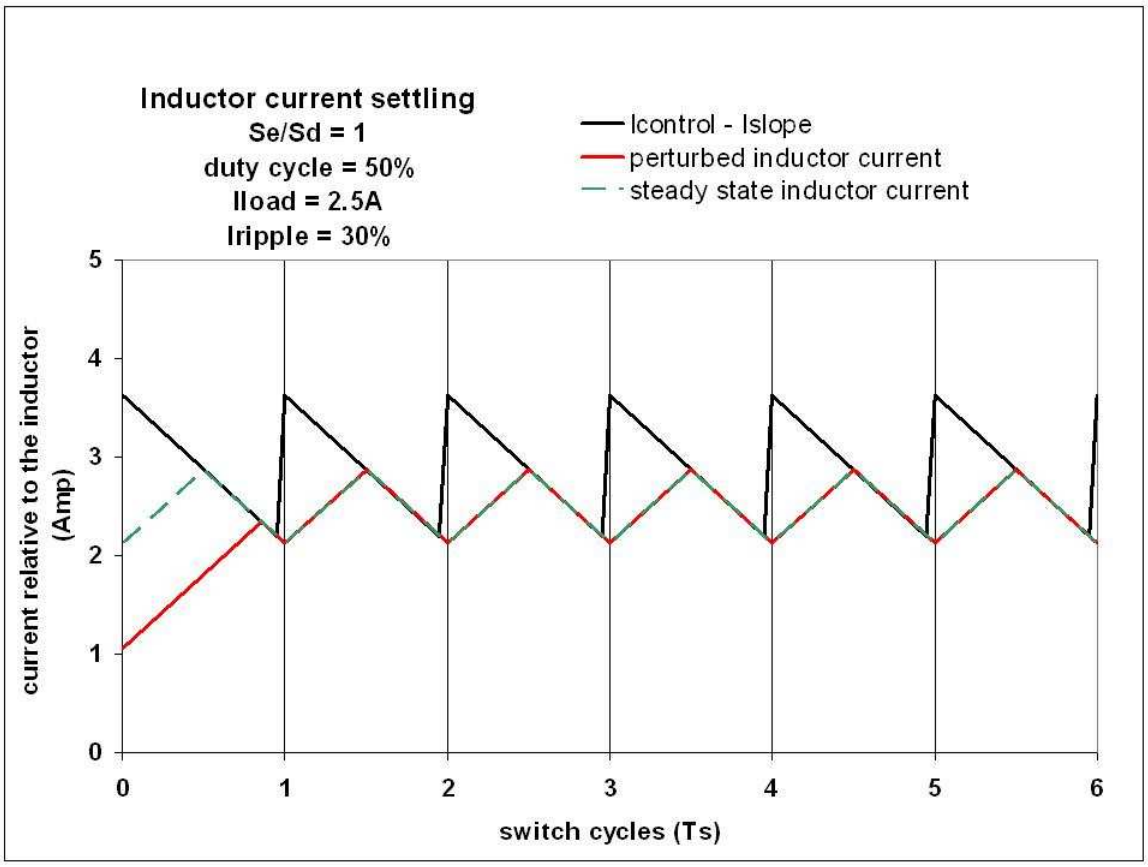


Figure 10. Response to perturbed inductor current - Duty cycle = 50% and the magnitude of Islope is the same as the downward slope of Isense.

The result of the special case in Figure 10 is that the perturbed inductor current settles in one switching cycle. This condition is often called ‘deadbeat’. With linear slope compensation and a fixed value of Se, this condition can only occur with one value of Vout and one value of inductor. With non-linear slope compensation, deadbeat can occur for a wide range of Vout settings.

3. Investigation of Peak CMC Waveforms Across a Wide Range of Vin

Assuming a typical application where Vout and L are fixed how does the variation of Vin affect slope compensation? Analyzing this with time plots of steady state inductor and control signals is a good vehicle for visualizing the operation of slope compensation in specific applications.

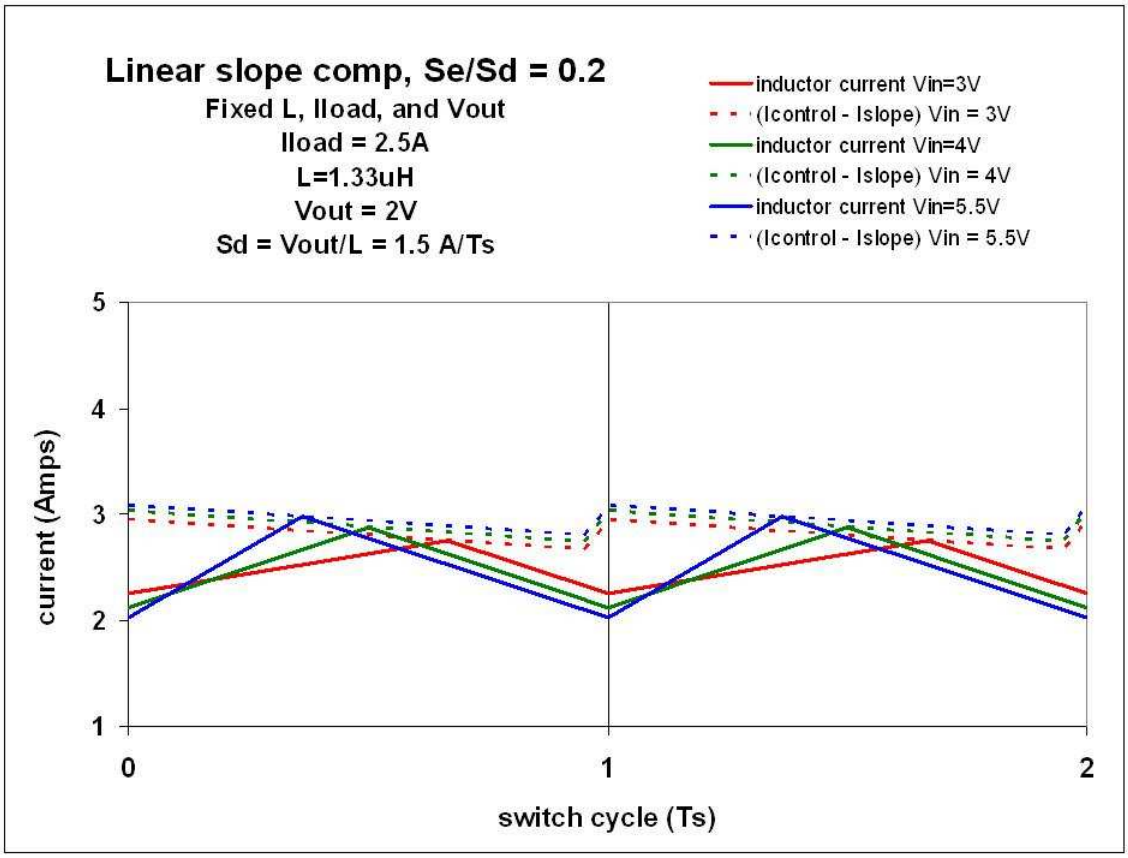


Figure 11. Inductor and linear compensated control current for fixed Vout, L, and Iload - low level of Se (slope of Islope) relative to Sd (slope of inductor current on down slope).

In Figure 11 the inductor current waveforms are shown for three values of Vin. Notice that the downward slope of the inductor current, Sd, is constant for the fixed value of inductor and Vout, independent of Vin. The dotted lines represent the values of (Icontrol – Islope) referenced to their respective inductor current waveform. Any change in Iload causes this cluster of waveforms to simply shift together up or

down. There is no apparent change in these waveforms within the CMC loop with Iload, however the load does have an effect on the converter's output pole (Co, Ro from Figure 1) and the overall gain of the CMC modulator. These two parameters are components that enter into the overall compensation of the system loop. The particular waveforms in Figure 11 assume a low value of linear slope compensation. The downward slope of (Icontrol – Islope), Se, is significantly lower magnitude than Sd. From the previous series of plots illustrating the settling of perturbed current, it is probable that the Vin = 3V condition will be unstable with this low level of slope compensation. Another important observation seen with this particular case of low Se is that a small disruption of the control signal results in relatively large change of duty cycle. Greater Se therefore results in much lower system sensitivity to injected noise.

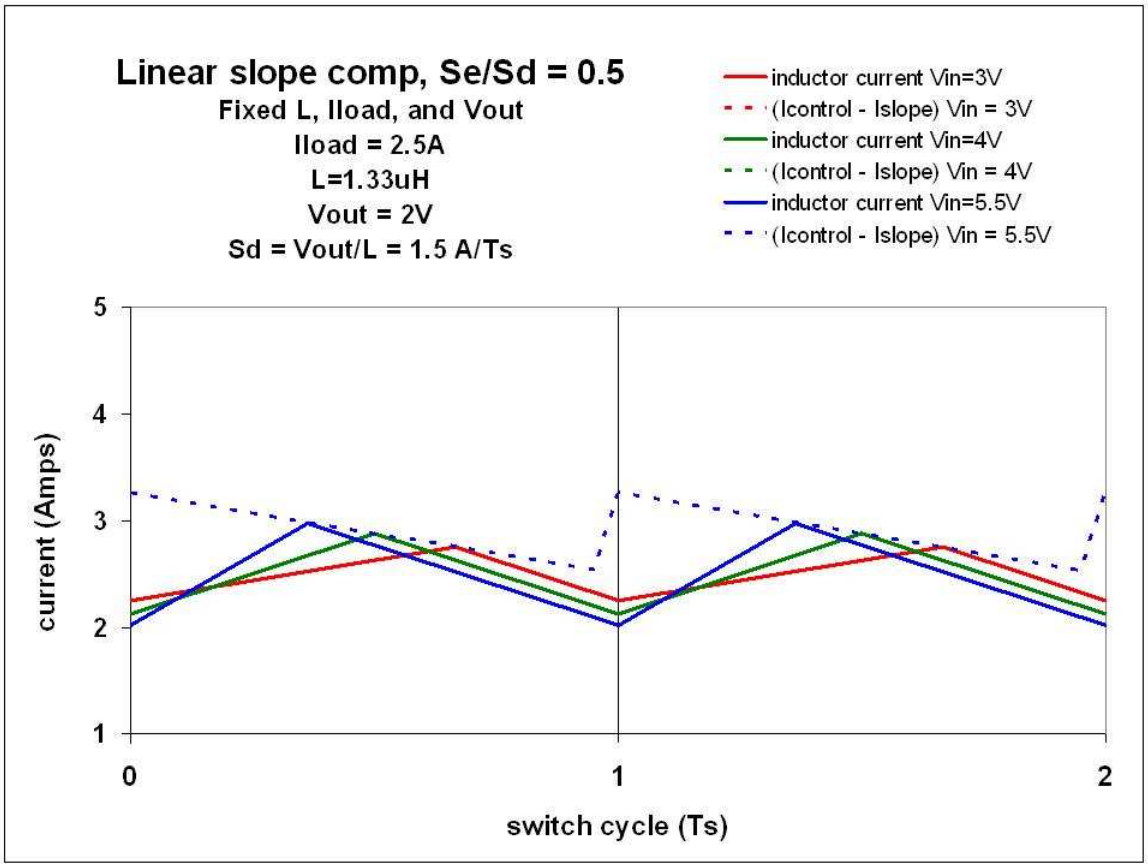


Figure 12. Inductor and linear compensated control current for fixed Vout, L, and Iload. Linear slope comp that provides zero line regulation.

Figure 12 assumes the same set of operating conditions as in the previous figure, however with greater Se. This illustrates a special case of slope compensation. The slope of Se is equal to one half of the downward slope of the inductor current. The three (Icontrol – Islope) waveforms nearly lie on top of each other. In other words, changes in Vin, which result in a simultaneous change of duty cycle and peak inductor current, require no change in the (Icontrol – Islope) signal. No change in Icontrol requires no change in the error amplifier's output and therefore no change in feedback or output voltage. This provides for no systematic source of line regulation error, even with finite error amp gain. An additional note of interest for Se/Sd = 0.5 is this is the minimum value of Se that assures stability for all duty cycles. Another special value for slope compensation is observed in Figure 13.

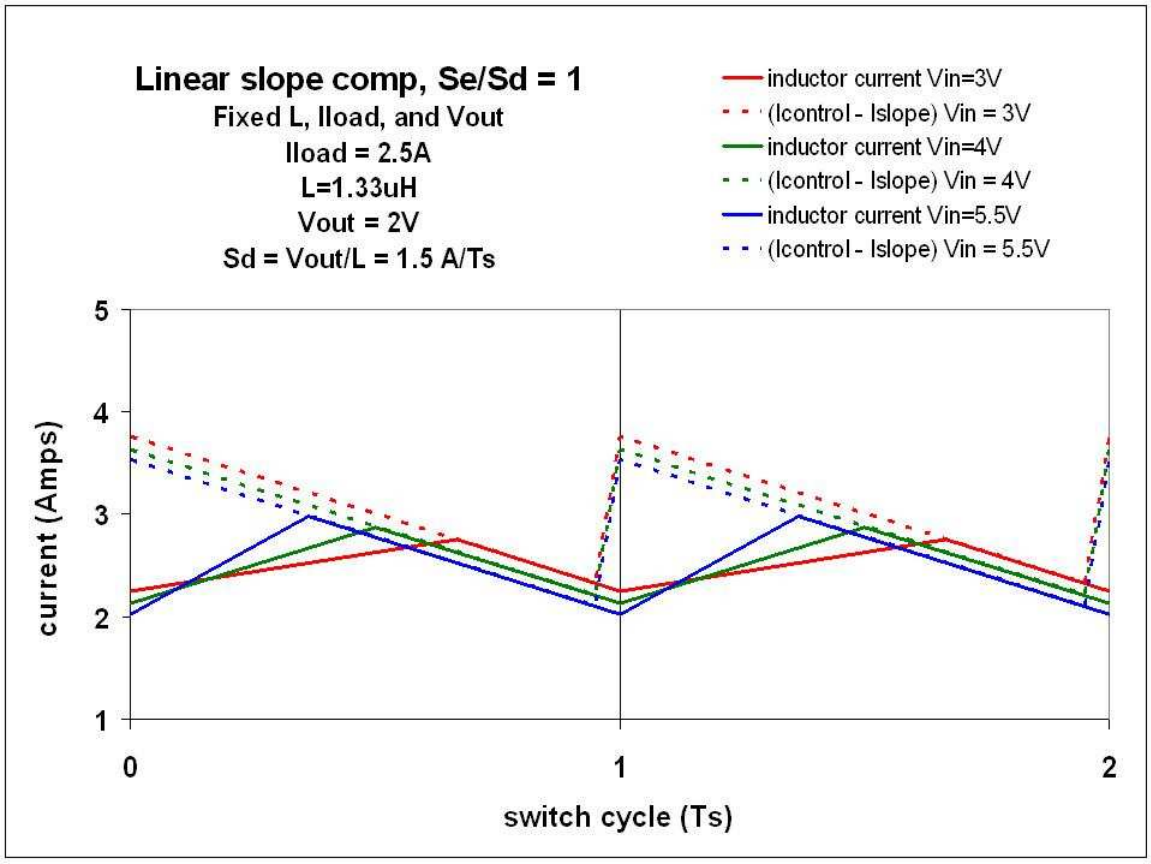


Figure 13. Inductor and linear compensated control current for fixed Vout, L, and Iload. Linear slope compensation that provides deadbeat control.

In Figure 13, the slope compensation is increased again, now to Se/Sd = 1, and the other special case termed deadbeat is achieved for all values of Vin. Because the slope of (Icontrol – Islope) matches the downward slope of the inductor current, the inductor current will recover from a disruption at the first PWM termination. The inductor's downward slope will instantaneously align to the desired steady state value. For linear slope compensation, if deadbeat is achieved for a particular Vout and L, it is achieved for all values of Vin.

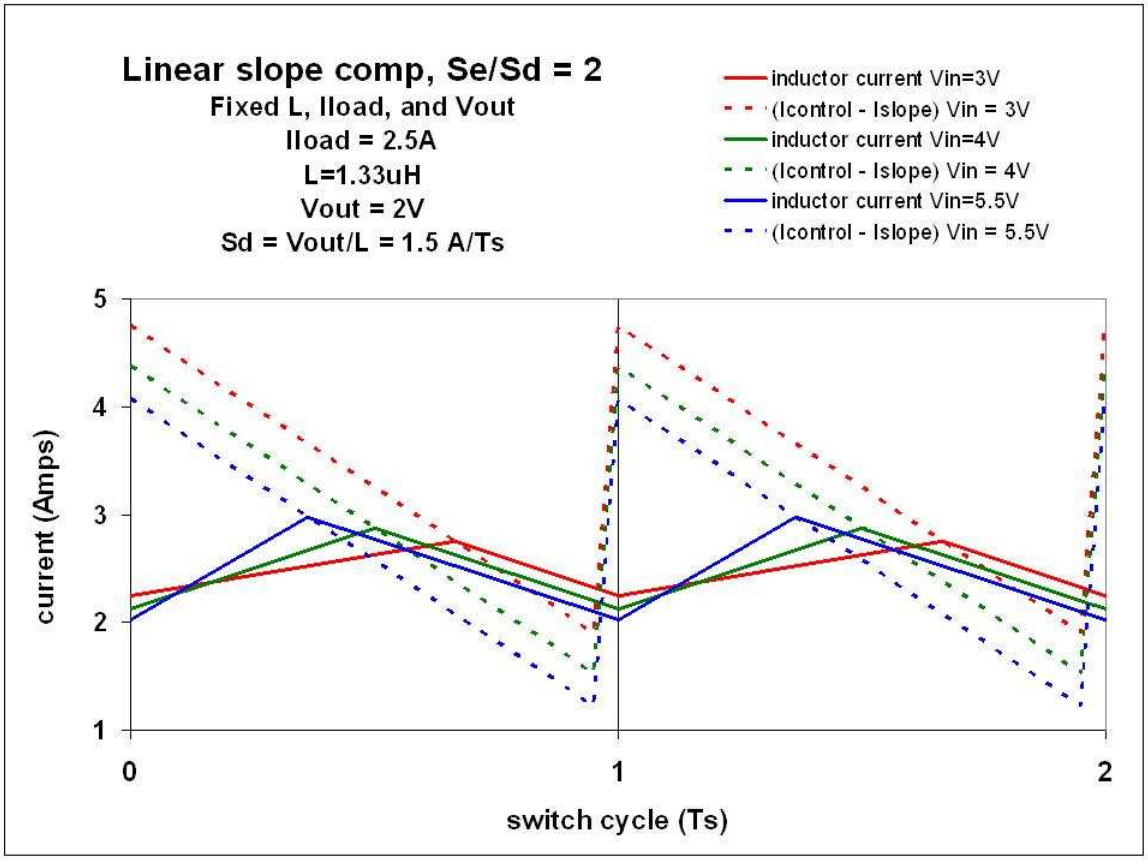


Figure 14. Inductor and linear compensated control current for fixed Vout, L, and Iload. High level of linear slope comp

Figure 14 continues the trend of this series of plots with the slope compensation increasing to even greater downward slope. The general trend is that the magnitude of the control current, the value of (Icontrol – Islope) at the start of the switch cycle, must increase as Se increases. The drawback is the dynamic range of the control is compressed toward the high end of the signals' range. No additional benefit in stability is gained with excessive Se, in fact it is argued that

in the extreme, the loop approaches a hysteretic mode of operation and the benefits of CMC are lost.

Next, the same current waveforms for the same series of set applications (fixed output voltages) with non-linear slope compensation are plotted. Ideally Se changes linearly with duty cycle as Vout is changed so a more constant Se/Sd ratio is maintained with change in Vout. The magnitude of Islope is derived by integrating this ideal Se which is a linear function of duty cycle. So the resultant non-linear Islope increases with the square of the duty cycle before it is subtracted from Icontrol.

Figure 15. Inductor and non-linear compensated control current for fixed Vout, L, and Iload. Low level of linear slope comp

In Figure 15, a low value of non-linear slope compensation is applied and all of the observations discussed in reference to Figure 11, where a low value of linear slope compensation is applied, still hold true. Instability will probably occur for Vin = 3V because this level of Se is marginal compensation for higher values of duty cycle. The sensitivity to noise is still greater than that for larger Se. Therefore these waveforms represent an inadequate level of slope compensation.

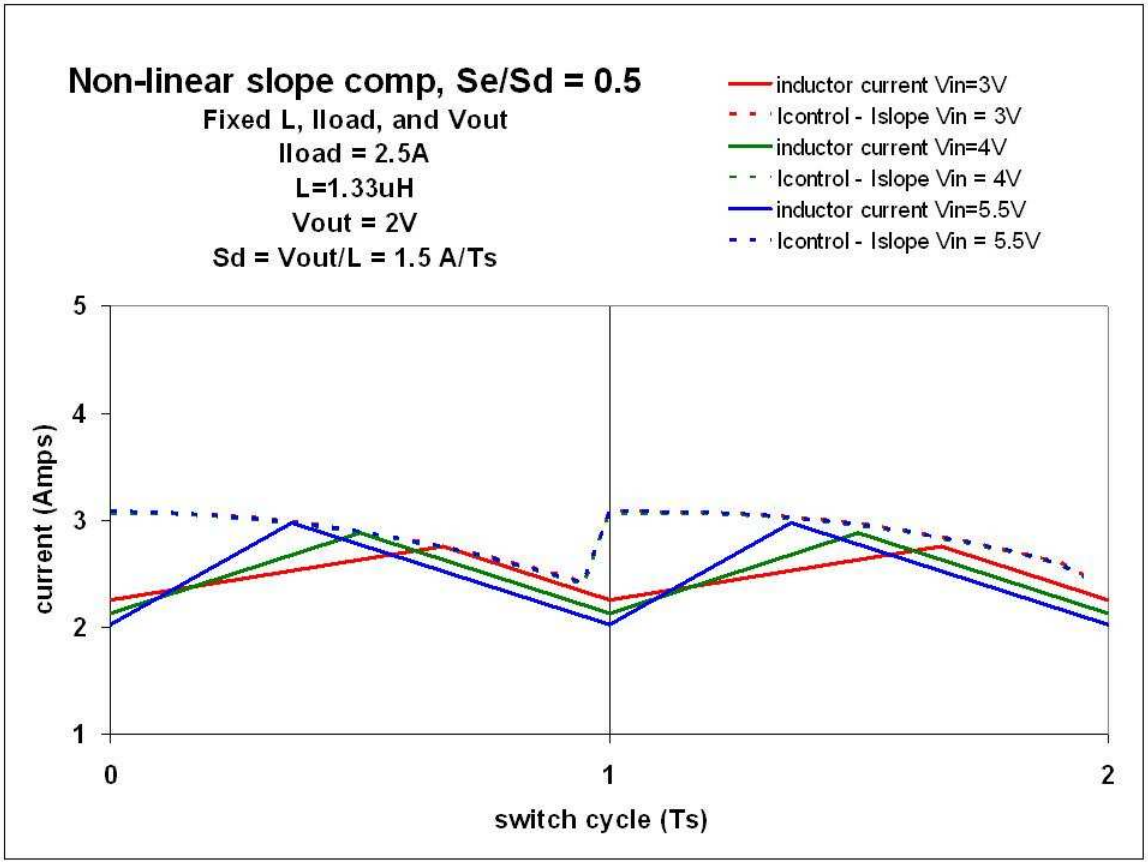


Figure 16. Inductor and non-linear compensated control current for fixed Vout, L, and Iload. Se/Sd = 0.5 at Vin = 4V and Vout = 2V.

The waveforms in Figure 16 have the appearance of no change in (Icontrol – Islope) for the full range of Vin related duty cycles and is similar to the example in Figure 12 for linear slope compensation and Se/Sd=0.5, set at the mid-point of the Vin and Vout ranges. The locus of peak currents for all values of Vin is linear and therefore the non-linear slope compensation seen in Figure 16 is only an approximation of zero line regulation. However for this range of Vin (3V to 5.5V), the approximation of zero line regulation is close to ideal.

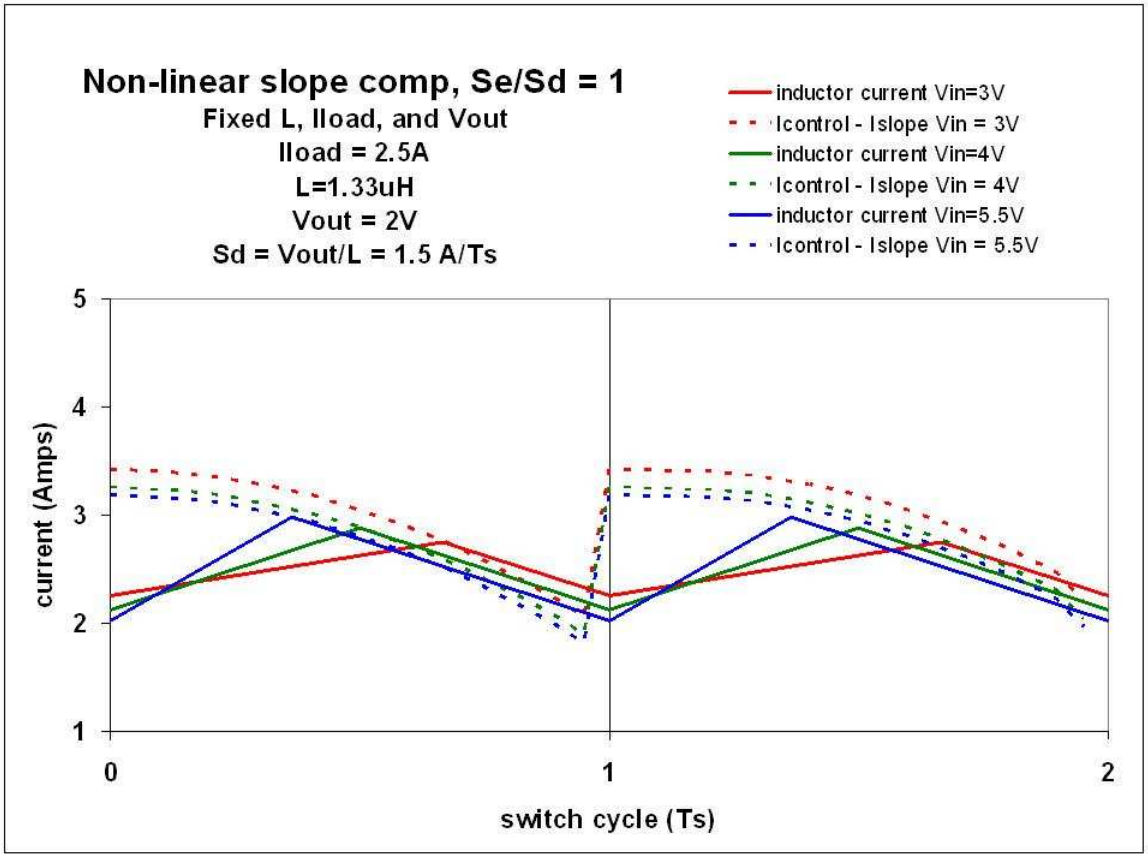


Figure 17. Inductor and non-linear compensated control current for fixed Vout, L, and Iload. Se/Sd = 1 at Vin = 4V and Vout = 2V.

The deadbeat condition for non-linear slope compensation is only met for one value of Vin. Figure 17 illustrates a slight deviation of the Se = Sd criteria for deadbeat at the high and low values of Vin. Linear compensation maintains deadbeat over Vin, however non-linear will be shown to be superior to linear when the effect of slope compensation is examined over the range of possible Vout values. This is the topic of section 4.

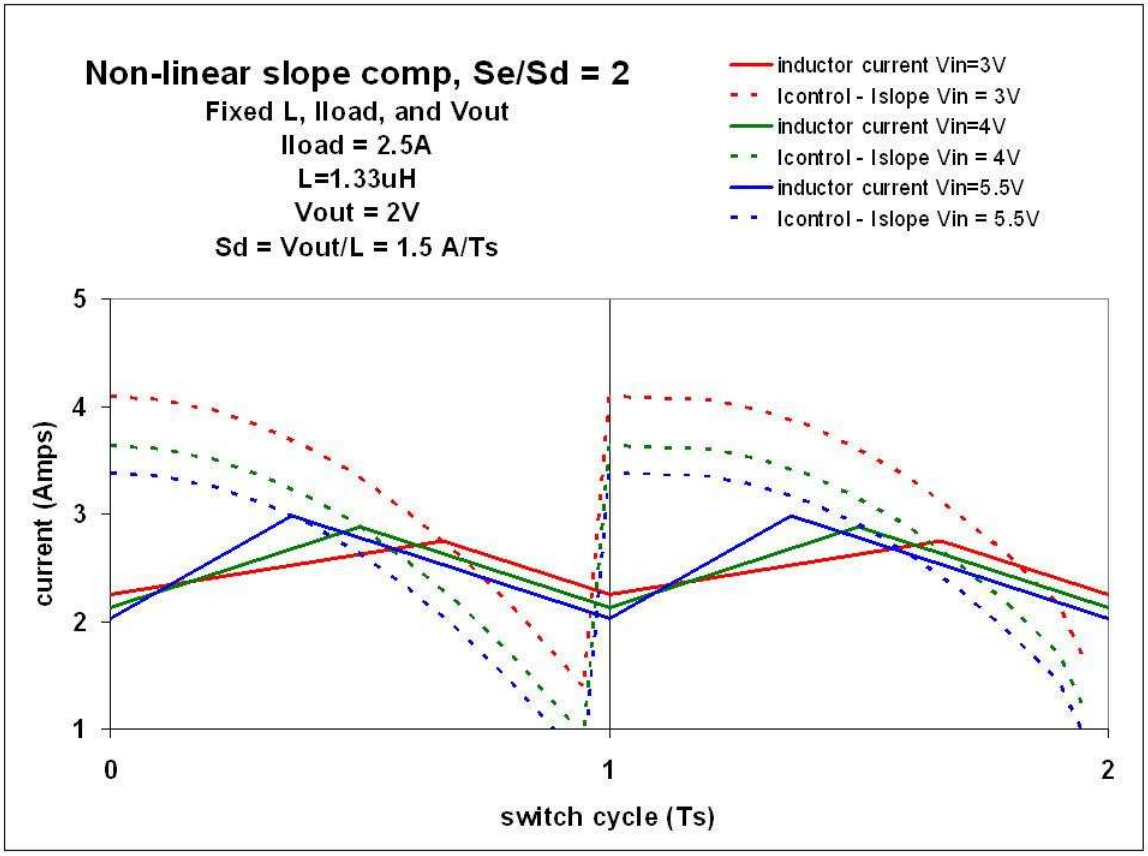


Figure 18. Inductor and non-linear compensated control current for fixed Vout, L, and Iload. High level of Se.

Figure 18 is a final look at the same three values of Vin for non-linear slope compensation with a high value of Se. One advantage of non-linear slope comp for high duty cycles and high Se is that the peak magnitude of Icontrol is less than in the linear case and therefore provides more dynamic range of the control signal and less opportunity for over-ranging Icontrol.

From this last series of plots where Vin is varied for a fixed value of Vout, the case for zero line regulation and the case for deadbeat over the full range of Vin is less than ideal for non-linear slope compensation and theoretically ideal for linear slope compensation. This section addressed the full range of Vin for one particular Vout. The argument for non-linear slope compensation requires reviewing the Se controlled parameters for the full range of Vout applications.

4. Comparison of Linear and Non-linear Slope Compensation across the Full Application Space

It is important to recognize that CMC acts as a sampling function. Detailed analysis of CMC sampling results in a complex pole pair located at one half of the switching frequency. Unlike the complex LC pole pair of voltage mode control, the CMC sampling poles are always at one half of the switching frequency and can not drift down with component selection. All complex pole pairs do have the danger of excessive gain peaking and rapid phase shift if not managed properly. Q is the common term for qualifying the amount of gain peaking. For example, a Q value of 1.5 indicates that the gain will peak by 50% near the pole frequency. High values of Q even at one half of the switching frequency can introduce instability into the system loop and therefore peaking is managed by the amount of slope compensation added to the CMC loop. The term 'Qs' is used to identify the peaking associated with the CMC sampling complex pair pole.

The value of slope compensation is one of many degrees of freedom effecting stability, or instability. The end users' ability to adjust Se complicates the implementation of the peak CMC integrated controller circuit. Therefore the magnitude of peak CMC Se is not usually adjustable by the user. It is simpler if the controller IC provides the most robust fixed value of slope compensation that best covers the full range of applications. Good engineering practice would suggest that the fixed value of Se be set at some ideal value near the center of the application space. As the same design is applied over the full range of rated Vout, deviations in parameters such as Icontrol dynamic range, line regulation, I-ripple, and Qs are balanced at the extreme limits of both Vout and Vin. The following plots will now compare linear and non-linear slope compensation operation at typical high and low settings for Vout. Examples of typical 5V and 16V rated converters are used for the analysis.

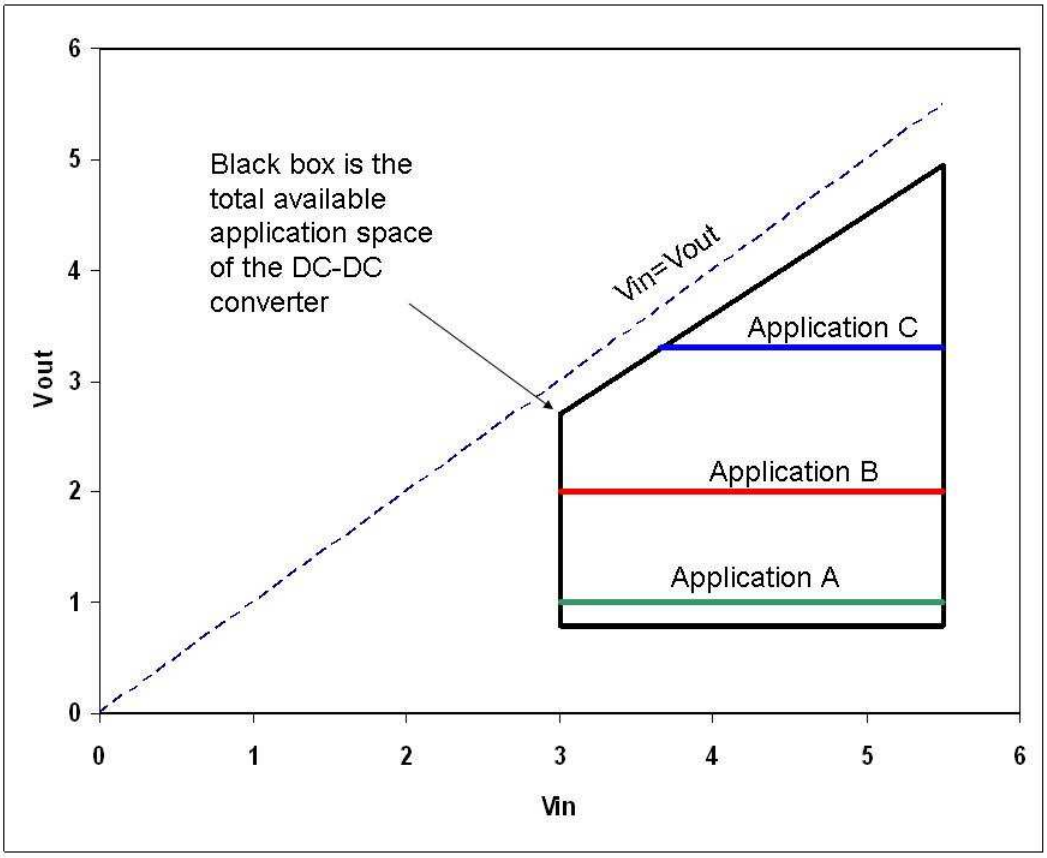


Figure 19. Total application space for a 5V DC-DC buck converter model and three specific applications (fixed Vout, and L) within the space.

Figure 19 is useful for visualizing the concept of application 'space' for a buck DC-DC power converter. The rated range of Vout and Vin for any DC-DC buck converter is bound by the maximum duty cycle limits along the top boundary, the minimum duty cycle and the value of the error amp reference voltage along the bottom, and by the minimum and maximum allowed Vin values on the left and the right sides of the box. Within this application space, any value of regulated Vout can be provided with the full range of Vin allowed by the boundaries of the space. In Figure 19, a typical 5V converter application space is defined and three example applications are shown. Each is a constant Vout and the range of Vout represents a majority of the available values of Vout that might be used with the same DC-DC converter model number.

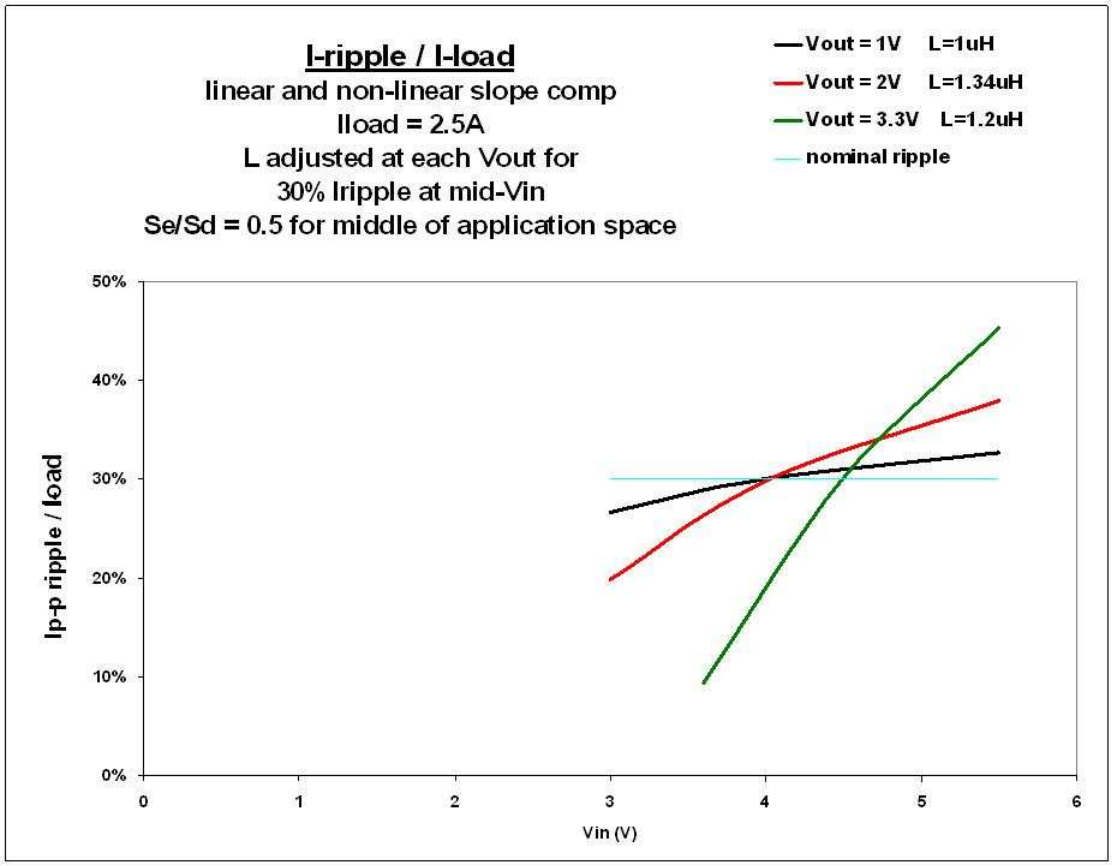


Figure 20. Inductor ripple current for the 5V converter sample applications.

Figure 20 shows the dependence of inductor current ripple on Vin for the three sample applications. Since CMC relies on inductor ripple as a feedback signal, ripple current needs to be bounded. Without enough ripple, excessive noise may interfere with CMC operation and the physical size of the inductor also becomes larger than is necessary. Excessive current ripple leads to greater output voltage ripple and the possibility of either negative valley current in the inductor or discontinuous conduction if the converter operates with unnecessary discontinuous mode control. A center value for ripple current equal to 30% of Iload is targeted for this example. It is often desired to limit the deviation of peak-to-peak ripple current from the nominal value over the application's Vin range. Therefore the analysis assumes that for each application, the target value of ripple is set at the mid level of Vin range. Ripple is adjusted by the selection of the inductor value for a given switching frequency and load current. The ripple's positive and negative deviation from the target is therefore

balanced over the expected range of Vin. The inductor ripple current is not affected by slope compensation. Conversely, the preferred value of slope compensation is dependent on the system determined inductor ripple; therefore the system engineer is usually advised of an optimal ripple current that best suits the slope compensation value provided by the controller circuit. The Figure 20 plot of ripple current for various Vout applications is independent of slope compensation design options. Where the type of slope compensation does matter is the Qs variation across the vertical direction of the application space and, to a lesser degree, the magnitude variation of the control signal. These parameters are plotted in Figure 21.

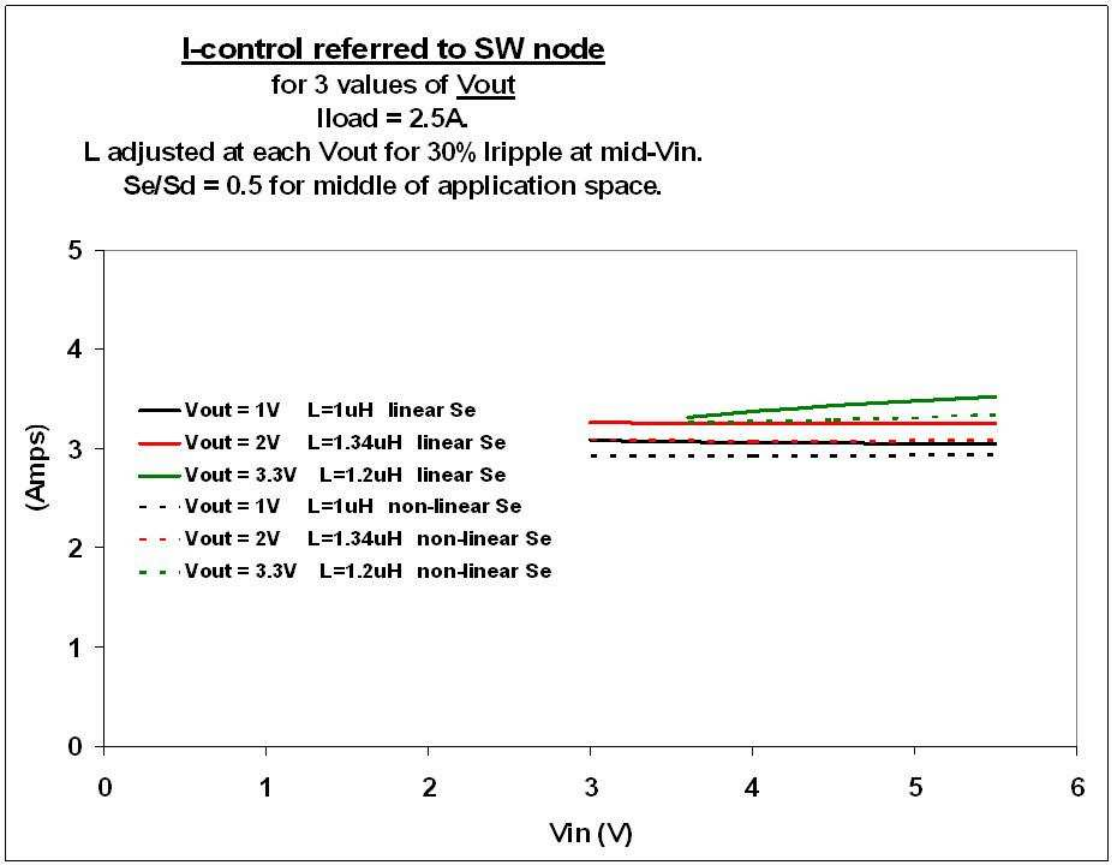


Figure 21. Variation of Icontrol with Vin for several values of Vout, 5V converter example. Linear and non-linear slope compensation techniques are contrasted.

Figure 21 illustrates that across the range of Vout applications, non-linear slope compensation has approximately the same variation in Icontrol as linear slope compensation. The advantage of non-linear slope compensation is the slightly lower peak magnitude required

which translates to a larger useful range. This plot assumes Se/Sd = 0.5 at roughly the middle of the application space (Vin = 4V and Vout = 2V). A plot of Se/Sd = 1 would look similar, with the curves shifted down by about 0.5 Amp. The benefit of non-linear slope compensation is not yet clearly evident with this plot.

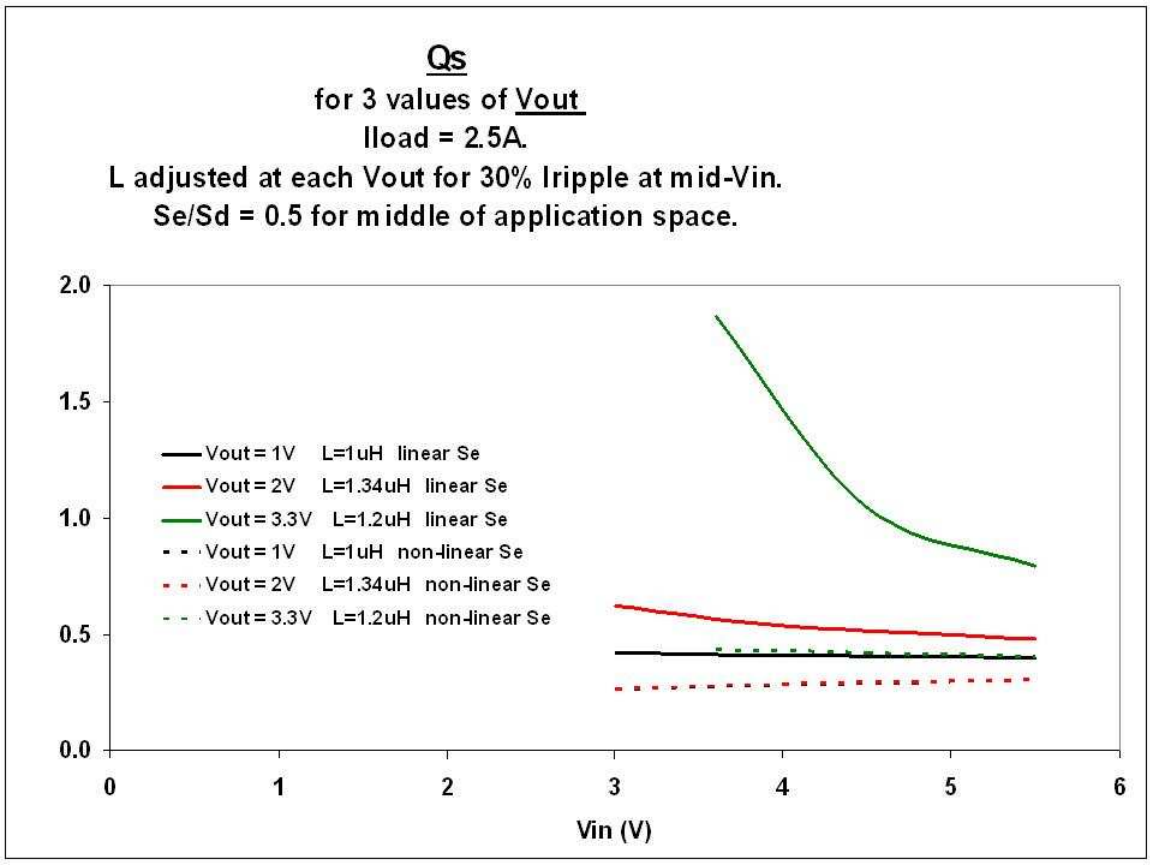


Figure 22. Variation of CMC small signal gain peaking due to the Fs/2 sampling complex pole pair versus Vin for different values of Vout, 5V converter example. Linear and non-linear slope compensation techniques are contrasted.

Qs is a key parameter for prediction of sub-harmonic oscillations. Sub-harmonic oscillation can be predicted by plotting waveforms as was done in Figures 5-7 (from part 1) or by calculation of Qs. The equation for Qs is listed in the Appendix. It is curious that both large signal analysis of inductor currents and a small signal analysis of the CMC gain peaking both predict the sub-harmonic or Fs/2 oscillation. The plots of settling time for perturbed inductor current are a good visual aid for proving instability. However the sampling Qs is a more

convenient parameter for plotting a measure of stability as a function of operating conditions.

Figure 22 above illustrates the benefit of non-linear slope compensation. For a fair comparison, the magnitude of linear compensation Se at the mid-Vout point is set to match that of non-linear slope compensation the same value of Vin and Vout. Due to non-linear slope compensation's continuously adapting to change in duty cycle, Qs is limited to a narrower band. In the case of linear compensation, Se/Sd deviates from the mid-Vout value as higher values of Vout are selected. Higher Vout applications require higher Se if the ripple current is bounded to a target range. The non-adapting linear slope compensation necessarily leads to a lower Se/Sd as higher Vout is required. The highest value of Qs in Figure 22 is nearly a value of 2 and this level of peaking probably requires some extra attention in the choice of compensation components and may limit the final system bandwidth in order to reduce the risk of instability. The system designer has some latitude with ripple current for high duty cycle applications with linear slope compensation. Since it is known that Se will be lower than ideal for high duty cycle, Sd could be lowered with increases in L. This incurs risk as was mentioned earlier, as CMC requires adequate ripple current feedback signal strength and this approach lowers ripple current at the lower range of Vin for a given application.

The examples up to this point have been for a typical low voltage converter. The following is the same analysis applied to medium voltage systems.

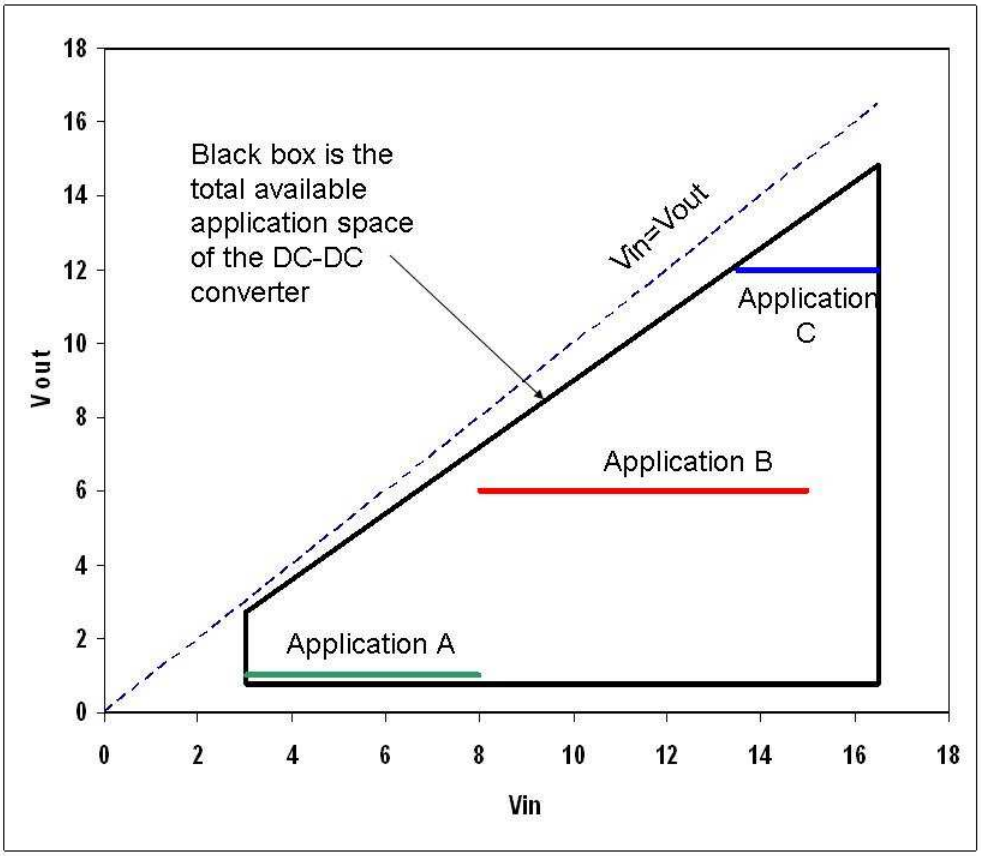


Figure 23. Total application space for a 16V buck DC-DC converter model and three specific applications (fixed Vout, and L) within the space.

The 16V DC-DC converter application space of Figure 23 includes examples of 3 possible applications each with a fixed value of Vout and an expected range of possible Vin. The individual Vin ranges of each application are more staggered than in the 5V example, however it is shown that the relative merits of linear and non-linear slope compensation remain approximately the same.

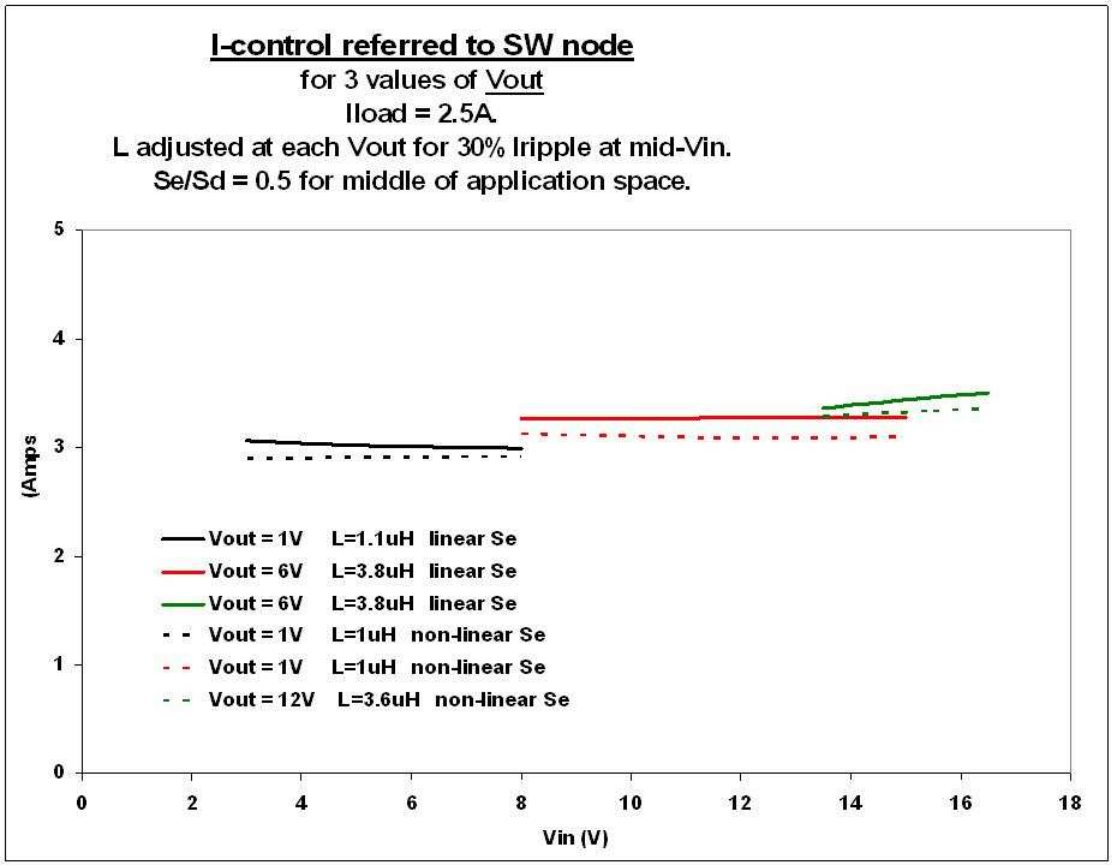


Figure 24. Variation of Icontrol with Vin for several values of Vout for a 16V converter example. Linear and non-linear slope compensation techniques are contrasted.

The 16V converter control current variation is shown in Figure 24 for Se/Sd = 0.5 at the mid-Vout option of 6V. Notice that the zero line regulation (flatness of Icontrol with a change in Vin) appears ideal for the mid-point, 6V linear slope compensation option. Non-linear slope compensation under the same conditions results in a very slight curvature of Icontrol. However this Icontrol variation is significantly flatter than is required for voltage mode control schemes. (Voltage mode control can include line voltage feed-forward compensation of the ramp voltage to improve line regulation.)

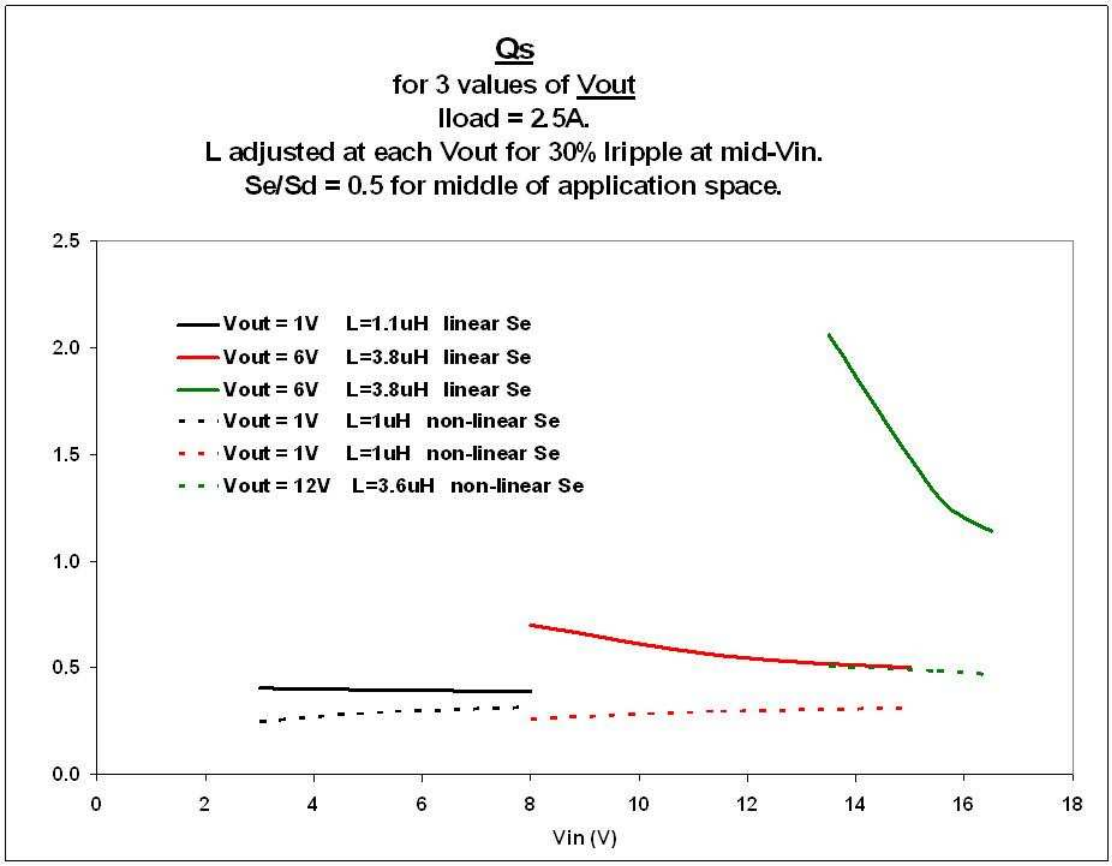


Figure 25. Variation of gain peaking due to the Fs/2 sampling complex pole pair versus Vin for different values of Vout, 16V converter model. Linear and non-linear slope compensation techniques are contrasted.

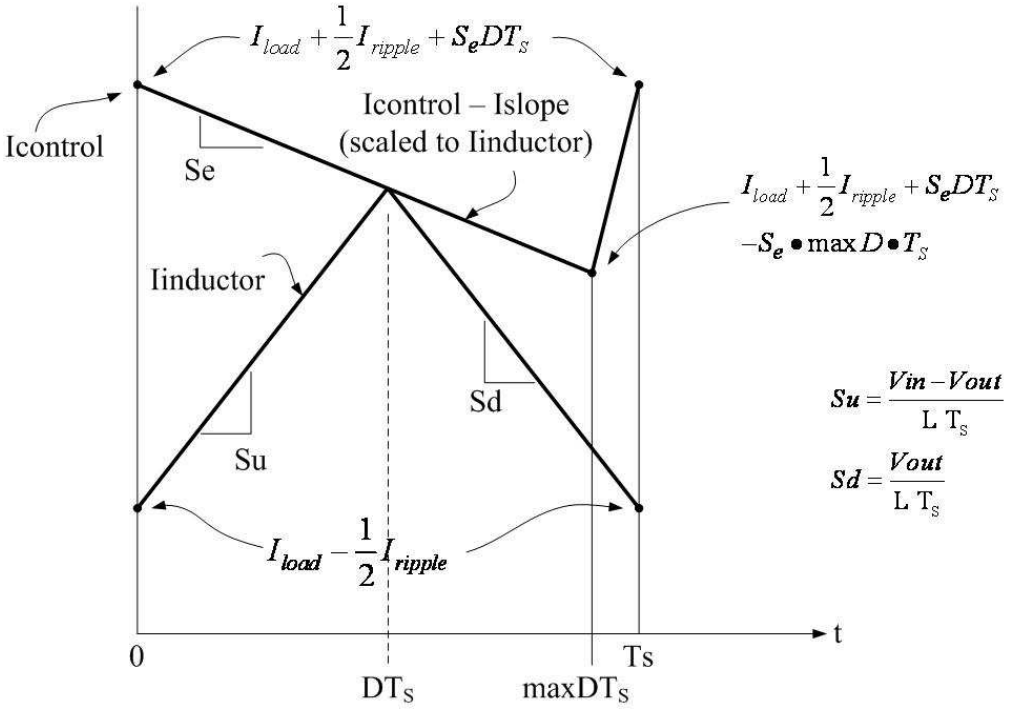
Figure 25 displays the same penalty of increasing Qs for the high duty cycle application of linear slope compensation; as was seen in the 5V example. The non-linear slope compensation approach adjusts Se to match Sd as Vout is changed for different applications, so non-linear offers more consistent control over the entire application space.

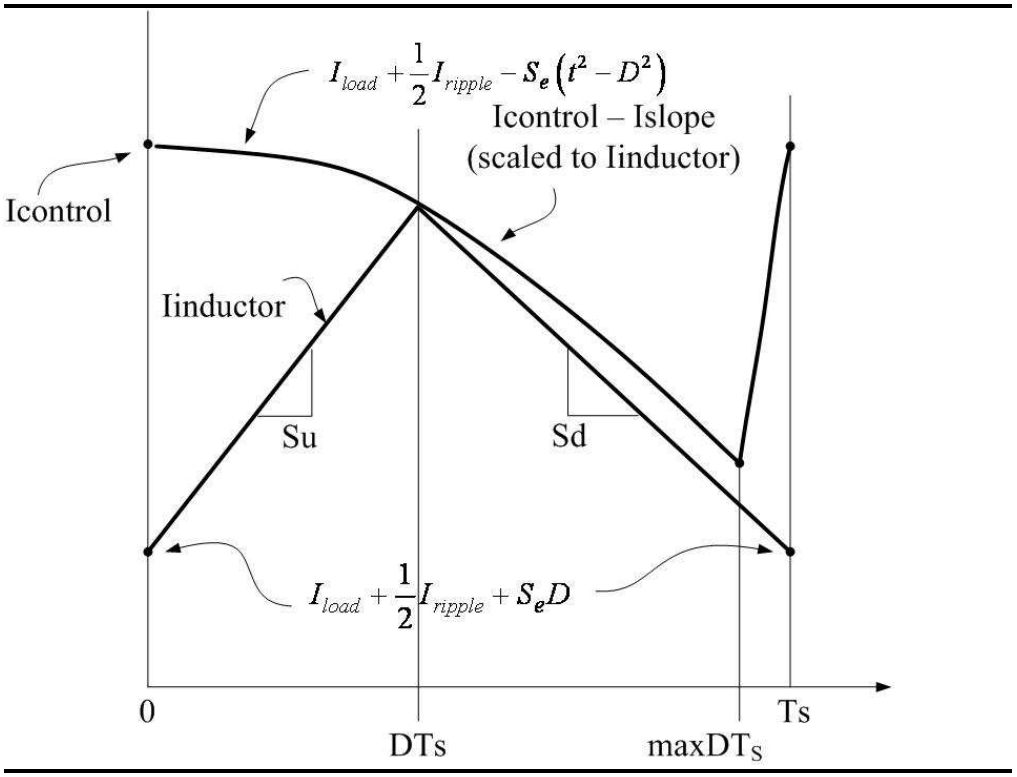
5. Summary

The reason for the addition of slope compensation to peak Current Mode Controlled buck converters is graphically revealed in plots of perturbed inductor current for different levels of Se. Inadequate Se was shown to lead to instability. A second method that predicts the

same cause of instability, Qs, was also discussed. The addition of slope compensation was also shown to increase the noise rejection. Two special cases of Se were detailed, one that provides single cycle settling and the other that promises near ideal systematic line regulation. The plots revealed that for these two special cases, linear slope compensation has slight advantage over non-linear slope compensation for a particular value of Vout where both methods have a similar Se/Sd. Significant improvement was seen in the favor of non-linear slope compensation when a fixed setting for the magnitude of Se was applied to the full range of Vout. This fact was illustrated by a low level of sensitivity of Qs to the location of the design in the total application space.

Appendix of Equations Used in the Plots





$$Q_S = \frac{1}{\pi\left[\left(1+\frac{\mathrm{Se\,L}}{Vin-Vout}\right)(1-D)-\frac{1}{2}\right]}$$

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