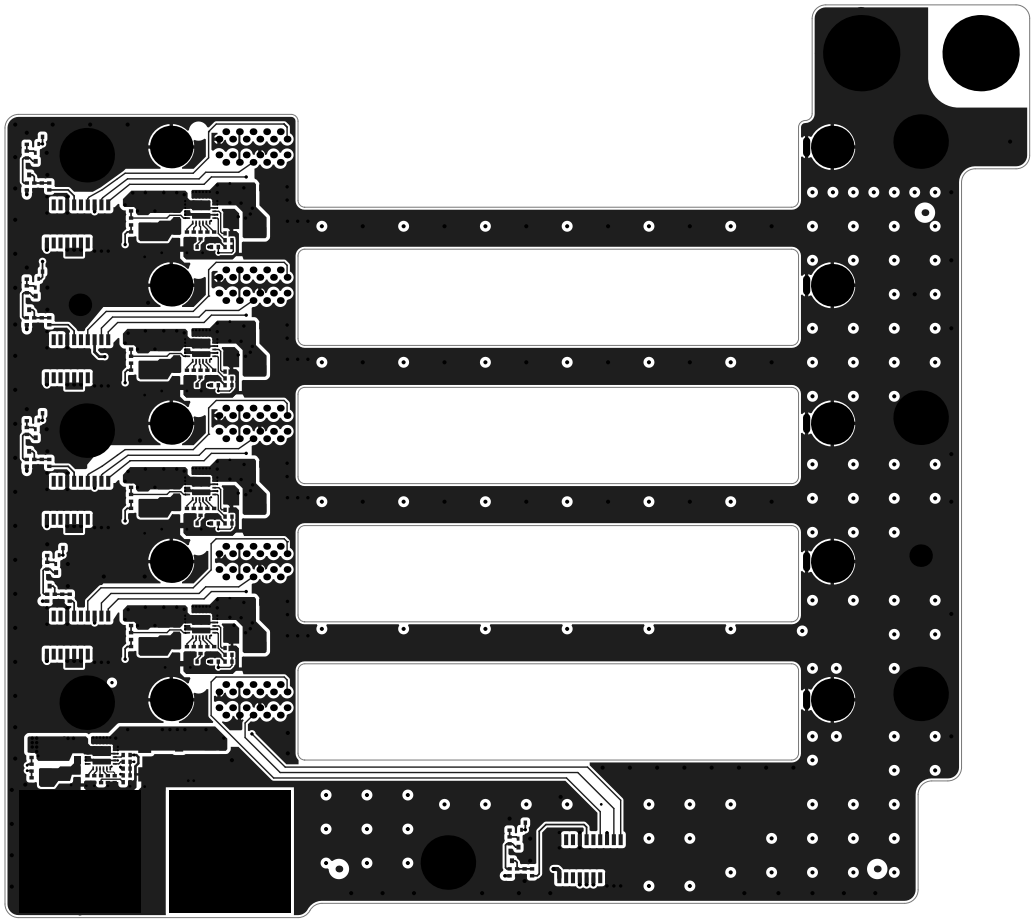
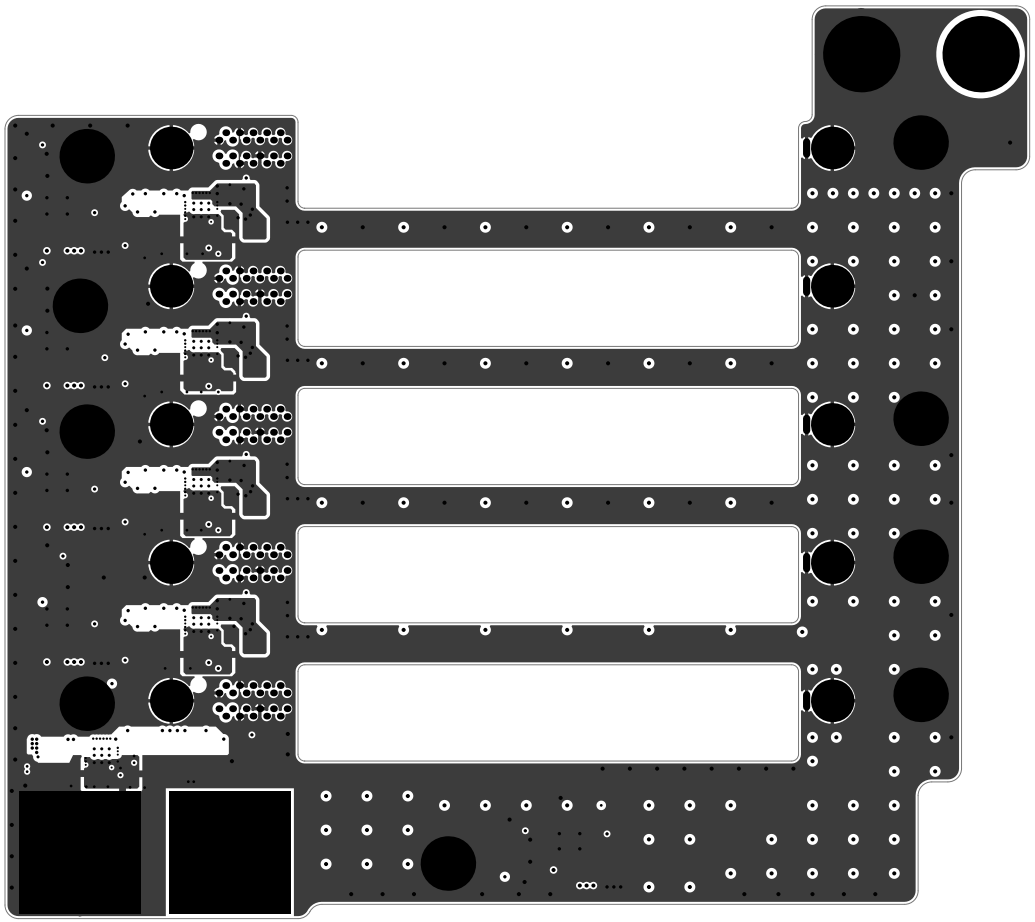
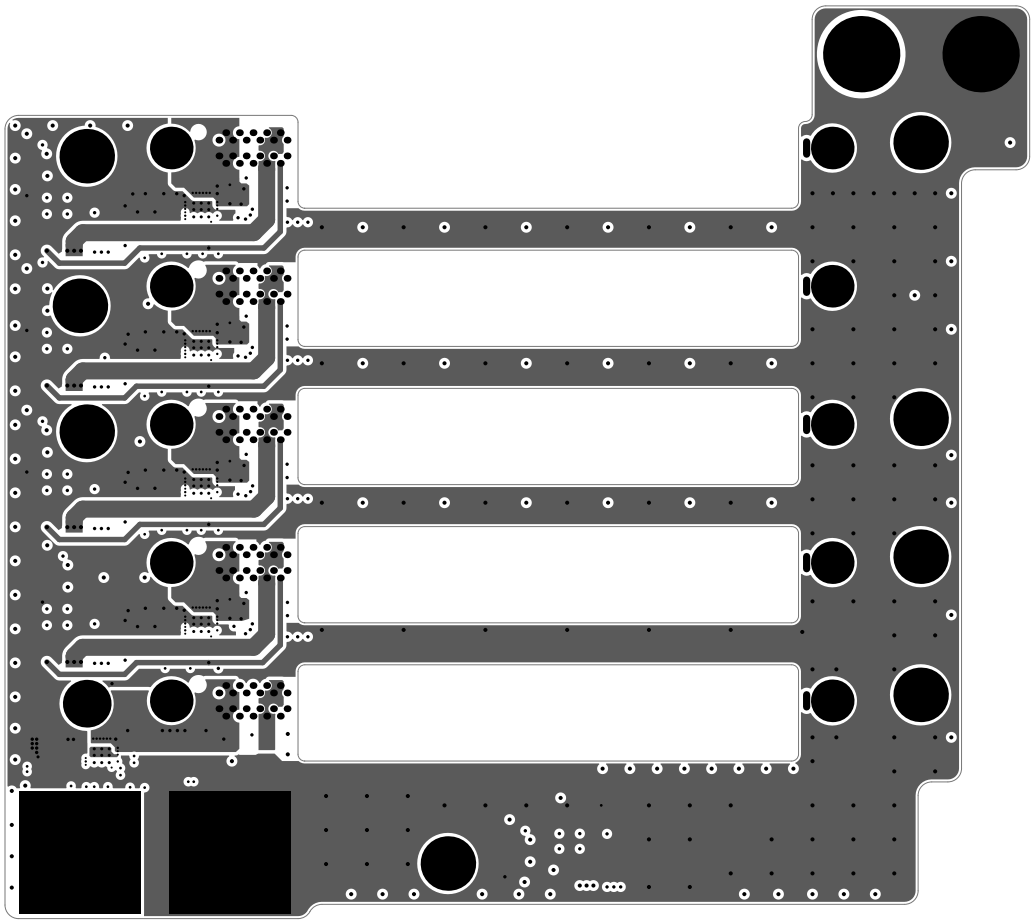


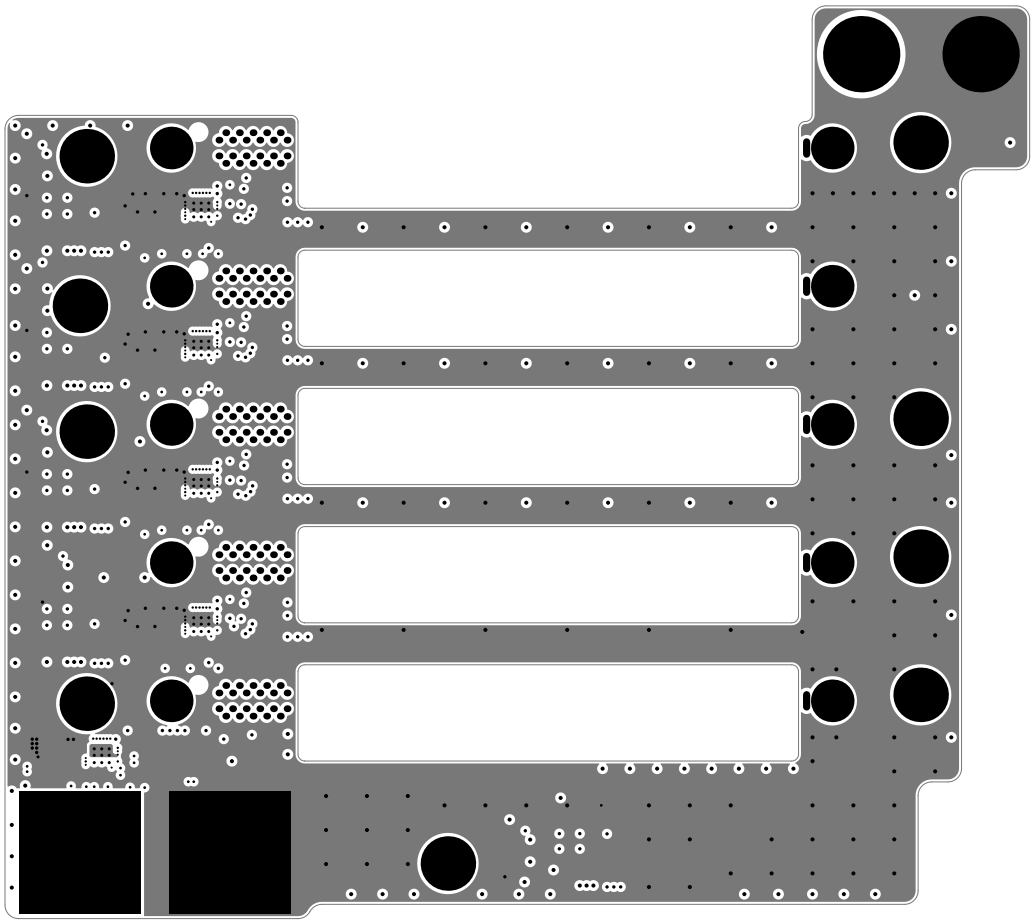
TOP Layer



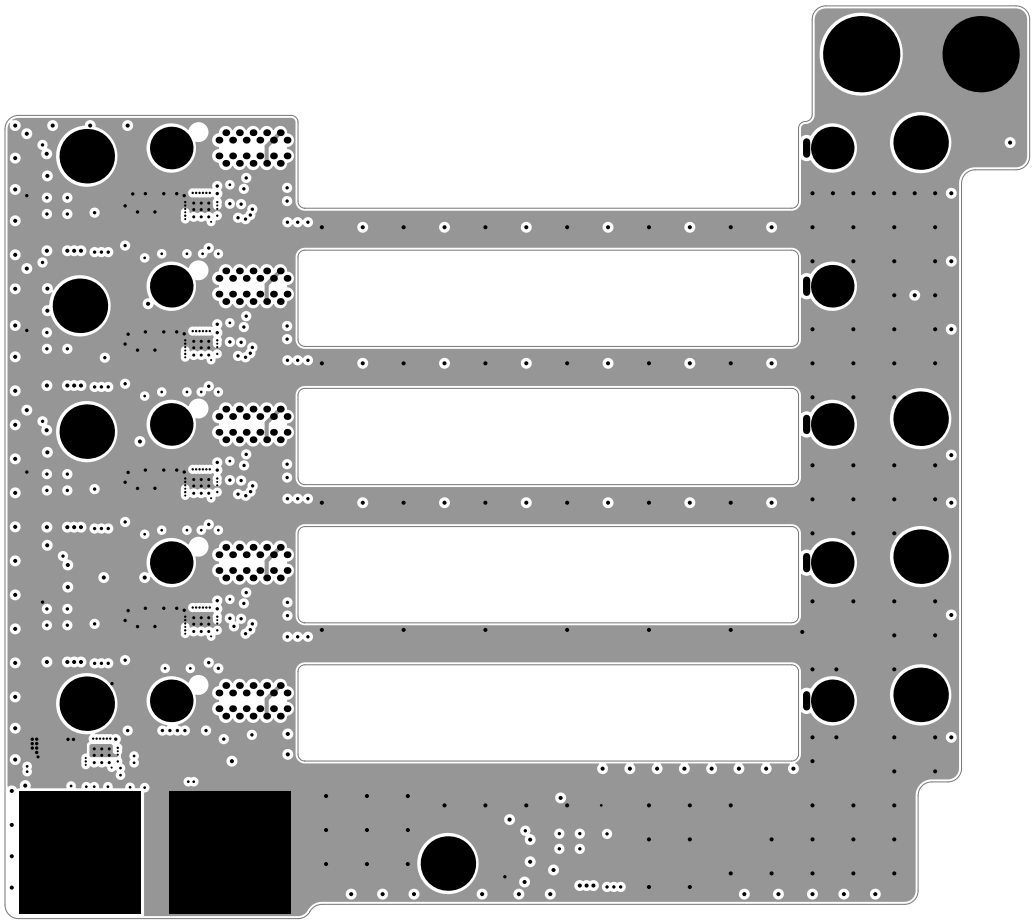
Layer 2



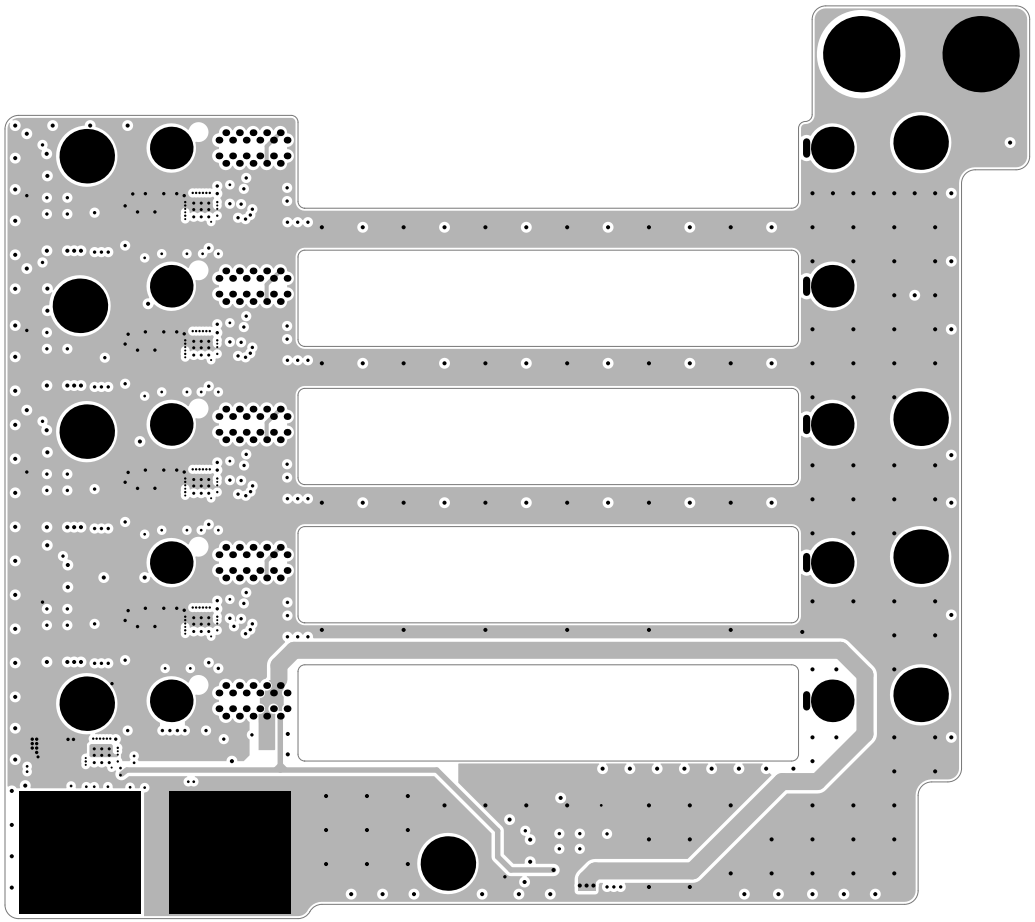
Layer 3



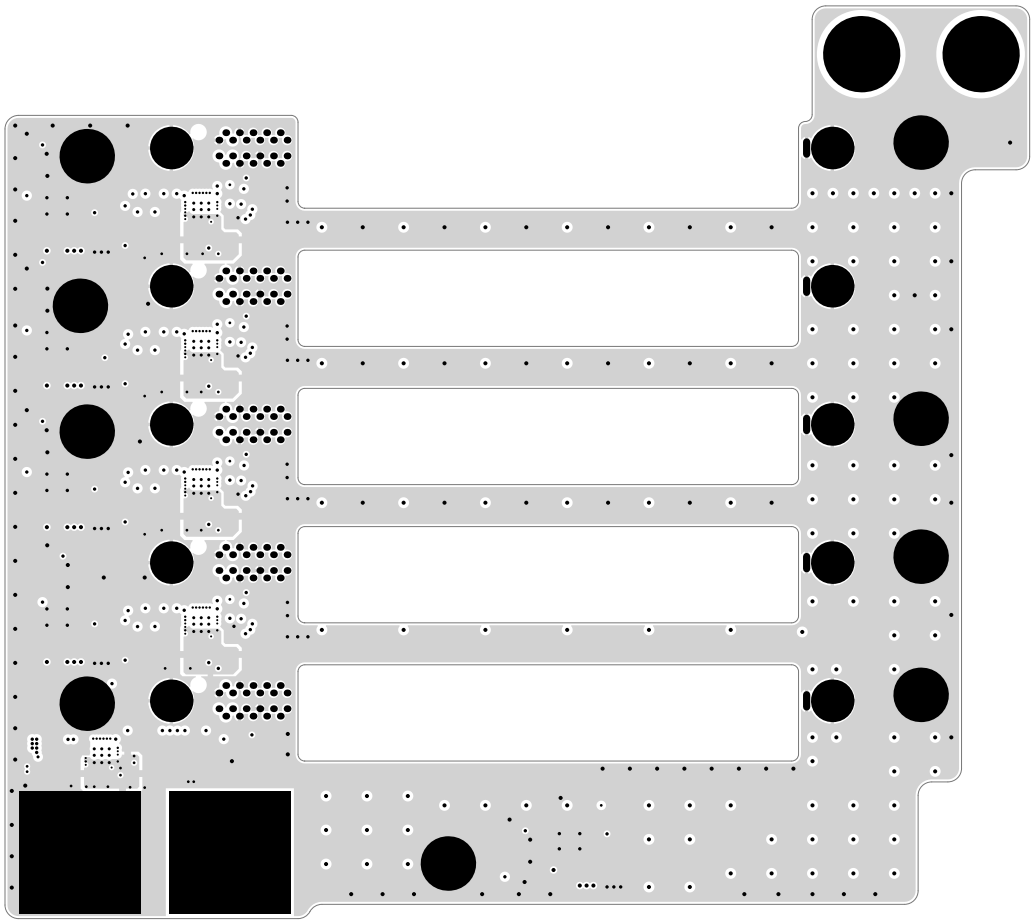
Layer 4



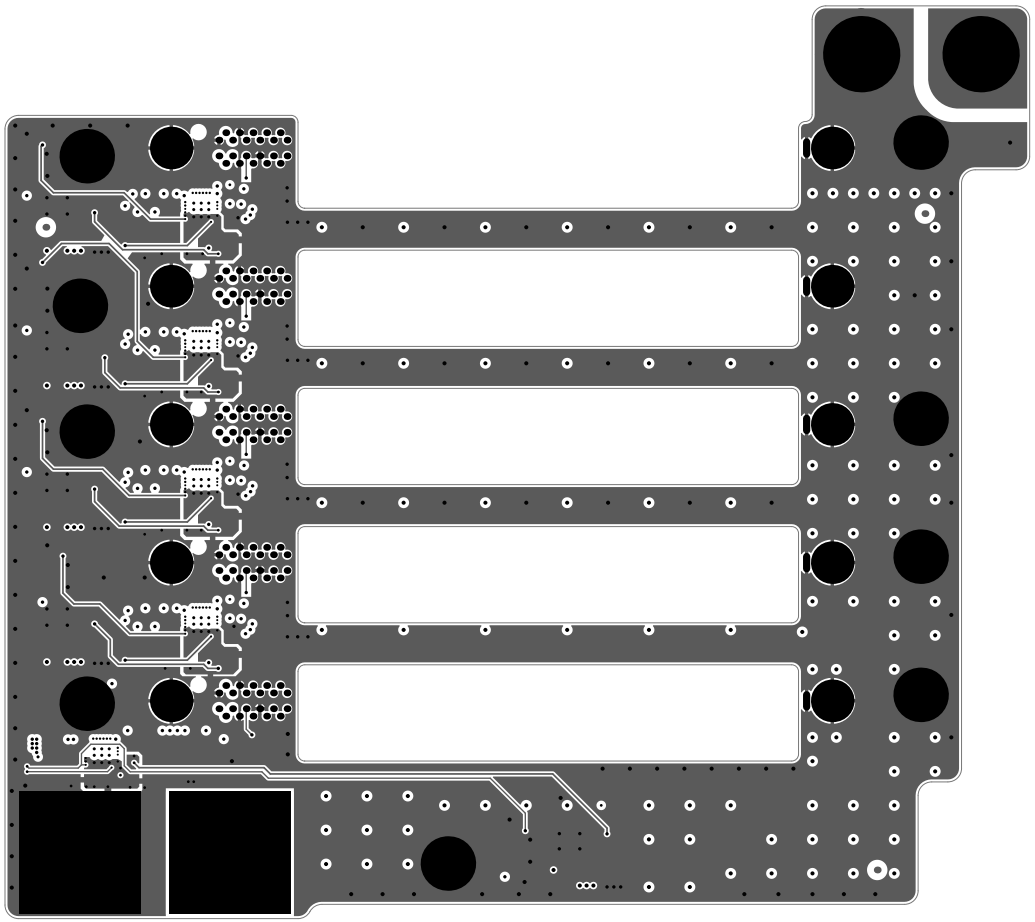
Layer 5



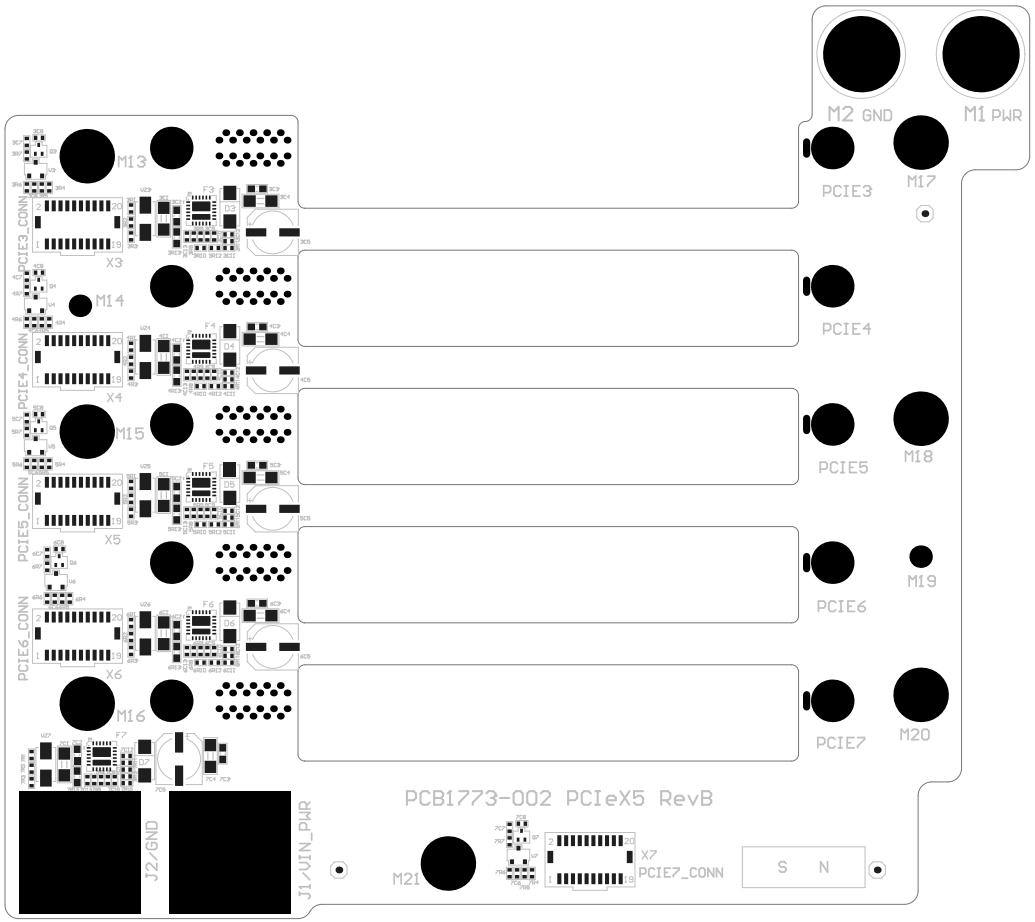
Layer 6



Layer 7



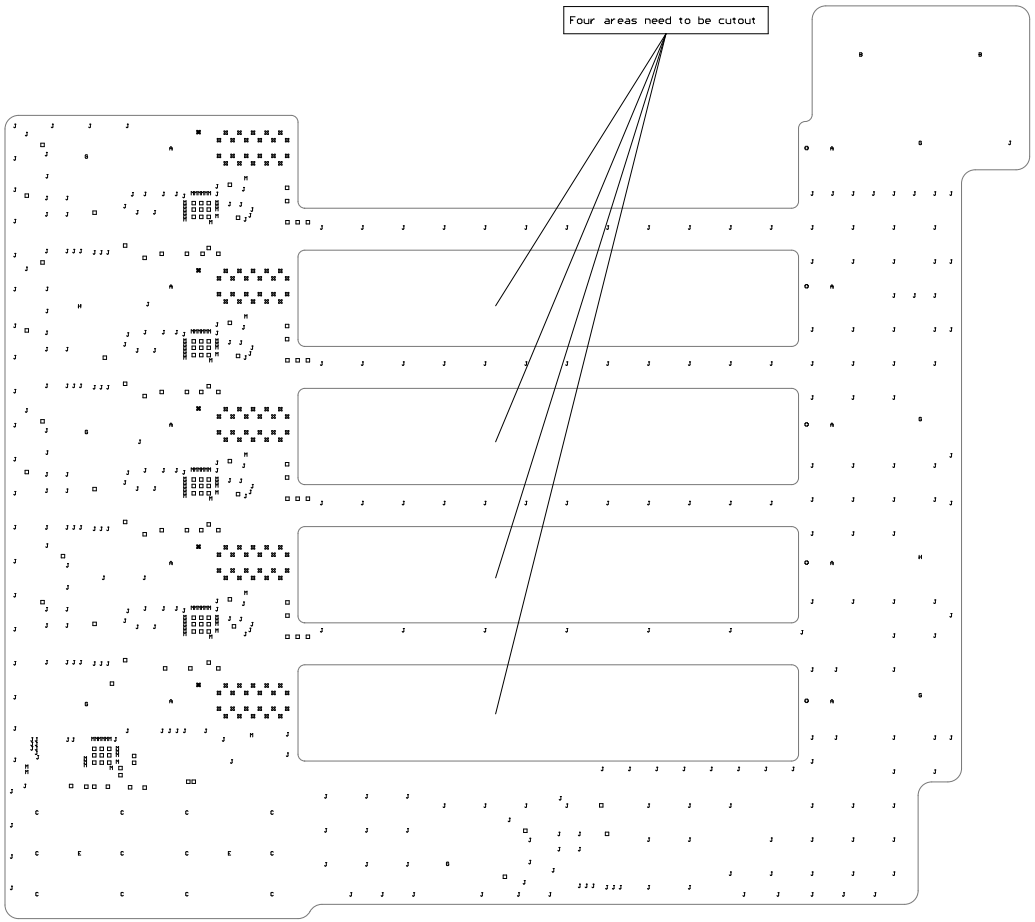
Bottom Layer


M2 GND
M1 PWR
PCIE3
M17
M13
PCIE3_CONN
X3
M14
PCIE4
PCIE4_CONN
X4
M15
PCIE5
M18
PCIE5_CONN
X5
PCIE6
M19
PCIE6_CONN
X6
M16
PCIE7
M20
PCB1773-002 PCIeX5 RevB
J2/GND
J1/VIN_PWR
M21
X7
PCIE7_CONN
S N

TOP Overlay

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
H	2	3.300mm (129.92mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c330h330z800x800(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
E	2	4.500mm (177.17mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rectangle	r1800_1780h450			
B	2	5.500mm (216.54mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c1120h550(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
✪	5	0.660mm (25.98mil)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r106_286h66_246r100(Tol8-8)		0.075mm (2.95mil)	0.075mm (2.95mil)
⊠	5	1.900mm (74.80mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn190m200(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
G	7	3.500mm (137.80mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
A	10	4.220mm (166.14mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
C	12	3.100mm (122.05mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c500h310			
M	89	0.150mm (5.91mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
⊠	110	0.720mm (28.35mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c100h72(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
□	128	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
J	346	0.250mm (9.84mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
	718 Total										

Slot definitions : **Routed Path Length** = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.39mil	4	
3	Top Layer	Copper	2.95mil		
4	Dielectric1	FR-4	5.91mil	4.8	
5	L2_GND	Copper	2.76mil		
6	Dielectric 2	FR-4	5.91mil	4.8	
7	L3_PWR	Copper	2.76mil		
8	Dielectric 4	FR-4	5.91mil	4.8	
9	L4_PWR	Copper	2.76mil		
10	Dielectric 5	FR-4	5.91mil	4.8	
11	L5_GND	Copper(plated)	2.76mil		
12	Dielectric 6	FR-4	5.91mil	4.8	
13	L6_PWR	Copper	2.76mil		
14	Dielectric 7	FR-4	5.91mil	4.8	
15	L7_PWR	Copper	2.76mil		
16	Dielectric 3	FR-4	5.91mil	4.8	
17	Bottom Layer	Copper(plated)	2.95mil		
18	Bottom Solder	Solder Resist	0.39mil	4	
19	Bottom Overlay				

1. Fabricate and test per IPC-6012, Class 2.
2. Finish: ENIG.
3. There are to be no non-functional pads on all internal signal layers.
4. All dimensions on the drill drawing layer are in MM.
5. General Hole Tolerance Drilled holes +/- 1mil and Finished holes +/- 2mil
6. Soldermask shall be liquid photoimageable. Blue soldermask under white silkscreen.
7. The thickness of board is 1.6mm+/-10% .
8. The impedance is 50ohm +/-10% for 0.205mm width on Top layer.
9. Add year/weak in blank location and SN place the specified position.
10. High-voltage insulation test(5 pcs power)
    Test conditions: voltage/current -1500V/0.1mA, the Creepage Voltage 500V/S,
    1500V is maintained for 3 to 5 seconds.