Hello Ferry,

I reviewed the schematic and waveforms and have a few comments and suggestions.

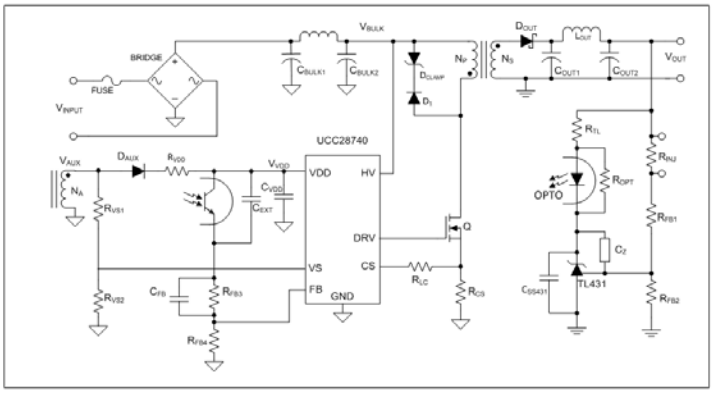
1. The gate drive and auxiliary waveforms signals that you sent appear to be bursting at 62.5 kHz.
    a. The UCC28740 does not have burst mode.
    b. This could be a large signal issue or small signal loop stability issue.

2. I don't believe this is an over current fault. I believe it is a large signal or small signal loop stability issue.

3. Possible causes of Large Signal Loop Stability Issues.
    a. Electronic device not properly setup or biased.
    b. Things to check
        i. If VDD was transitioning between the turn on threshold (21V) and turnoff threshold (7.75V) this would indicate a fault. (Input Under Voltage, Over Current, Over Voltage, and Temperature).
            - Double check VDD to ensure this is not occurring.
        ii. Op Amps and ICs are not properly biased.
        iii. OpAmp IC202-A/B bias rails should be DC stable.
        iv. Voltage supping the TPS25740 should be DC stable.
        v. IC1 input and output voltage should be DC stable.
        vi. TPS25740 is misbehaving.
            - Check CTL1 and CTL2 voltages for DC stability.
    c. If any of the above ends being the cause of the issue. The biasing or misbehaving component issues need to be resolved.

4. Small Signal Stability Recommendations.
    a. To check loop stability you can evaluate the UCC28740 FB pin and the designs output voltage to check for stability.
        i. They should be DC with very little ripple voltage.
        ii. If these pins have large signal sinusoidal ripple the cause is most likely small signal loop stability.
        iii. If these pins have large triangular or square waves on them most likely it is large signal stability issue.
    b. I noticed the feedback loop was type 3 compensation and you were depending on the opto for the high frequency pole.
        i. This is not the typical compensation network that is used for the UCC28740. However, it can be used if you use a network analyzer to compensate the voltage loop.
    c. The UCC28740 data sheet recommends using a capacitor (CFB) across RFB3 (R63 in your design) to filter out high frequency noise.

i. I notice this design does not have this capacitor. You might consider adding it to make the design less susceptible to noise.
ii. The data sheet recommends setting this time constant to 1 ms and then fine tune the capacitor as needed.



a. There is an Excel calculator that you can use to compensate the voltage loop at the following link. http://www.ti.com/lit/zip/sluc487
iii. Please note that this compensation scheme is slightly different than what your customer is using. However, the board could be modified to support this control scheme just to check to see if it resolves the problem.

b. If this problem proves to be a small signal stability issue. The following can be done.
a. Use UCC28740s recommended compensation scheme with the Excel design tool to compensate the voltage loop.
b. Use a network analyzer to compensate the voltage loop.

Regards,

Mike