Top layer – Ground and signal – L7 has a special polygon allocated only for it (for switching).
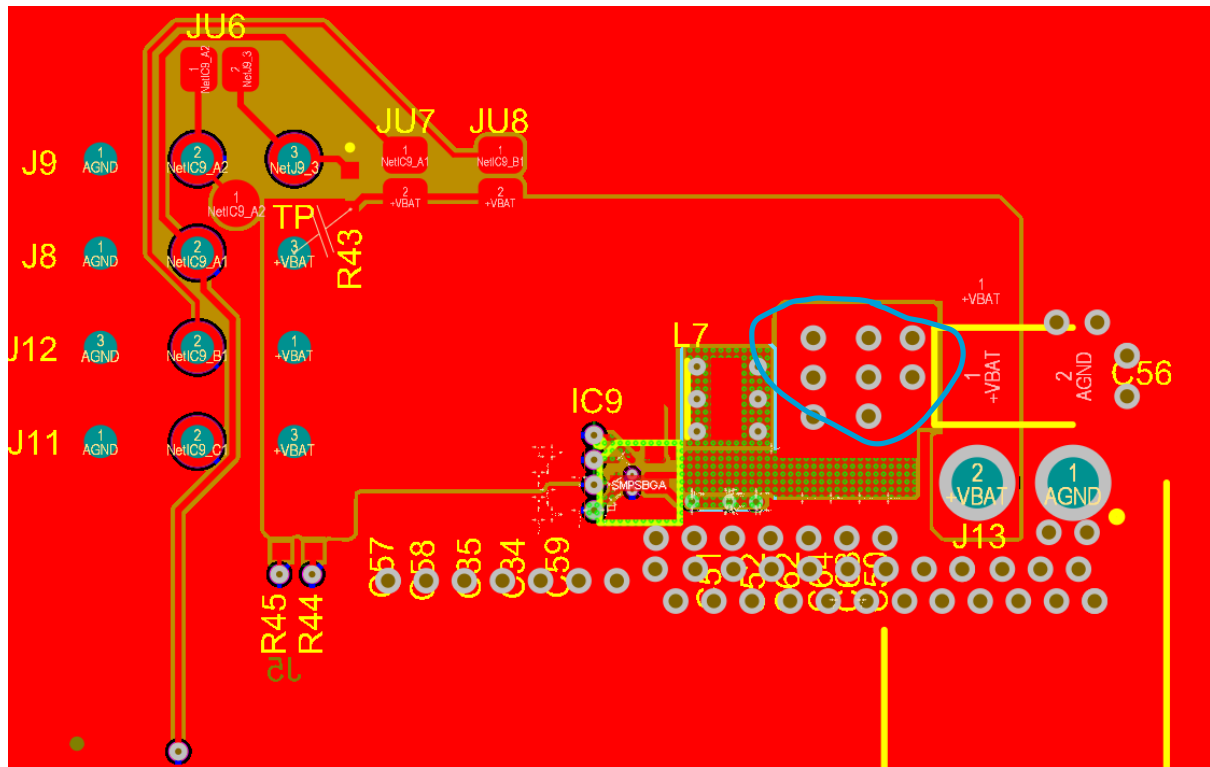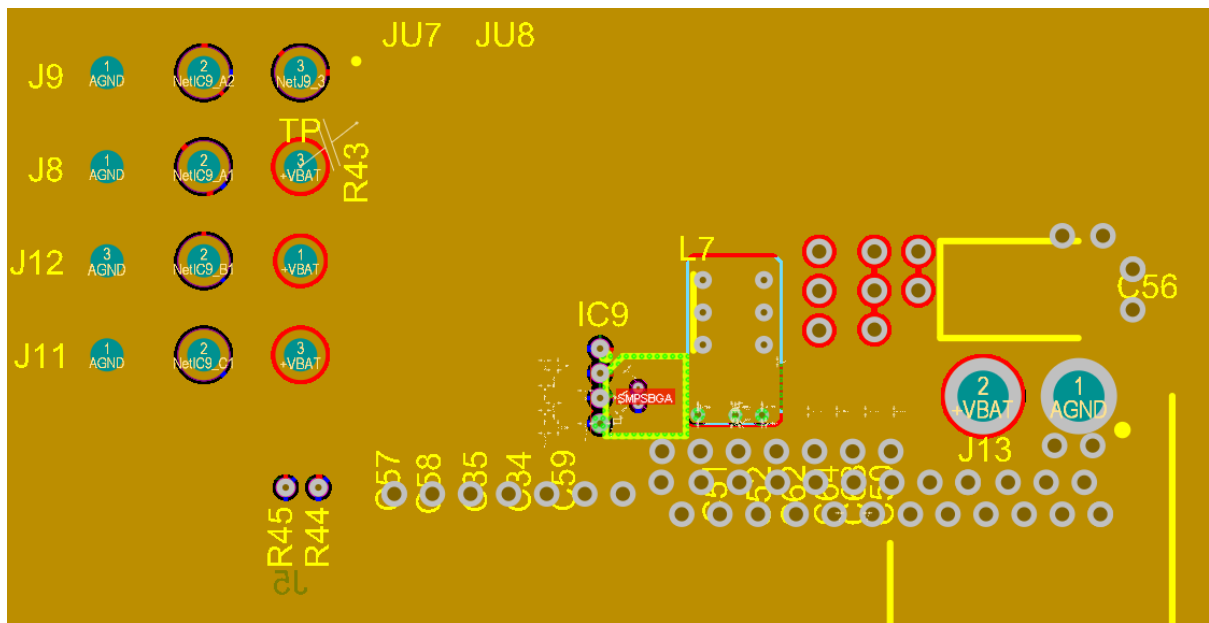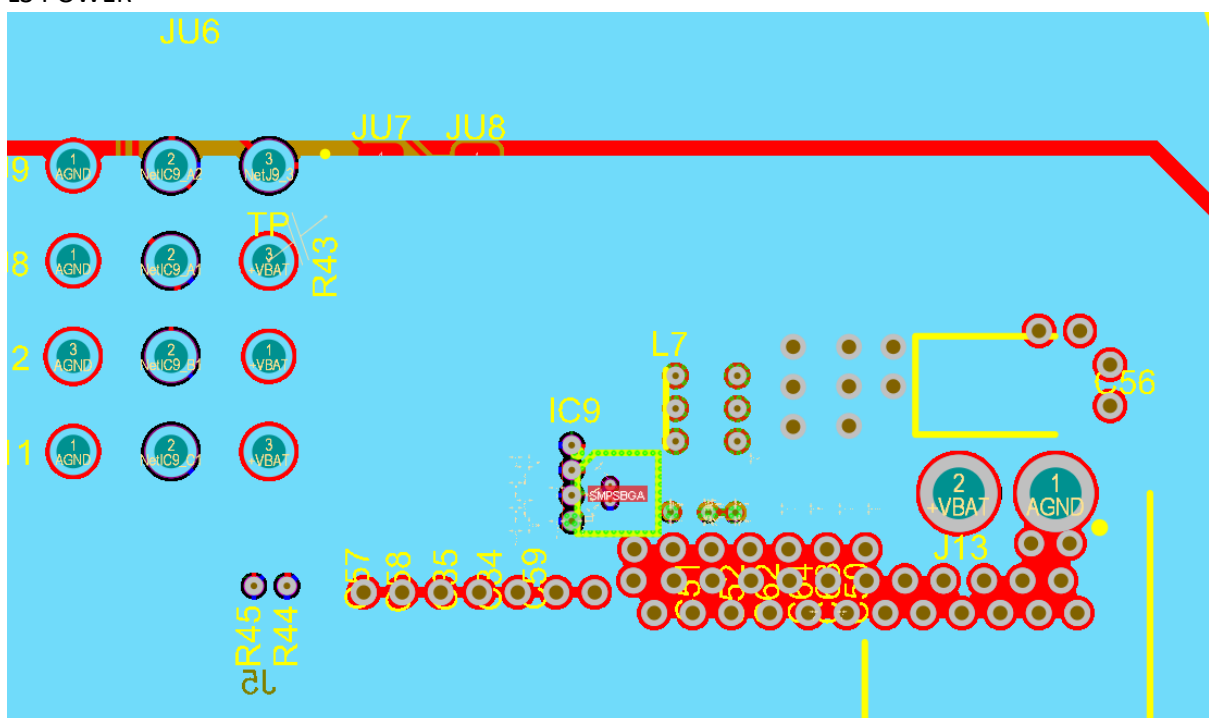
Right of the L7 is the BGA Vout (in the blue circle)

L2 – Ground

L3 POWER

L4 GROUND

PCB Layout (top)

J9 1 AGND 2 NetIC9_A2 3 NetJ9_3 JU7 JU8

J8 1 AGND 2 NetIC9_A1 3 +VBAT TP R43

J12 3 AGND 2 NetIC9_B1 1 +VBAT

J11 1 AGND 2 NetIC9_C1 3 +VBAT IC9 SMPSBGA

L7 C56

2 VBAT 1 AGND J13

C57 C58 C35 C34 C59

R45 R44 J5

Schematic (bottom)

GPIO[USER SET LOW] = RESET
GPIO[OUTPUT] = LOW = FAULT

EN[LOW] = SHUTDOWN MODE
EN[HIGH] = ENABLE

NBYP[LOW] = BYPASS MODE
NBYP[HIGH] = NORMAL OPERATION

DEVICE_GND J9 R43 ERJ-PA2J222X +VBAT DEVICE_GND JU7 +VBAT

PSU GPIO +VBAT JU6

R44 2.2k DEVICE_GND +VBAT JU1

TP4 TP Test Point

+C56 150uF C57 4.7uF C58 4.7uF C35 4.7uF C59 4.7uF Test Point

IC9
A1 EN   NBYP C1
A2 GPIO   SDA C2
A3 VIN_1   SW_1 C3
A4 VIN_2   SW_2 C4
B1 VSEL   AGND D1
B2 SCL   PGND_1 D2
B3 VOUT_1   PGND_2 D3
B4 VOUT_2   PGND_3 D4
TPS61280Y9FT

PSU EN
PSU GPIO
Test Point

PSU NBYP
PSU SDA

L7 1 2

C59 DEVICE_GND

PSU VSEL

DEVICE_GND

PSU SCL JU8 R45 2.2k +VBAT +VBAT

DEVICE_GND DEVICE_GND

J12
VSEL[LOW] = PFM WITH TRANSITION PWM
VSEL[HIGH] = FORCED PWM

C51 10uF C42 10uF C62 10uF C63 10uF C64 10uF C50 10uF PVIN

DEVICE_GND

Battery Connector

2 +VBAT +VBAT
1 BAT_GND
J13 DEVICE_GND

Title

Size A4   Number   Revision

Date: 12/26/2021   Sheet of
File: C:\Users\...\System_PSU2.SchDoc   Drawn By: