COLIN,

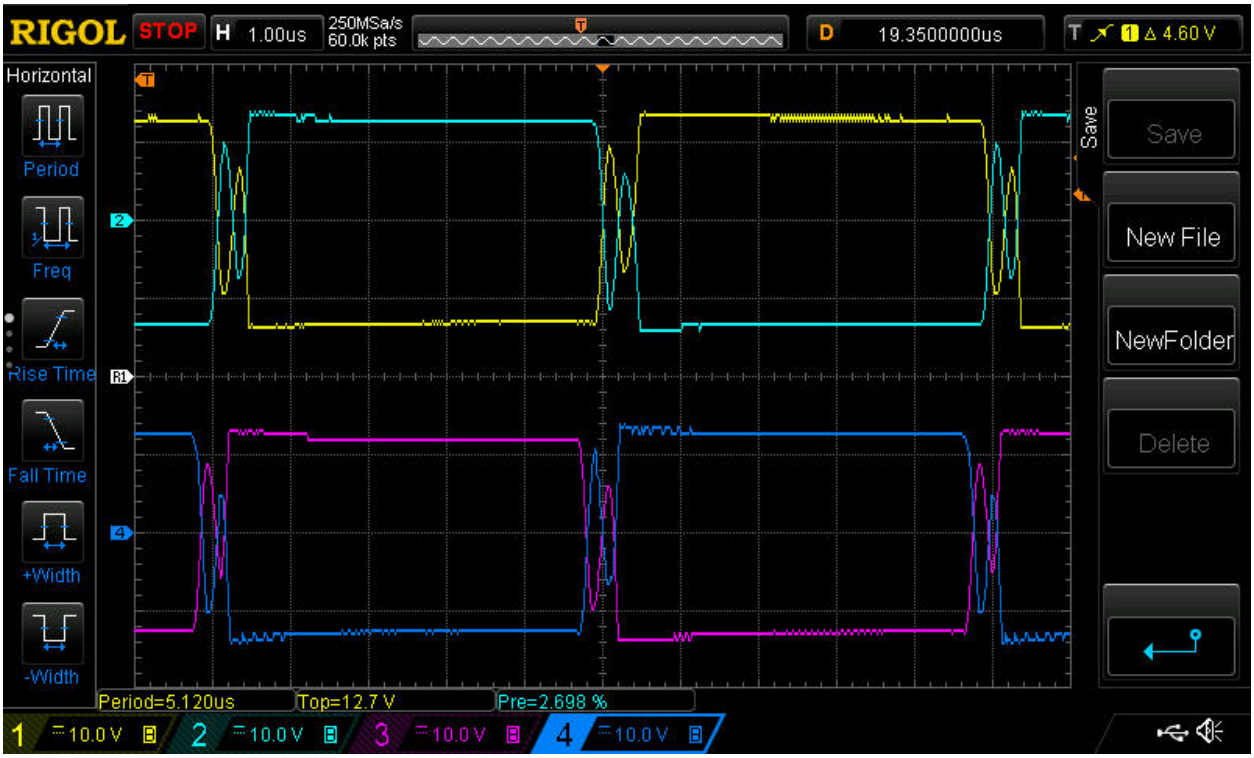
WITH NO VOTAGE ON THE DC INK, GATE SIGNALS LOOK GREAT. AS SOON AS I PUT ANY VOLTAGE ON THE DC LINK, THE OUTJPUT SIGNAL OF THE MOSFETS APPEAR TO GO INTO A STRANGE KIND OF BURST MODE. EVEN THE GATE SIGNALS CHANGED INTO A, FOR LACK OF BETTER WORDING, A STRANGE TYPE OF SPORATIC BURST MODE.

AS PER THE TI UCC28950, UCC28951 Debug LITERATURE : "The controller does not have an undervoltage lock out on the input voltage and so it will operate at Dmax". MY SYSTEM DID NOT OPERATE AT DEMAX. IT STARTED WITH SPORATIC TYPE BURST MODE SIGNALS WHICH I WAS UNABLE TO GET A PIC OF.

95% OF THE TIME MOSFETS GET DESTROYED THAY ARE Q3 AND Q4. Q1 AND Q2 USUALLY ARE NOT DAMAGED.

WITH NO MOSFETS, NO DC LINK, NO TRANSFORMER, THIS IS THE GDT OUTPUT SIGNALS.

GDT OUTPUT WAVEFORMS Q1 – YELLOW, Q2 – TEAL, Q3 – MAGENTA, Q4 BLUE




IS IT MY DELAY TIME, DEAD TIME? WHAT EVER IT IS, IT IS CHANGING THE SIGNAL COMING FROM THE UCC28950 IC. THIS TELS ME IT IS EITHER THE FEEDBACK PIN 4, CURRENT SENSE PIN 15, VDD RAIL?

WHATS HAPPENING TO THE OUTA, B, C, D SIGNALS ARE NOT BECAUSE OF THE LOAD, BECAUSE WHAT HAPPENS TO THE LOAD CAN NOT GO BACKWARDS THRU THE GDT AND CAUSE IT TO CHANGE.

I BELIEVE I HAVE AN INPUT TO THE BOARD THAT IS MESSING UP. I NEED TO FIND IT.

WILL REPLACE MOSFETS AND CAREFULLY CAPTURE WAVEFORMS SO YOU CAN SEE WHAT I SEE.

**FIGURE 1 THRU FIGURE 13 DEFINES MOSFET GATE WAVEFORM WITH NO DC LINK**

**FIGURE 14 THRU FIGURE 21 DEFINES MOSFET GATE WAVEFORM WITH 45V DC LINK**

PLEASE REVIEW AND RESPOND WITH ANY IDEA OF WHAT IS HAPPENING.

THANK YOU

EDDIE LOY

FIGURE 1. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**


FIGURE 2. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

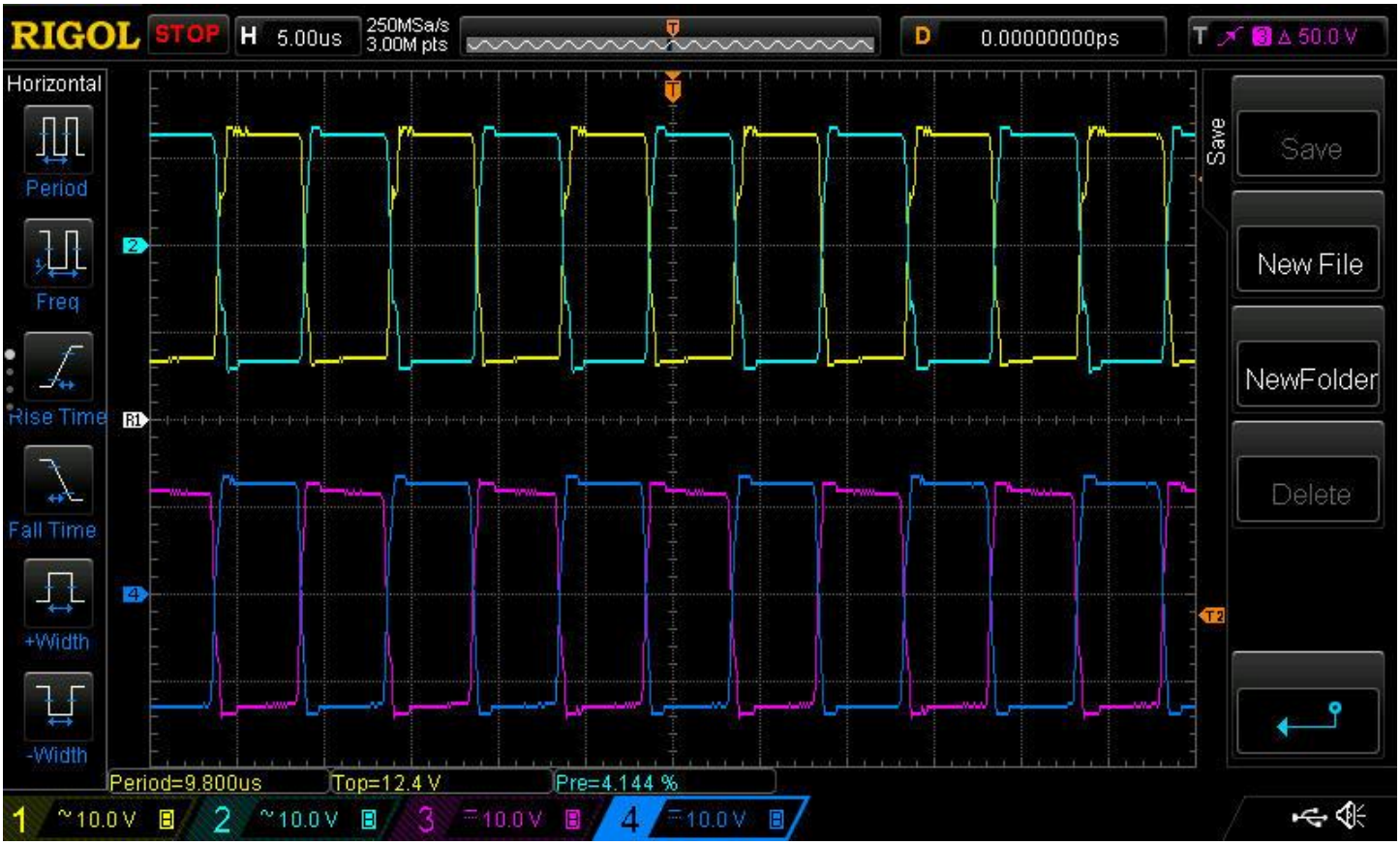


FIGURE 3. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

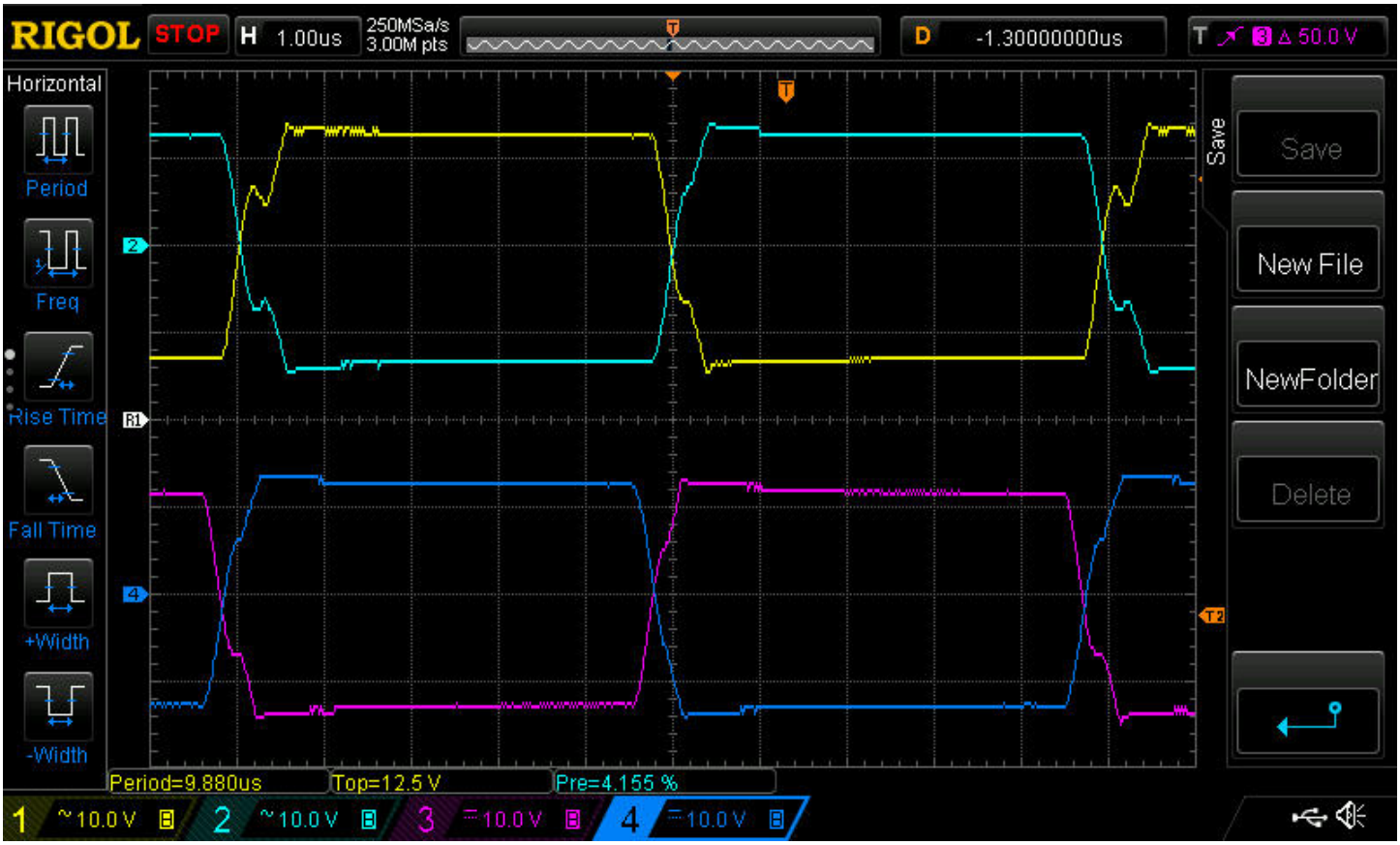



FIGURE 4. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

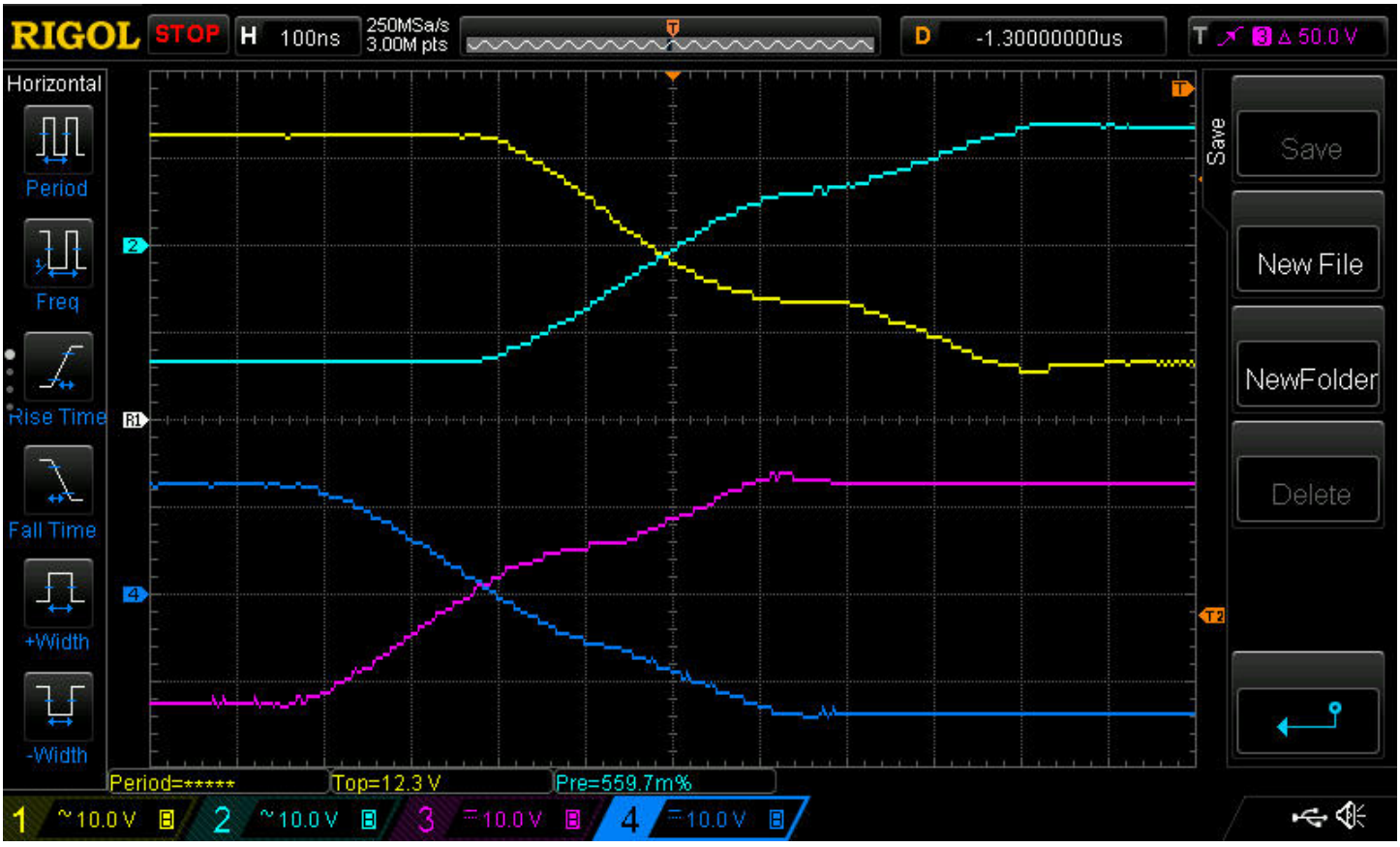


FIGURE 5. TOP WAVEFORM Q1 Q2 AT MOSFET GATE **NO DC LINK**

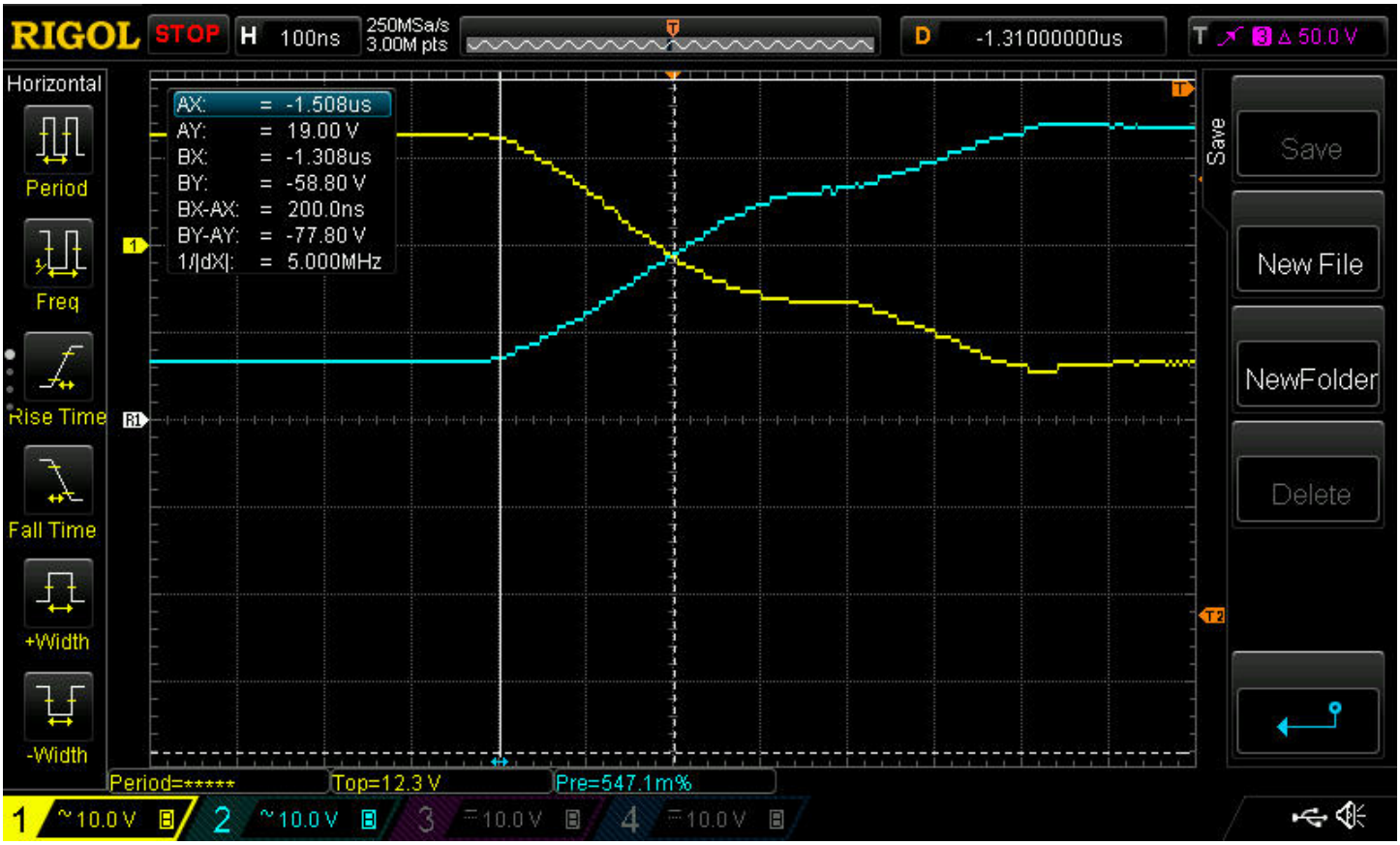



FIGURE 6. TOP WAVEFORM Q1 Q2 AT MOSFET GATE **NO DC LINK**

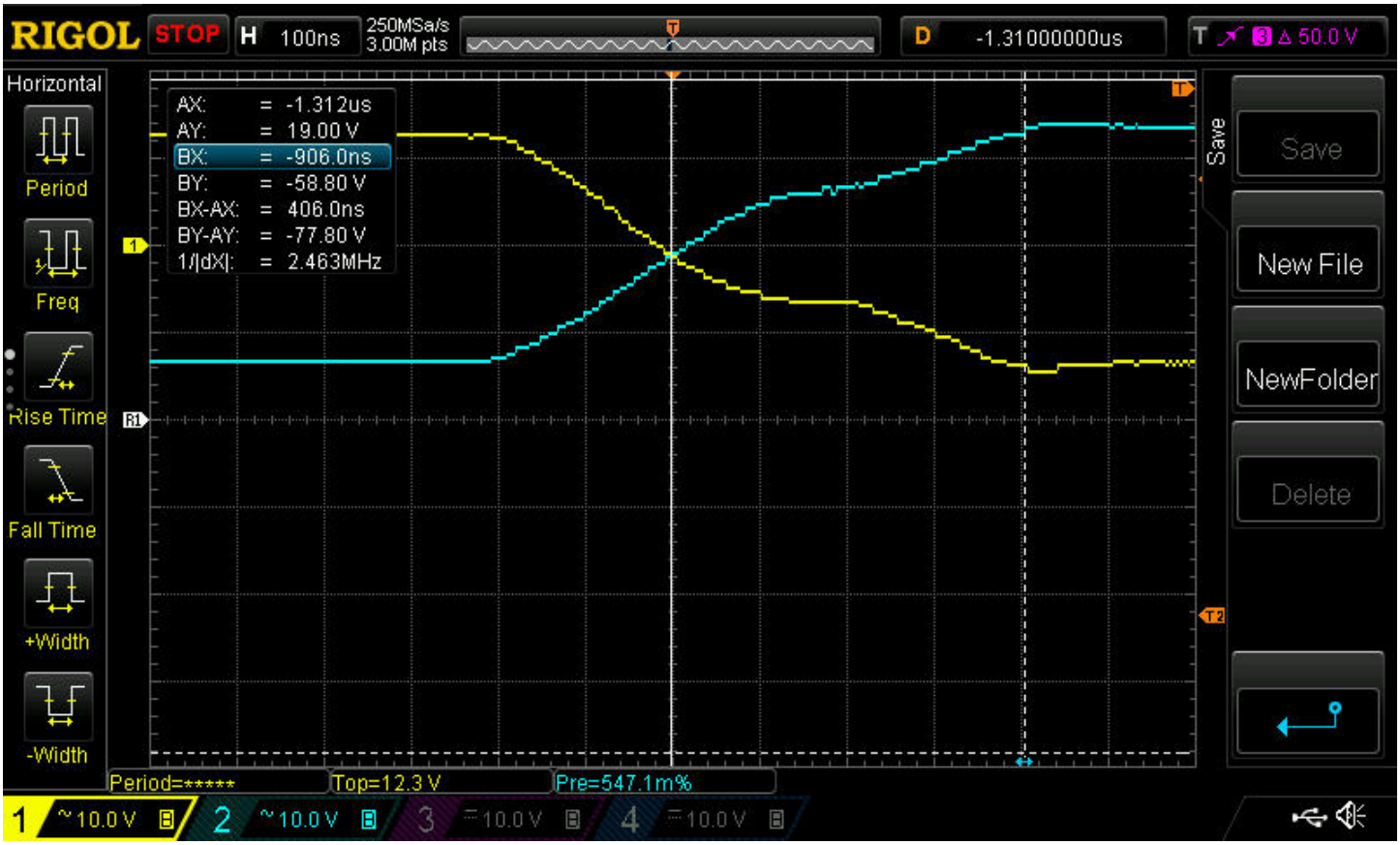


FIGURE 7. BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

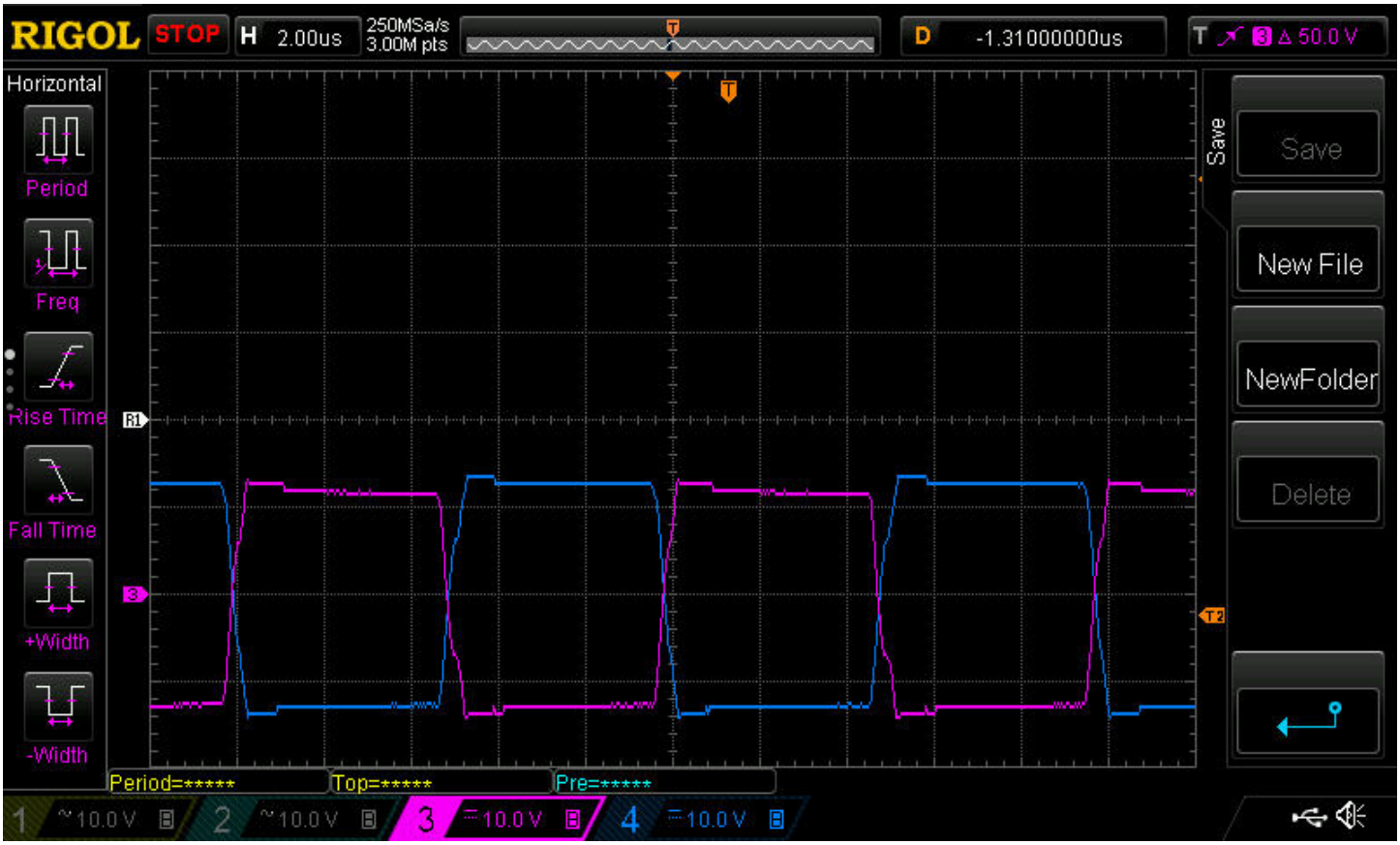



FIGURE 8. BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

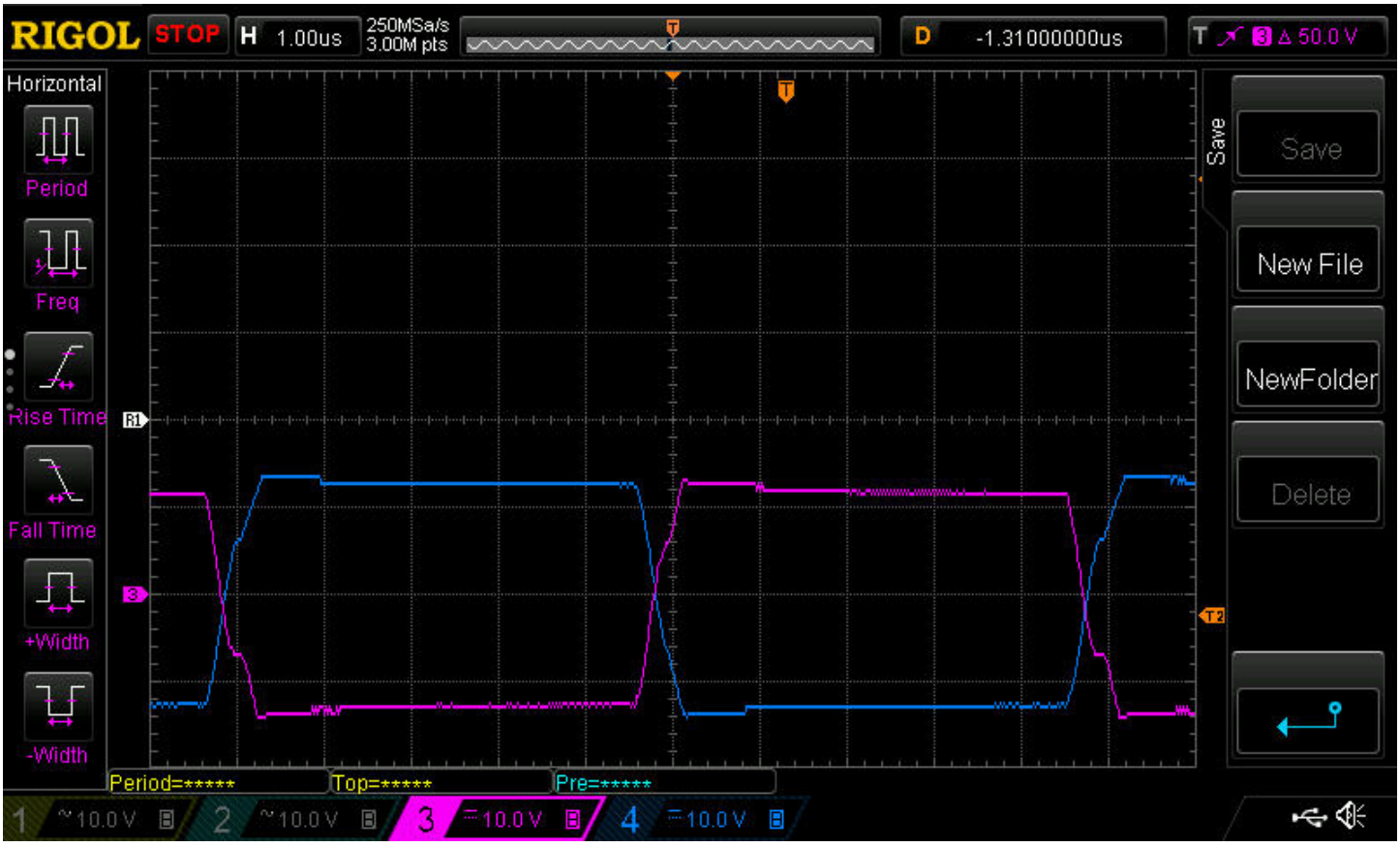


FIGURE 9. BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

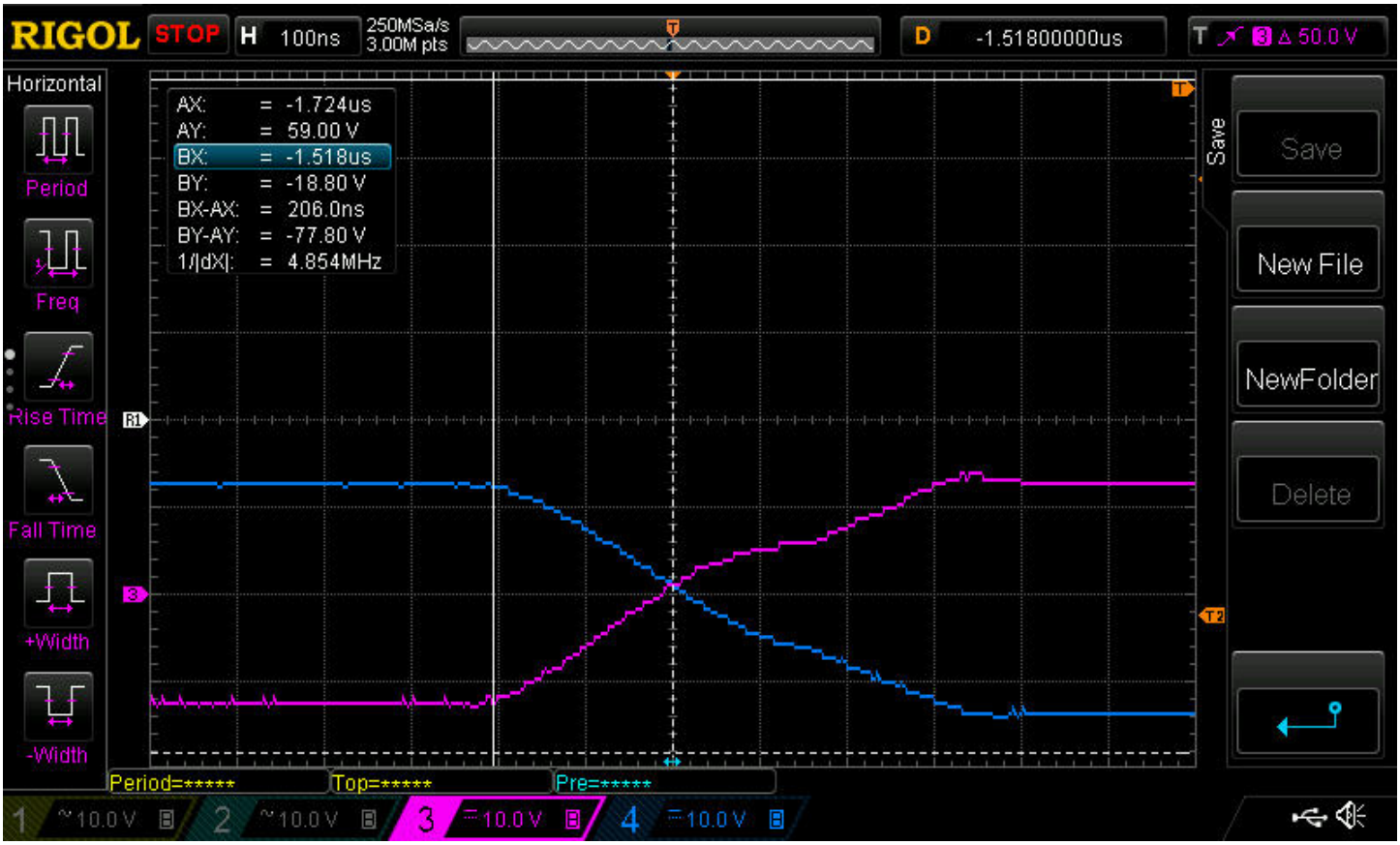



FIGURE 10. BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

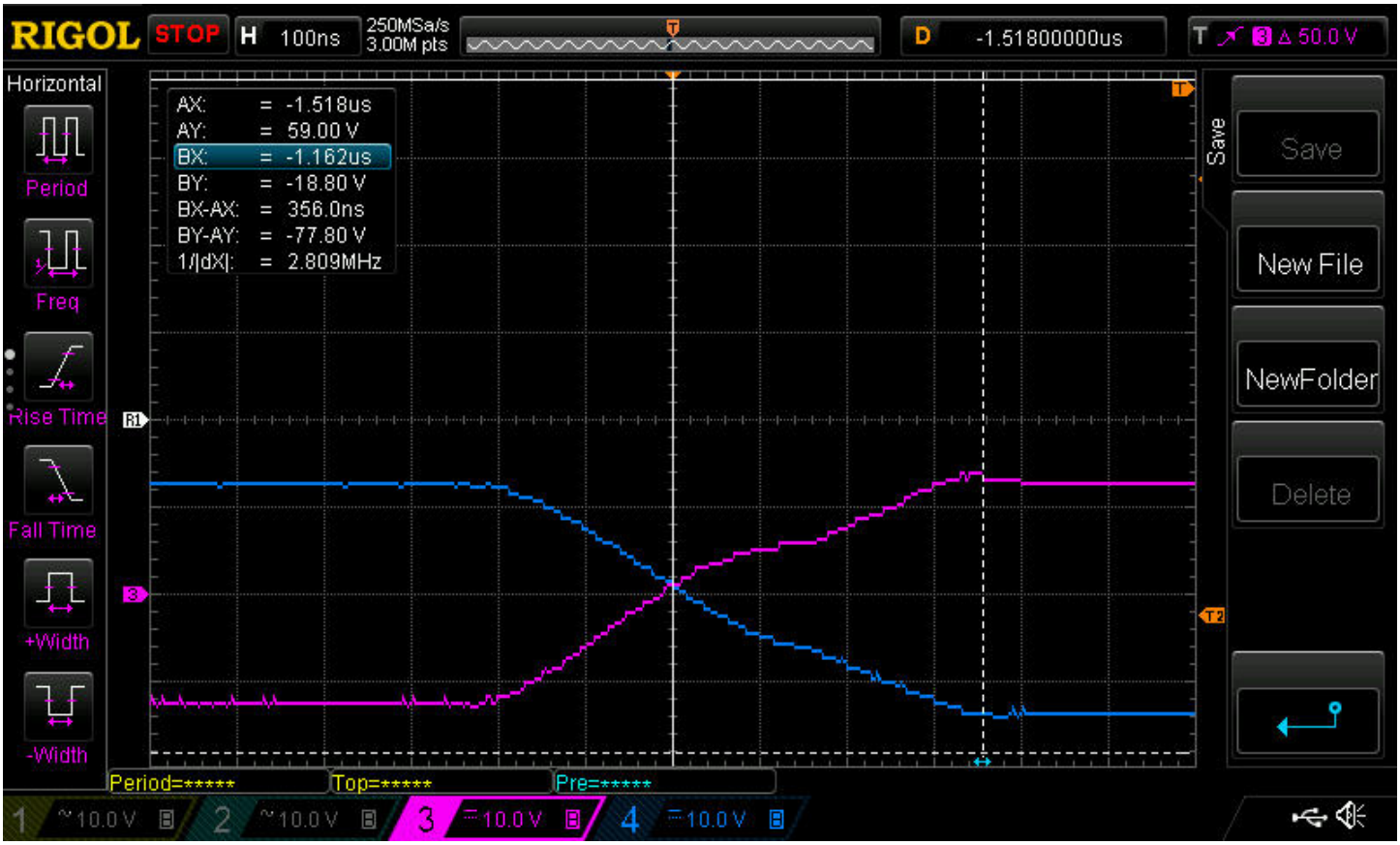


FIGURE 11. BOTTOM WAVEFORM Q3 Q4 AT MOSFET GATE **NO DC LINK**

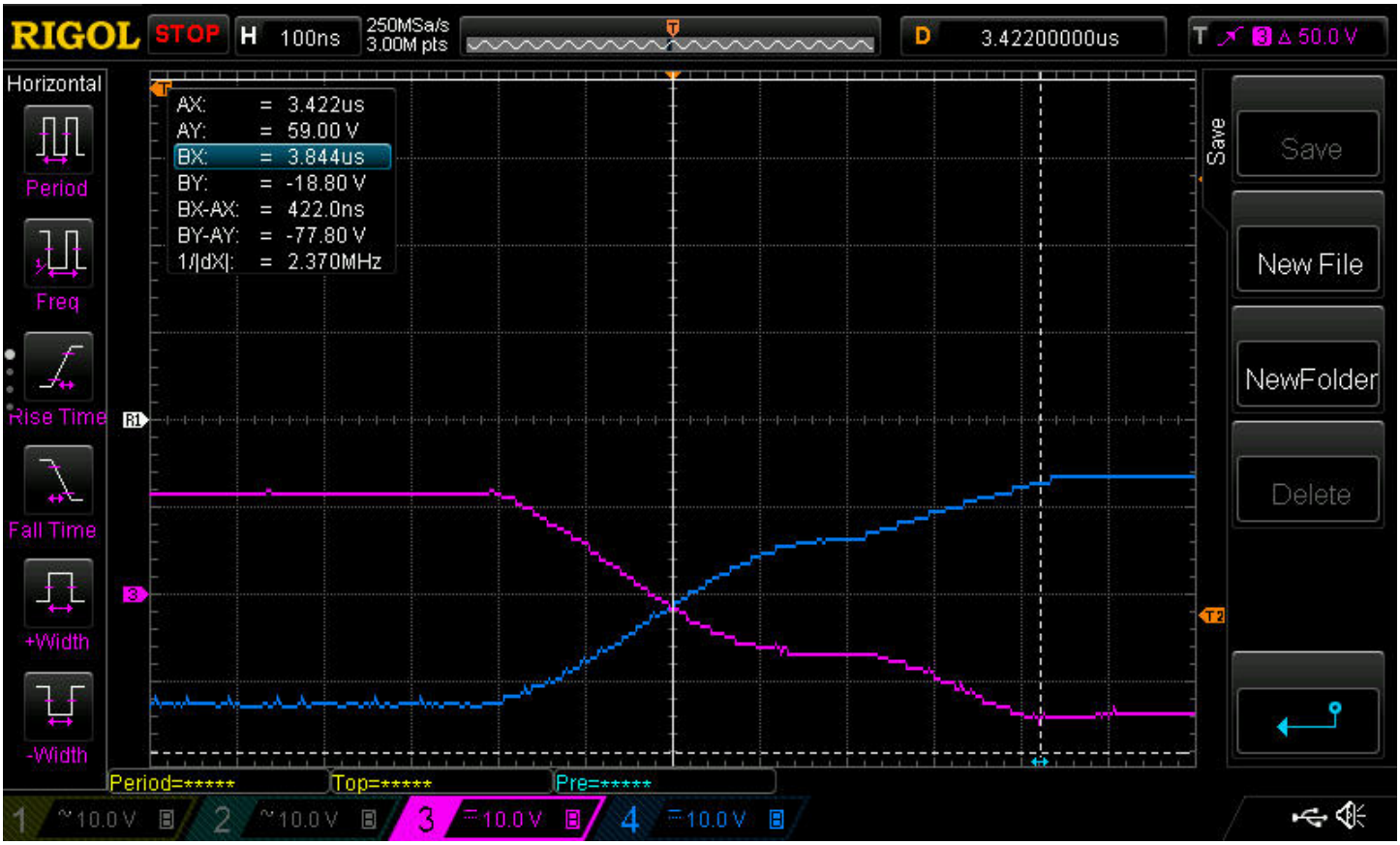



FIGURE 12. TOP WAVEFORM Q1 Q2 AT MOSFET GATE **NO DC LINK**

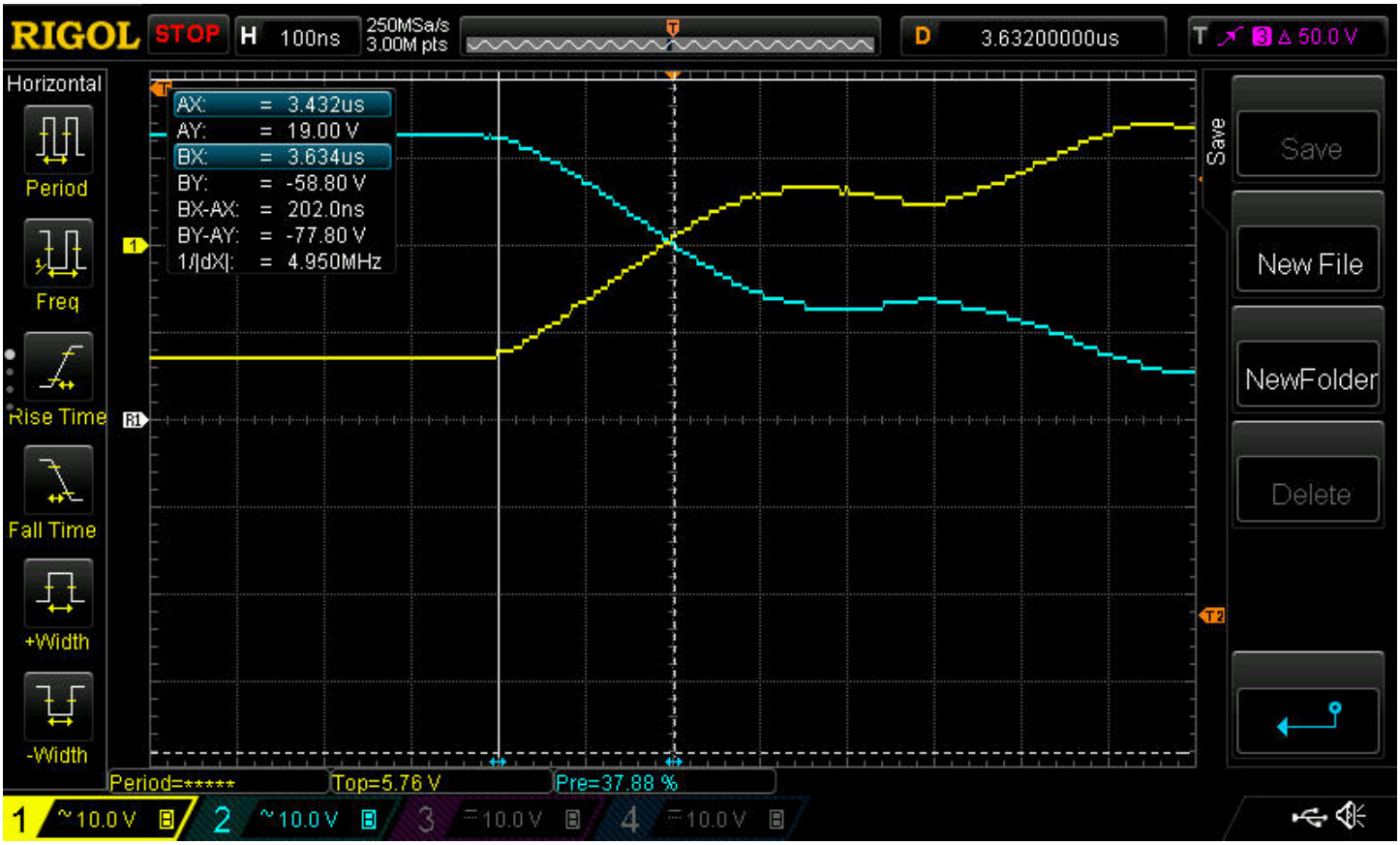


FIGURE 13. TOP WAVEFORM Q1 Q2 AT MOSFET GATE, **__NO DC LINK__ **SOMETHINIG WRONG HERE

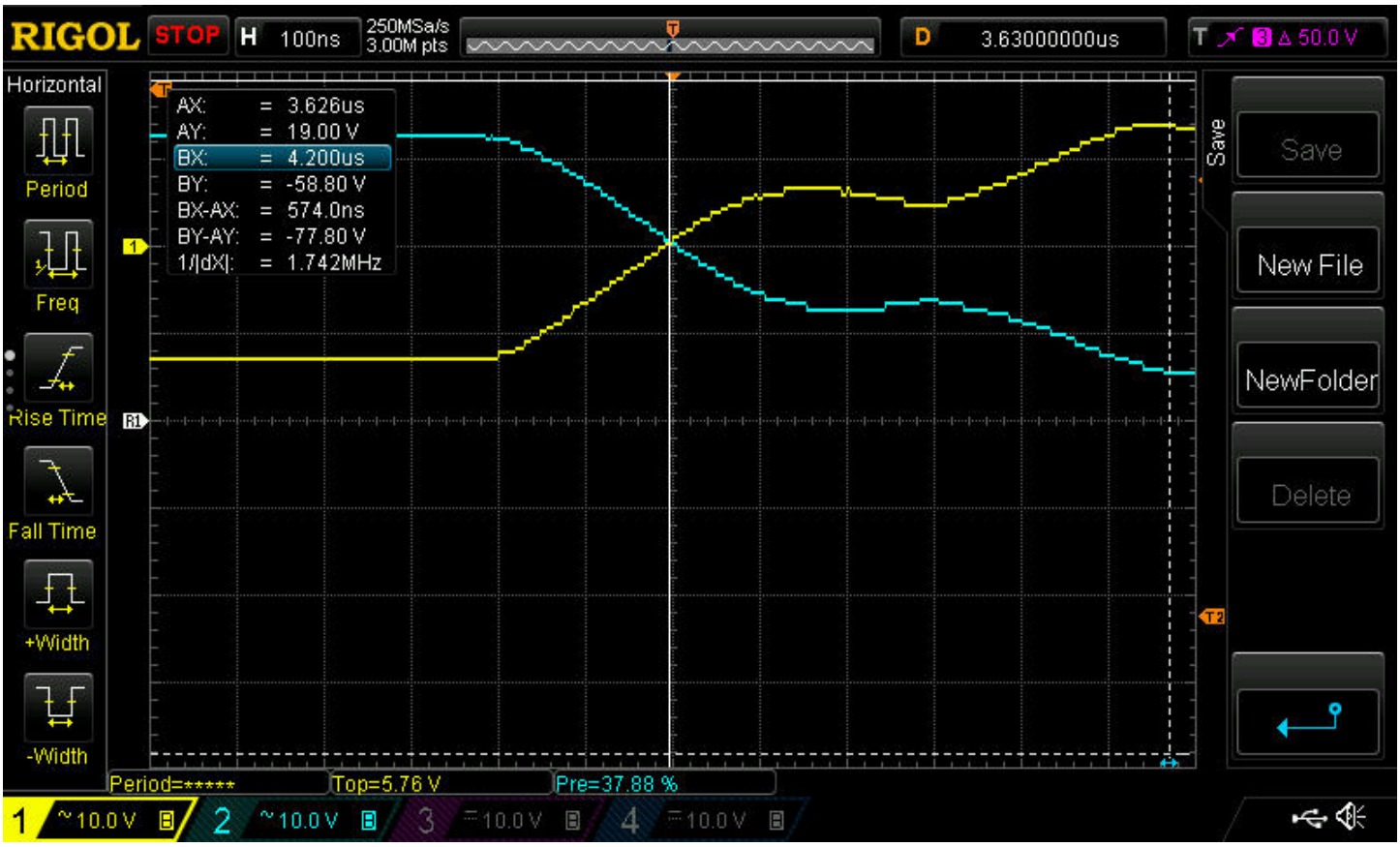


FIGURE 14. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

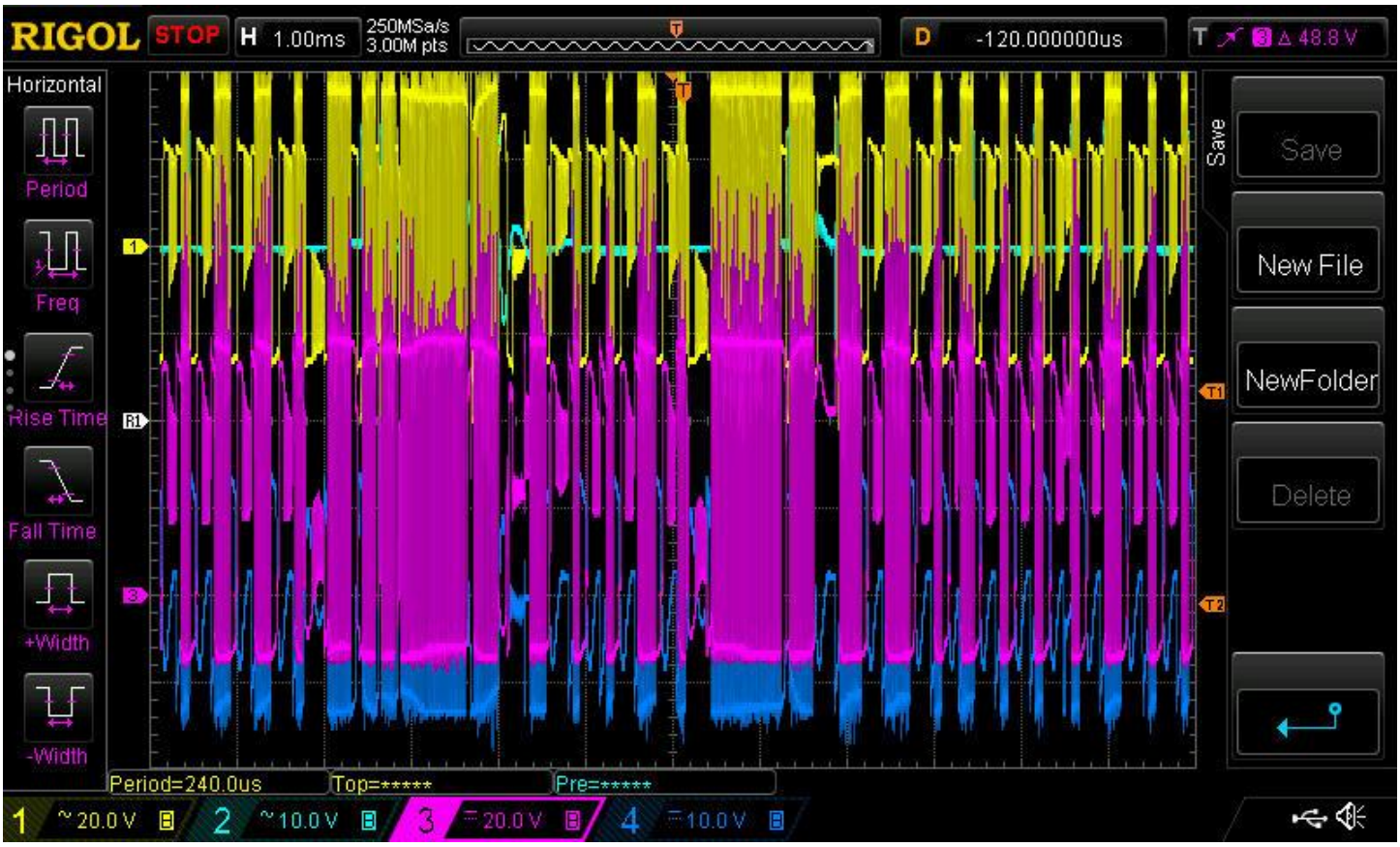



FIGURE 15. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

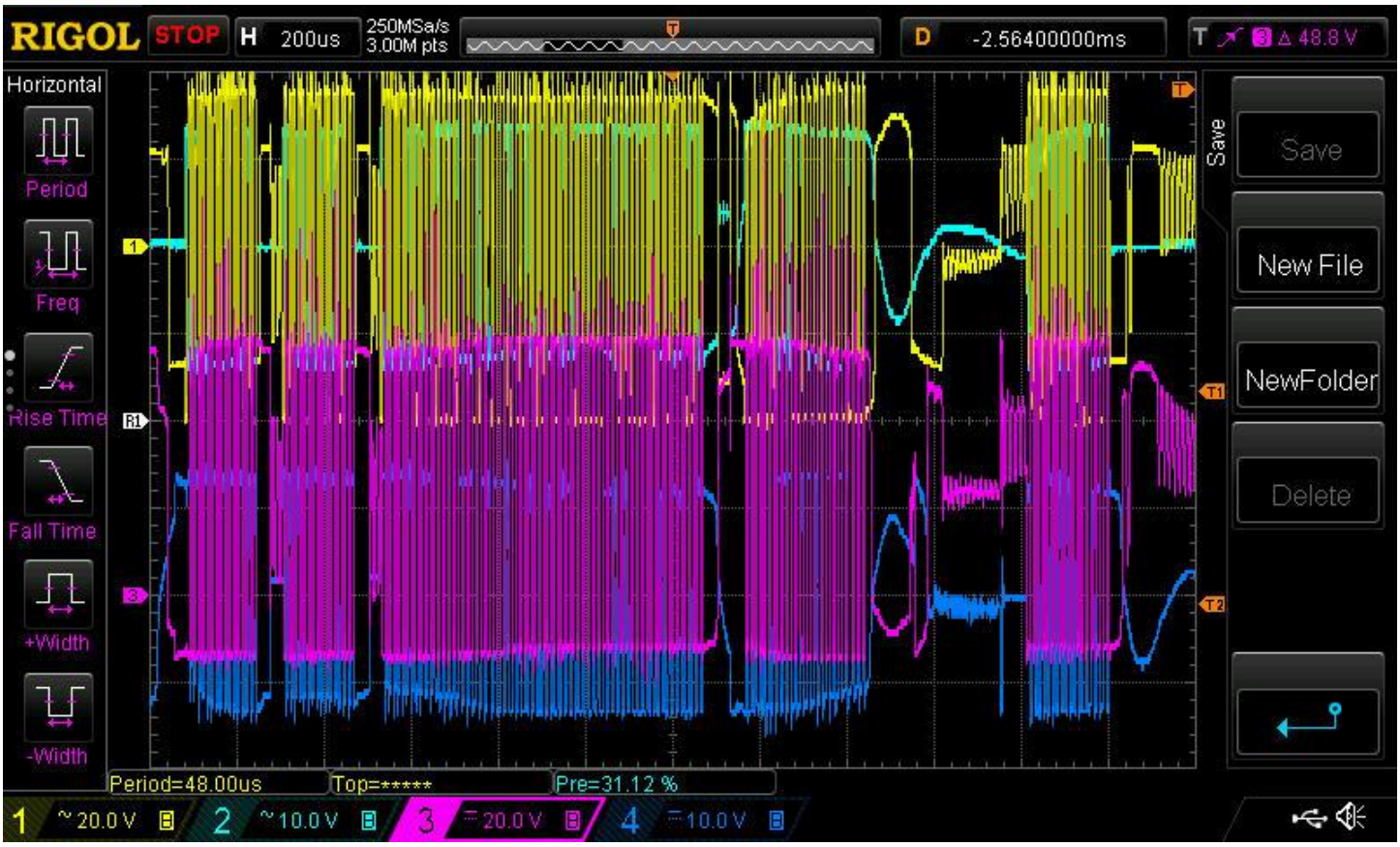


FIGURE 16. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

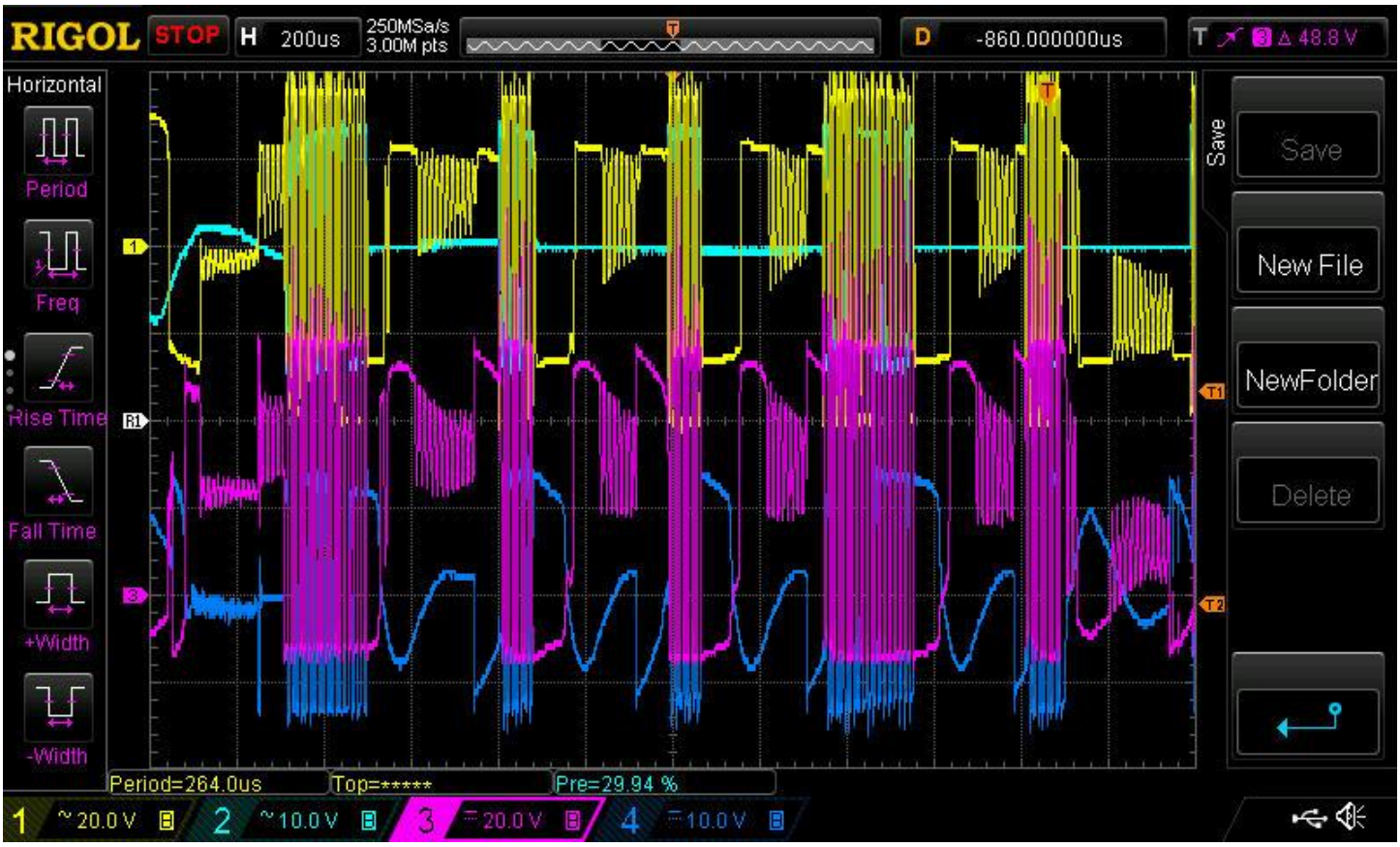



FIGURE 17. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

FIGURE 18. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

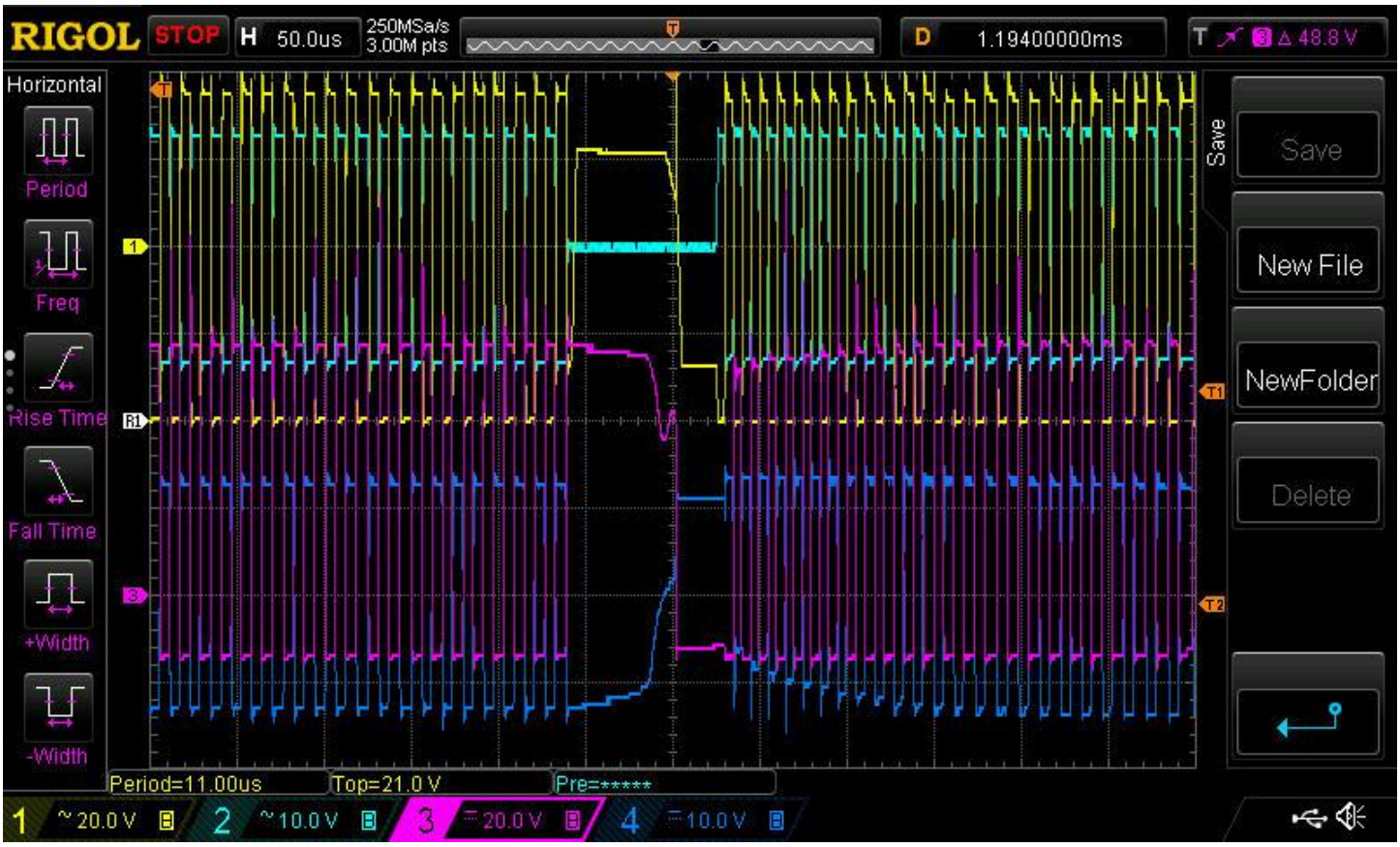



FIGURE 19. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

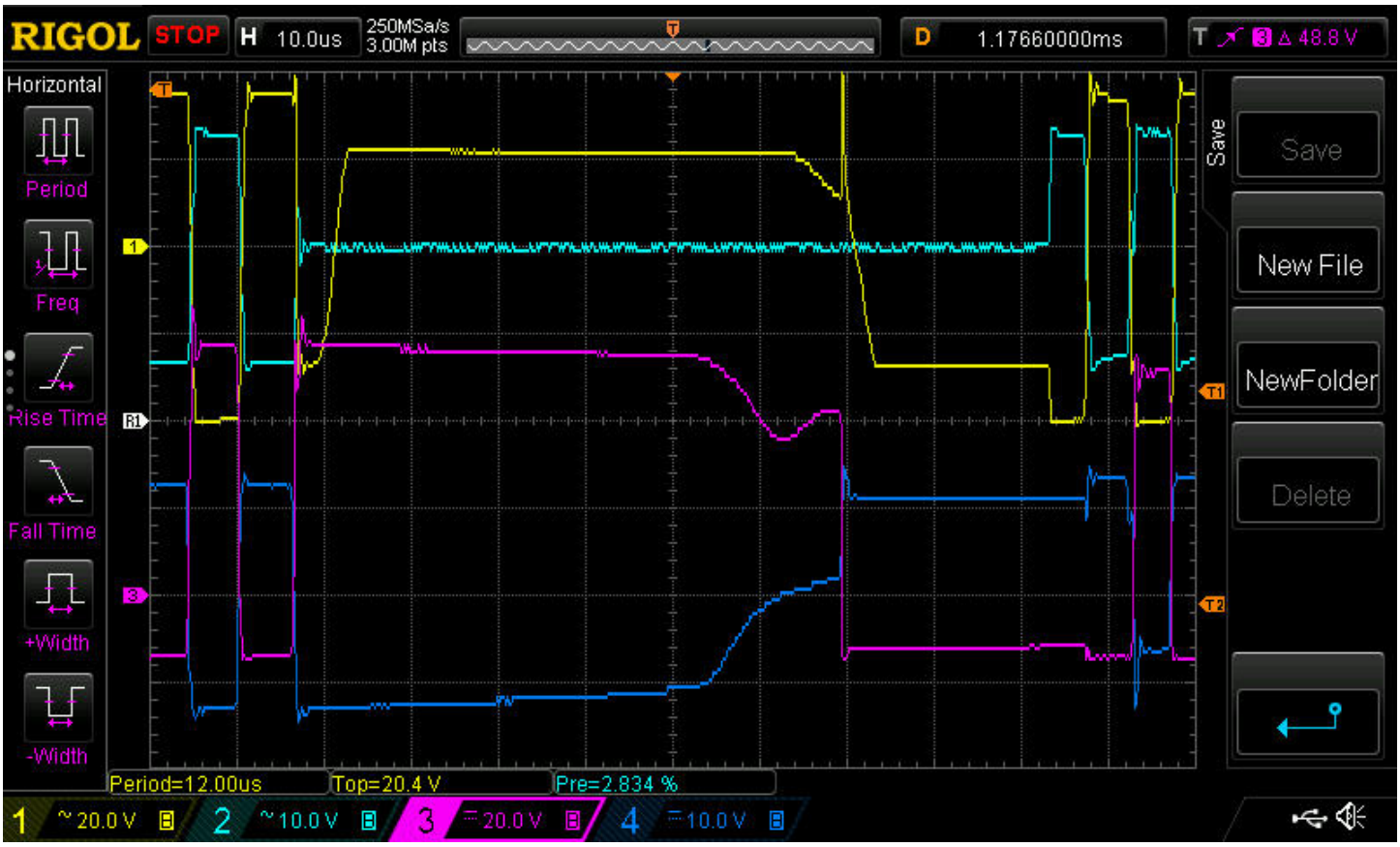


FIGURE 20. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK

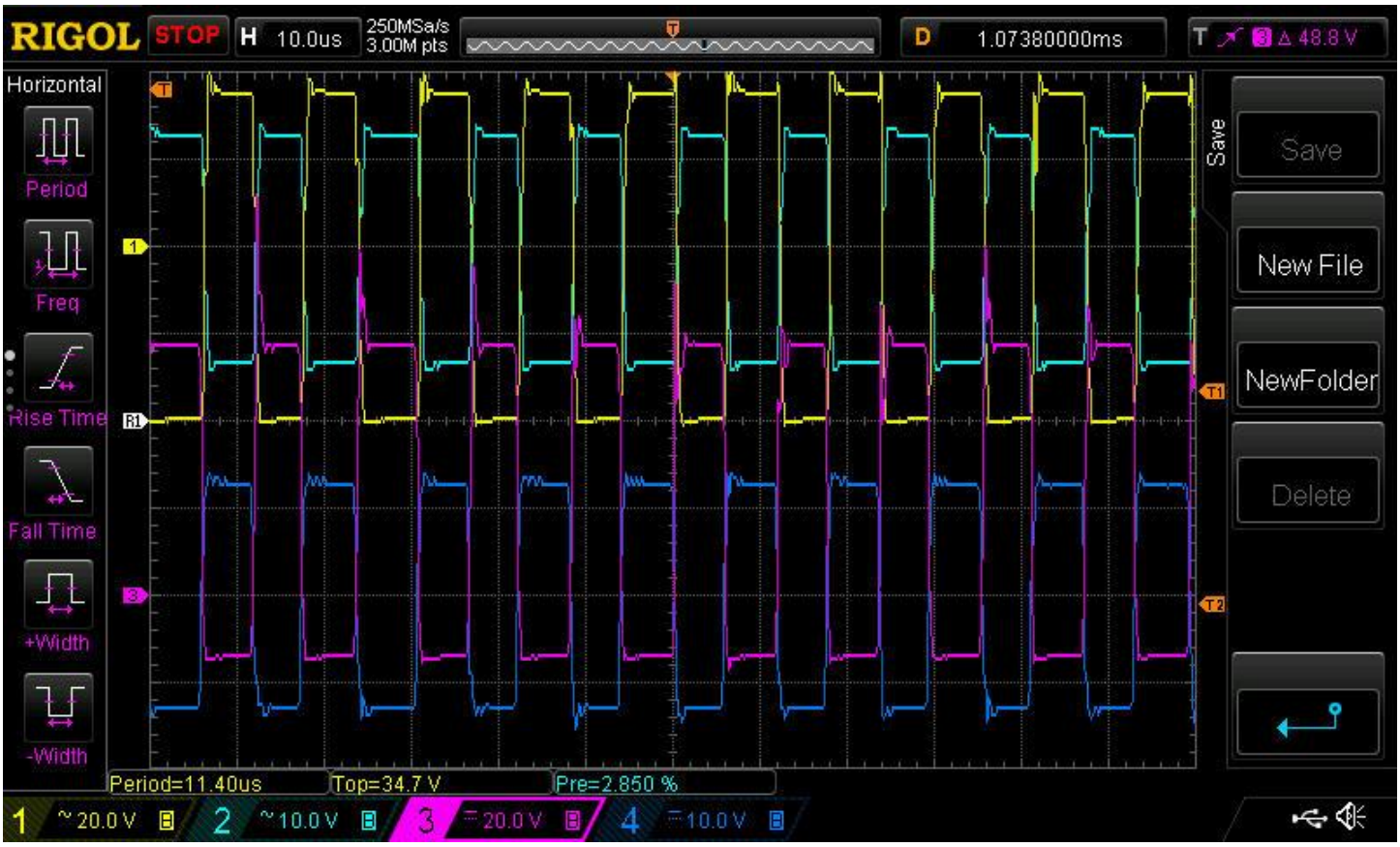



FIGURE 21. TOP WAVEFORM Q1 Q2 GATE, BOTTOM WAVEFORM Q3 Q4 GATE, ROUGHLY 45V DC INK