Experiment 1:

Vbat / P+:19.6V

Vin / PCHG+: 0V -> 21V (regular state).

We expect the LM9061 to open the output.

Figure 1:

CH1: PCHG+

CH2: P+

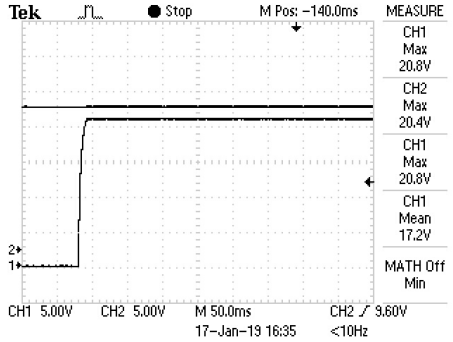


Figure 2:

CH1: PCHG+

CH2: Gate of Q14

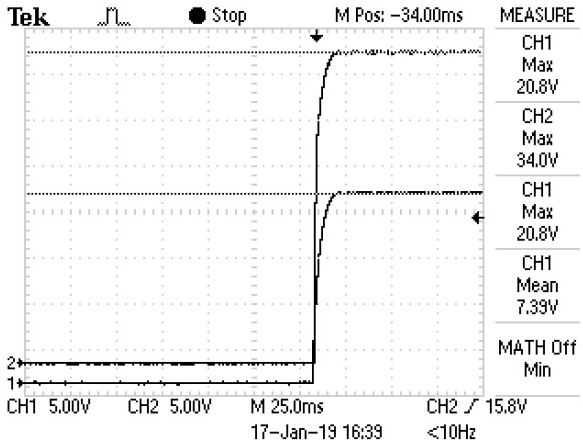
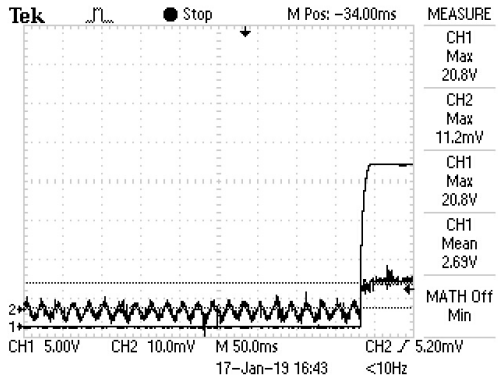


Figure 3:

CH1: PCHG+

CH2: DELAY pin of LM9061



Experiment 2:

Vbat / P+:19.6V

Vin / PCHG+: 0V -> 30V (OVP mode).

We expect the LM9061 **not** to open the output.

Figure 1:

CH1: PCHG+

CH2: P+

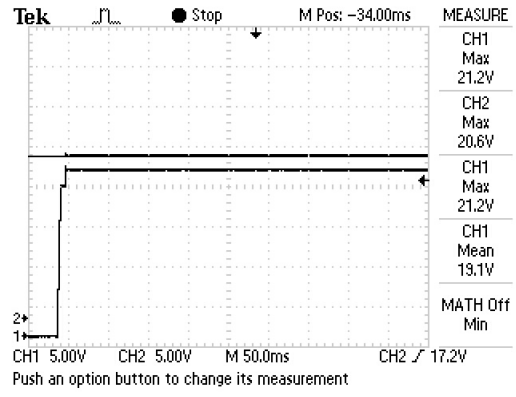
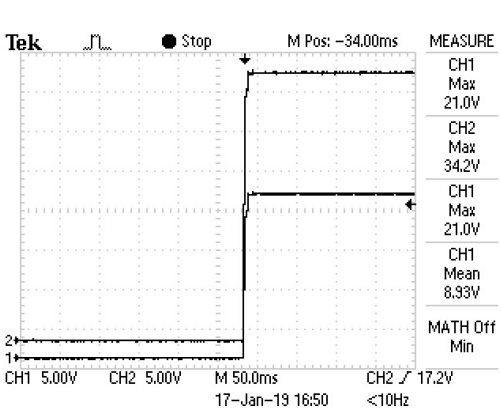


Figure 2:

CH1: PCHG+

CH2: Gate of Q14



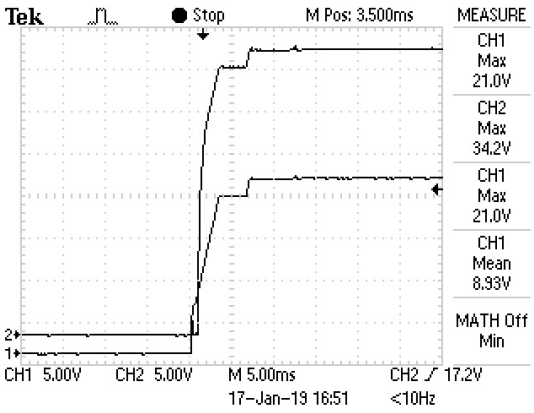


Figure 3:

CH1: PCHG+

CH2: DELAY pin of LM9061