High-Voltage ORing with Low-Voltage Controllers

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This paper describes how a low-voltage (less than 18 V) Or-ing FET controller can be used in a high-voltage (greater than 18 V) application. The controller VDD pin is connected to the system high voltage input and a regulator maintains bias voltage to the controller GND pin. The controller GND is allowed to float with respect to the input voltage.

1.1 Introduction

As design engineers strive for increased reliability and efficiency in their systems they look for reduced losses throughout their design. In some systems such as ATCA, Telecom, and mission critical computing, higher reliability can be achieved by diode OR-ing two Power Supply Units (PSU) to the system as shown in Figure 1-1.

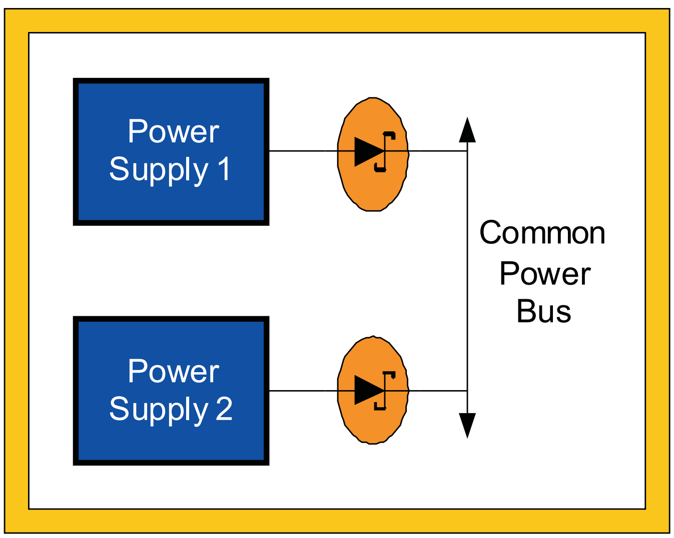

Figure 1-1. Traditional Diode OR

The TPS2412 and TPS2413 are low voltage power supply ORing controllers. The controllers operate a MOSFET to emulate a diode for high efficiency energy transfer. At 18-V input maximum, these controllers were designed for less than 16-V systems allowing 10% tolerance.

Although the TPS2412 might not appear suitable for use with voltage levels greater than 18 V, this application note describes a technique that will allow this low voltage part work at higher voltages.

When a traditional diode is used for OR-ing, losses can be high. Replacing the diodes with a MOSFET and a controller, as shown in Figure 1-2, greater efficiency can be achieved.

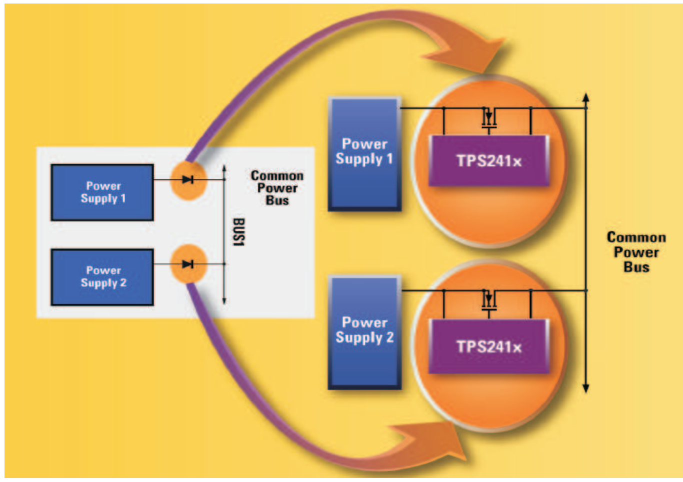

Figure 1-2. TPS241X and MOSFET ORing Solution

The graph in Figure 1-3 illustrates the power savings of the MOSFET solution over the diode for a given current.

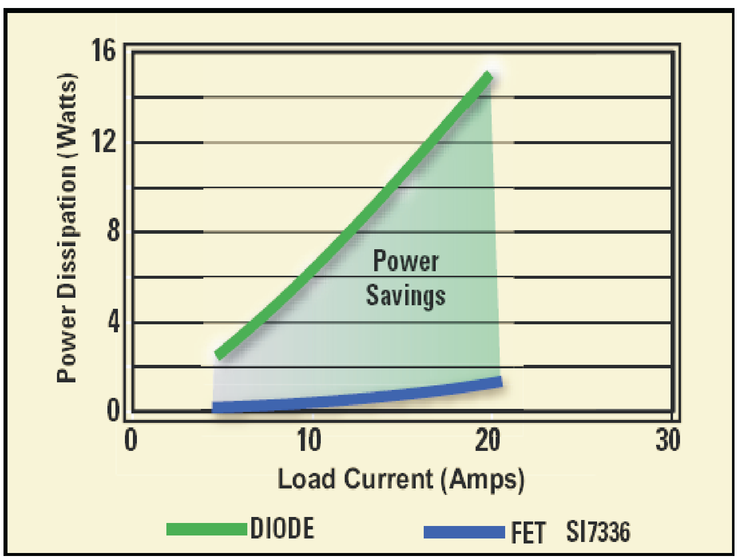

Figure 1-3. Power Savings

A design example of 48 volts is used here but the circuit can be adjusted to control other voltages.

1.2 Schematic

Figure 1-4 shows the schematic for high voltage ORing.

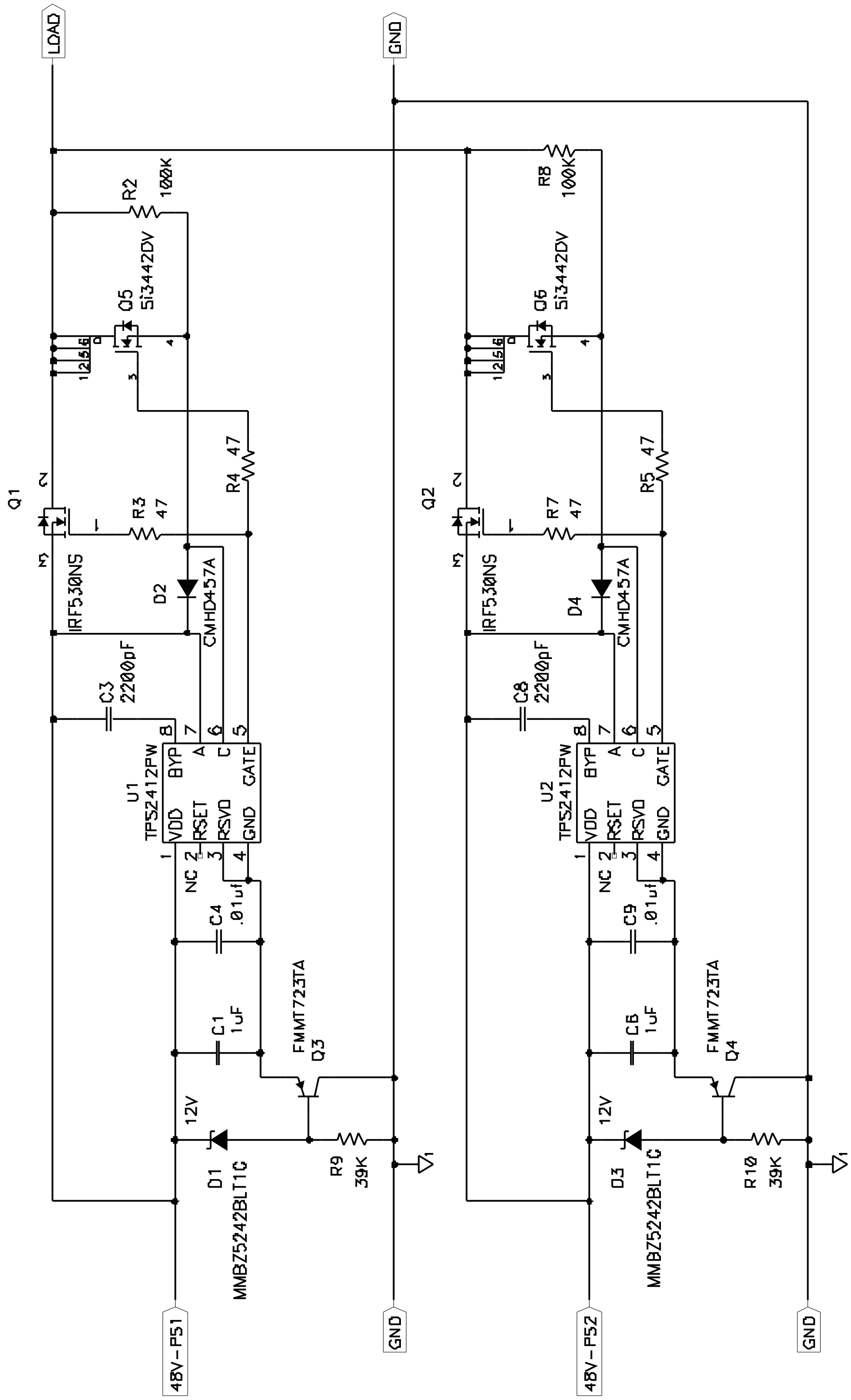

Figure 1-4. TPS2412 Schematic

1.3 Description

1.3.1 Operation

When working with the TPS2412 please reference the schematic, Figure 1-4. The top and bottom half of the schematic are symmetric. Only the reference designators in the top half of the schematic will be addressed.

When the voltage at U1 Pin A is 10 mV or higher than the voltage at Pin C, the gate of the MOSFET, Q1, is turned on. Because the load is referenced to Pin C of U1 and U2, the higher voltage input, either 48V-PS1 or 48V-PS2, is selected to power the load.

The components to the left of U1 make up the voltage regulator used to operate the TPS2412 at 12 volts and prevent it from exposure to the full input supply voltage.

To the right of the TPS2412, the diode D2 is used to prevent the full supply input voltage from being applied from Pin C to Pin A in the event of an input power supply short. R2 is used to limit diode forward current. When D2 is back biased, Q1 and Q5 are on. Q5 maintains a low resistance path between the load and Pin C.

1.3.2 Design Example

A 2-A design was selected. Higher currents may be switched as determined by the selected MOSFET. A single MOSFET was tested but the TPS2412/13 can switch parallel MOSFETs depending on system specifications and MOSFET parameters such as gate capacitance and safe operating area on startup.

The regulator for the TPS2412/13 is made up of D1, R9, Q3 and C1. Please reference the schematic Figure 1-4 throughout the design example section

1.3.3 Regulator

D1, the zener diode, is selected at 12 V to operate the TPS2412/13. R9, providing the bias for the zener.

Set the current to the zener at the minimum input operating voltage. The current at the zener knee is on the component datasheet as I_{ZK} or read from graph of zener voltage vs current. Triple the knee current which is small to account for component tolerances and a slight current to the regulator transistor base. Use Equation 1-1to select the zener bias resistor, R9.

$$R9 = \frac{V_{MIN} - V_Z}{3 \times I_{ZMIN}} = \frac{43V - 12V}{3 \times 0.25mA} = 41.3k\Omega, use\,39k\Omega \quad (1\text{-}1)$$

R9 power rating is calculated in Equation 1-2.

$$P = E \times I = (V_{MAX} - V_Z) \times (3 \times I_{ZMIN}) = (53 - 12) \times (3 \times 0.25mA) = 30mW \quad (1\text{-}2)$$

Find the maximum current to the zener at maximum voltage, Equation 1-3.

$$\frac{(V_{MAX} - V_Z)}{39k\Omega} = \frac{(53V - 12V)}{39k\Omega} = 1.05mA \quad (1\text{-}3)$$

Calculate the zener power rating, Equation 1-4.

$$P = V \times I = 12V \times 1.05mA = 12.6mW \quad (1\text{-}4)$$

Capacitor C1 is chosen for regulator stability. The value is calculated to sustain the TPS2412 through a 10-ms voltage drop out.

$$C = \frac{(I \times T)}{V} = \frac{(1mA \times 10ms)}{9} = 1.1\mu F, use\,1.0\mu F \quad (1\text{-}5)$$

1.3.4 Decoupling Capacitor

C4 is a standard 0.01-µF decoupling capacitor for the TPS2412/13

1.3.5 Regulator Transistor Selection

Q3 is used to operate the regulator efficiently over the input voltage range reducing the power dissipation in D1 and R9. Selection criteria of the PNP transistor Q3 is:

- V_{CE} is double the system voltage to withstand transient
- I_C rating is 20 mA minimum (TPS2412 I_{DD} is 1 to 6 mA, de-rate for temperature)
- Power is less than:

$$(V_{MAX} - V_Z) \times I_C\, actual = (53V - 12V) \times 6mA = 246mW$$

1.3.6 Bypass Capacitor

C3 stabilizes the TPS2412 charge pump. The recommended bypass capacitor in the TPS2412 datasheet is 2200 pF.

1.3.7 Gate Pin Isolation

R3 is a small value, usually between 10 and 47 Ω to add some isolation of the gate pin from parasitic capacitance in the circuit traces and MOSFET.

1.3.8 Voltage TPS2412 Pin C to Pin A (VCA) Clamp

If 48V-PS1 is shorted to GND and 48V-PS2 is at normal output, V_{CA} will exceed specification. D2 is in the circuit to clamp V_{CA} to 0.7 preventing over-voltage. R2 is placed between the load and Pin C to apply the output voltage to Pin C when Q1 is off. R2 is subject to high voltage. A high impedance resistance value was selected to keep the power dissipation in R2 small. Equation 1-6 is used to calculate the power rating of R2.

$$(V_{MAX} - V_Z) \times I_C\, actual = (53V - 12V) \times 6mA = 246mW \tag{1-6}$$

Together with the leakage current in D2, R2 will alter the voltage at Pin C.

When Q1 is on, Q5 is on to keep a low impedance path from the load to Pin C. This gives a tighter control for fast turn off of Q1.

1.4 List of Materials for the TPS2412 High Voltage OR

Table 1-1. List of Materials

REF DES	COUNT	DESCRIPTION	PART NUMBER	MFR
C1, C6	2	Capacitor, ceramic, 1 µF, 1210	STD	Vishay
C3, C8	2	Capacitor, ceramic, 2200 pF, 805	STD	muRata
C4, C9	2	Capacitor, ceramic, 0.01 µF, 805	STD	muRata
D1, D3	2	Diode, Zener, 12 V, 225 mW, SOT-23	MMBZ5242BLT1 G	ON Semi
D2, D4	2	Diode IF 500 mA, IR 5 µA, SOD-123	CMHD457A	Central Semi
Q1, Q2	2	Transistor, NFET, 100 V, 33 A, 44 mΩ, D2PAK	IRF530NS	IR
Q3, Q4	2	Transistor, PNP power switching, VCE -100 V, 625 mW, SOT23	FMMT723TA	Zetex
Q5, Q6	2	MOSFET, N-channel, 20 V, 5 A, 70 mΩ, TSOP-6	Si3442DV	Vishay
R2, R8	2	Resistor, chip, 1/10 W, 1%, 100 kΩ, 805	STD	Vishay
R3, R4, R5, R7	4	Resistor, chip, 1/10 W, 1%, 47 Ω, 805	STD	Vishay
R9, R10	2	Resistor, chip, 1/10 W, 1%,39 kΩ , 805	STD	Vishay
U1, U2	2	Device, N+1 and Oring power rail controller, TSSOP-14	TPS2412PW	TI

1.5 Performance Data

The scope trace of Figure 1-5 shows a case where PS1 is set to 48 volts and PS2, not shown is set to 47 volts. There is no bulk capacitance at the input or output terminals of the ORing circuit. The dc load is 2 A.

The input terminals, 48-PS1 to GND, are shorted with a screw driver. The resultant drop in PS1 voltage turns off Gate MOSFET1 and turns on the Gate MOSFET2.

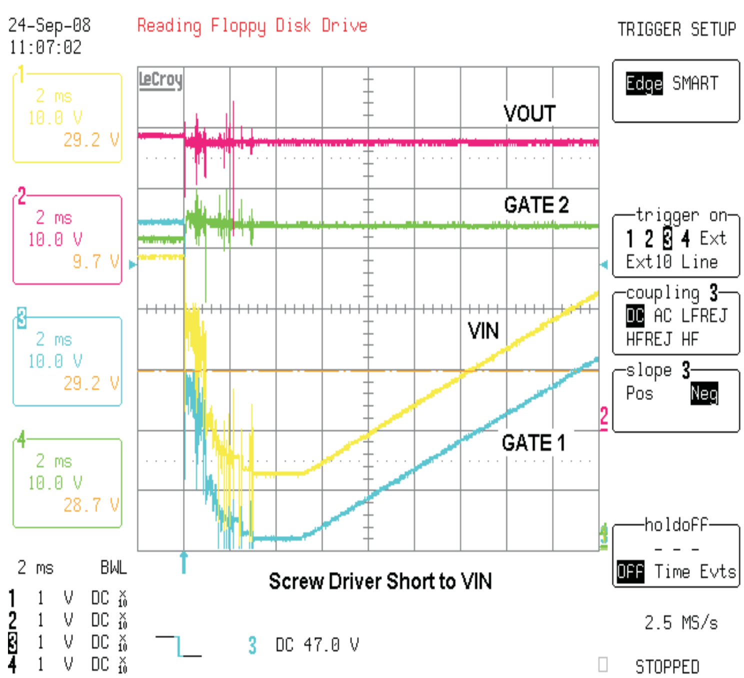

Figure 1-5. Scope Trace of High Voltage OR-ing with Screw Driver Short to PS1.