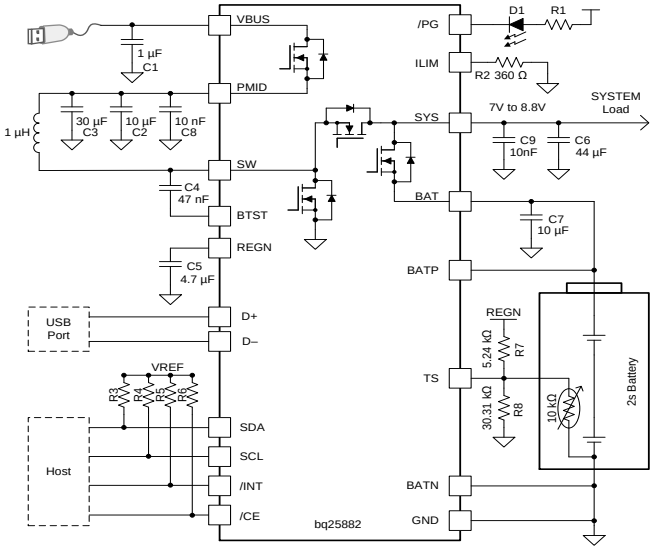
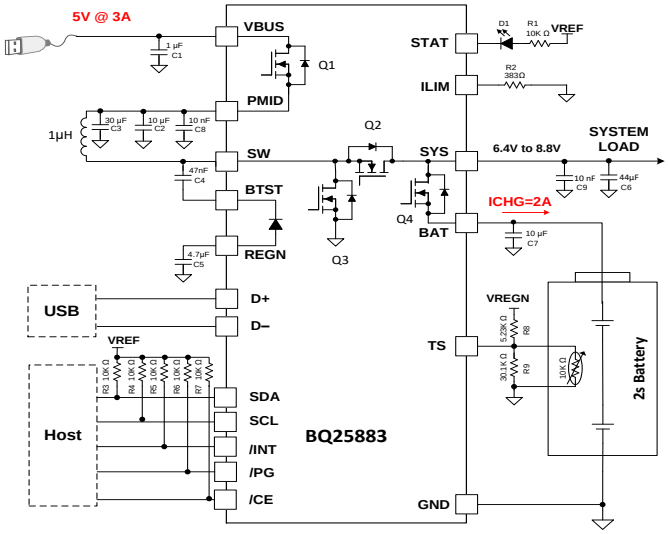
BQ25882 Schematic



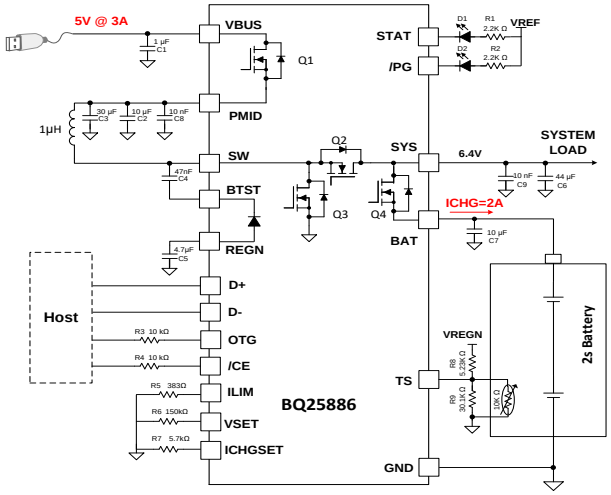
DESIGN CHECKLIST									
PIN NAME		**REQUIREMENT**	**COMPONENT**	**MIN**	**TYP**	**MAX**	**DESCRIPTION**	**COMMENTS AND RELEVANT EQUATIONS**	**PCB Placement**
VBUS	A1, B1	Required	C1		1 uF		Input supply	Place C1 as close to the IC as possible	Place C1 as close to the IC as possible
PMID	A2, B2	Required	C2		10 uF		Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
		Recommended	C3		30 uF		Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor for high frequency EMI filtering	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	D5	Required	C4		47 nF		PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	B4	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap from REGN to GND	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
SYS	B5	Required	C6		44 uF		System connection	Boost converter output. Connect at least 2 x 22 uF capacitance after derating closely to the SYS pin and GND	Place as close to the IC as possible.
		Optional	C9		10 nF		Optimal EVM performance	Place 0402 10 nF capacitor from SYS pin to GND	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	C4, C5	Required	C7		10 uF		Battery Power connection	Minimum 10 uF capacitance after derating closely to BAT pin and GND	Place as close to the IC as possible.
BATN	E4						Negative battery sense terminal	Kelvin connect as close as possible to negative battery terminal	
BATP	E5						Positive battery sense terminal	Kelvin connect as close as possible to positive battery terminal	
ILIM	D3	Recommended	R2		*Ω		Input current limit resistor programming	IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground.	
SDA	E2	Recommended	R2		10 kΩ		I2C interface data		
SCL	D2	Recommended	R4		10 kΩ		I2C interface clock		
/INT	C3	Recommended	R5		10 kΩ		Open drain active Interrupt Output		
/PG	C2	Recommended	R6		*kΩ		Open drain active low power good indicator	Current limiting resistor	
/CE	E1	Recommended	R7		10 kΩ		Active low charge eneable pin	/CE pin is internally pulled low with 900-kΩ resistor	
TS	E3	Required	R8		*Ω		Resistor network to set window for thermistor temperature-based battery charging profile	$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{T_{T3}} - \frac{1}{T_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{T_{T2}} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{T_{T3}} - 1\right)}$ $RT1 = \frac{\frac{1}{T_{T2}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$	
		Required	R9		*Ω				
D+	C1						Positive USB data line		
D-	D1						Negative USB data line		
SW	A4, A5	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	A3, B3						Ground return		

BQ25883 Schematic



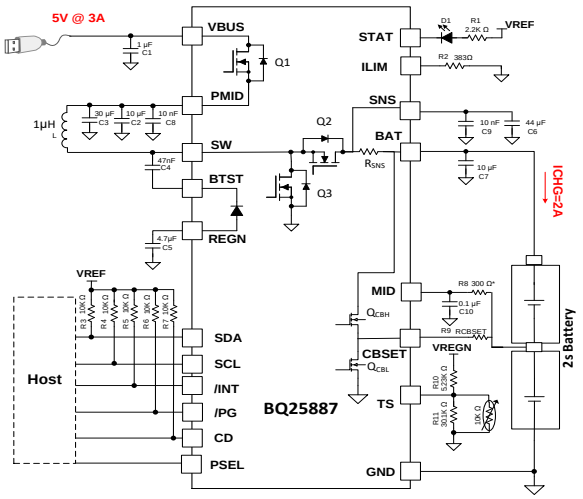
DESIGN CHECKLIST									
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	23	Required	C1		1 uF		Input supply		Place C1 as close to the IC as possible
PMID	21, 22	Required	C2		10 uF		Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, nominal is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
		Recommended	C3		30 uF		Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	12	Required	C4		47 nF		PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	11	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
SYS	15, 16	Required	C6		44 uF		System connection	Boost converter output. Connect at least 2 x 22 uF nominal capacitance closely to the SYS pin and PGND	Place as close to the IC as possible.
		Optional	C9		10 nF		Optimal EVM performance	Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	13, 14	Required	C7		10 uF		Battery Power connection	Minimum 10 uF nominal capacitance closely to BAT pin and GND	Place as close to the IC as possible.
STAT	2	Recommended	R1		*kΩ		Charging status indicating LED	Current limiting resistor	
		Optional	D1				Charging status indicating LED		
ILIM	8	Recommended	R2		*Ω		Input current limit resistor programming	IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground.	
SDA	4	Recommended	R2		10 kΩ		I2C interface data		
SCL	5	Recommended	R4		10 kΩ		I2C interface clock		
/INT	6	Recommended	R5		10 kΩ		Open drain active Interrupt Output		
/PG	9	Recommended	R6		*kΩ		Open drain active low power good indicator	Current limiting resistor	
/CE	3	Recommended	R7		10 kΩ		Active low charge eneable pin		
TS	7	Required	R8		*Ω		Resistor network to set window for thermistor temperature-based battery charging profile	$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{T_{T2}} - \frac{1}{T_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{T_{T1}} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{T_{T3}} - 1\right)}$ $RT1 = \frac{\frac{1}{T_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$	
		Required	R9		*Ω				
D+	24						Positive USB data line		
D-	1						Negative USB data line		
SW	17, 18	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	19, 20						Ground return		
PwrPad	-						IC Thermal dissipation pad	http://www.ti.com/lit/an/snva183b/snva183b.pdf	Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow EVM design.

BQ25886 Schematic



DESIGN CHECKLIST									
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	23	Required	C1		1 uF		Input supply		Place C1 as close to the IC as possible
PMID	21, 22	Required	C2		10 uF		Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
		Recommended	C3		30 uF		Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	12	Required	C4		47 nF		PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	11	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
SYS	15, 16	Required	C6		44 uF		System connection	Boost converter output. Connect at least 2 x 22 uF capacitance after derating closely to the SYS pin and PGND	Place as close to the IC as possible.
		Optional	C9		10 nF		Optimal EVM performance	Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	13, 14	Required	C7		10 uF		Battery Power connection	Minimum 10 uF capacitance after derating closely to BAT pin and GND	Place as close to the IC as possible.
STAT	2	Recommended	R1		*kΩ		Charging status indicating LED	Current limiting resistor	
		Optional	D1				Charging status indicating LED		
/PG	9	Recommended	R2		*kΩ		VBUS power good status indicating LED	Current limiting resistor	
		Optional	D2				VBUS power good status indicating LED		
OTG	5	Recommended	R3		10 kΩ		Active high OTG enable pin	Pull OTG pin high to enable OTG function	
/CE	3	Recommended	R4		10 kΩ		Active low charge eneable pin	/CE pin is internally pulled low with 900-kΩ resistor	
ILIM	8	Recommended	R5		*Ω		Input current limit resistor programming	IINMAX = KILIM / R5. If ILIM is not used, pull ILIM to ground to set the input current limit to maximum.	
VSET	6	Recommended	R6		*kΩ		Battery charge voltage limit	RVSET< 18kΩ (short to GND) = 8.2 V RVSET= 39kΩ (±10%) = 8.8 V RVSET= 75kΩ (±10%) = 8.7 V RVSET> 150kΩ (floating) = 8.4 V	
ICHGSET	10	Recommended	R7		*Ω		Battery charge voltage limit	ICHG=RICHGSET/KICHGSET. Precharge and termination current is 1/10 of the fasst charge current. Shorting ICHGSET to GND clamps the charge currrent to 30mA (typ). Floating ICHGSET disables charger.	
TS	7	Required	R8		*Ω		Resistor network to set window for thermistor temperature-based battery charging profile	$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{V_{T3}} - \frac{1}{V_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{V_{T3}} - 1\right)}$ $RT1 = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$	
		Required	R9		*Ω				
D+	24						Positive USB data line		
D-	1						Negative USB data line		
SW	17, 18	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	4, 19, 20						Ground return		
PwrPad	-						IC Thermal dissipation pad	http://www.ti.com/lit/an/snva183b/snva183b.pdf	Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow EVM design

BQ25887 Schematic



DESIGN CHECKLIST									
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	23	Required	C1		1 uF		Input supply		Place C1 as close to the IC as possible
PMID	21, 22	Required	C2		10 uF		Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
		Recommended	C3		30 uF		Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	12	Required	C4		47 nF		PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	11	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
SYS	15, 16	Required	C6		44 uF		System connection	Boost converter output. Connect at least 2 x 22 uF capacitance after derating closely to the SYS pin and PGND	Place as close to the IC as possible.
		Optional	C9		10 nF		Optimal EVM performance	Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	13, 14	Required	C7		10 uF		Battery Power connection	Minimum 10 uF capacitance after derating closely to BAT pin and GND	Place as close to the IC as possible.
STAT	2	Recommended	R1		*kΩ		Charging status indicating LED	Current limiting resistor	
		Optional	D1				Charging status indicating LED		
ILIM	8	Recommended	R2		*Ω		Input current limit resistor programming	IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground to set the input current limit to maximum.	
SDA	4	Recommended	R3		10 kΩ		I2C interface data		
SCL	5	Recommended	R4		10 kΩ		I2C interface clock		
/INT	6	Recommended	R5		10 kΩ		Open drain active Interrupt Output		
/PG	1	Recommended	R6		*kΩ		VBUS power good status indicating LED	Current limiting resistor	
CD	3	Recommended	R7		10 kΩ		Active high chip disable	Pull CD low to enable the IC. Pull CD high to disable the IC.	
MID	9	Optional	R8		300 Ω		Voltage sense input for mid point between cells in 2S1P configuration	300-Ω resistor is used to limit the current in the case where the bottom cell is plugged in reversely	
		Optional	C10		0.1 uF		VBUS power good status indicating LED	Noise filtering for the mid voltage sense	
CBSET	10	Required	R9		*Ω		Cell balancing current path	Connect CBSET to the mid point between the two cells with a current limit resistor. The maxiumu cell balancing current can be calculated as ICB_MAX = VCELLREG/R9.	
TS	7	Required	R10		*Ω		Resistor network to set window for thermistor temperature-based battery charging profile	$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{T_{T3}} - \frac{1}{T_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{T_{T3}} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{T_{T1}} - 1\right)}$ $RT1 = \frac{\frac{1}{T_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$	
		Required	R11		*Ω				
PSEL	24						Power source selection pin	HIGH = 500mA; LOW=3A	
SW	17, 18	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	4, 19, 20						Ground return		
PwrPad	-						IC Thermal dissipation pad	http://www.ti.com/lit/an/snva183b/snva183b.pdf	Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow EVM design.