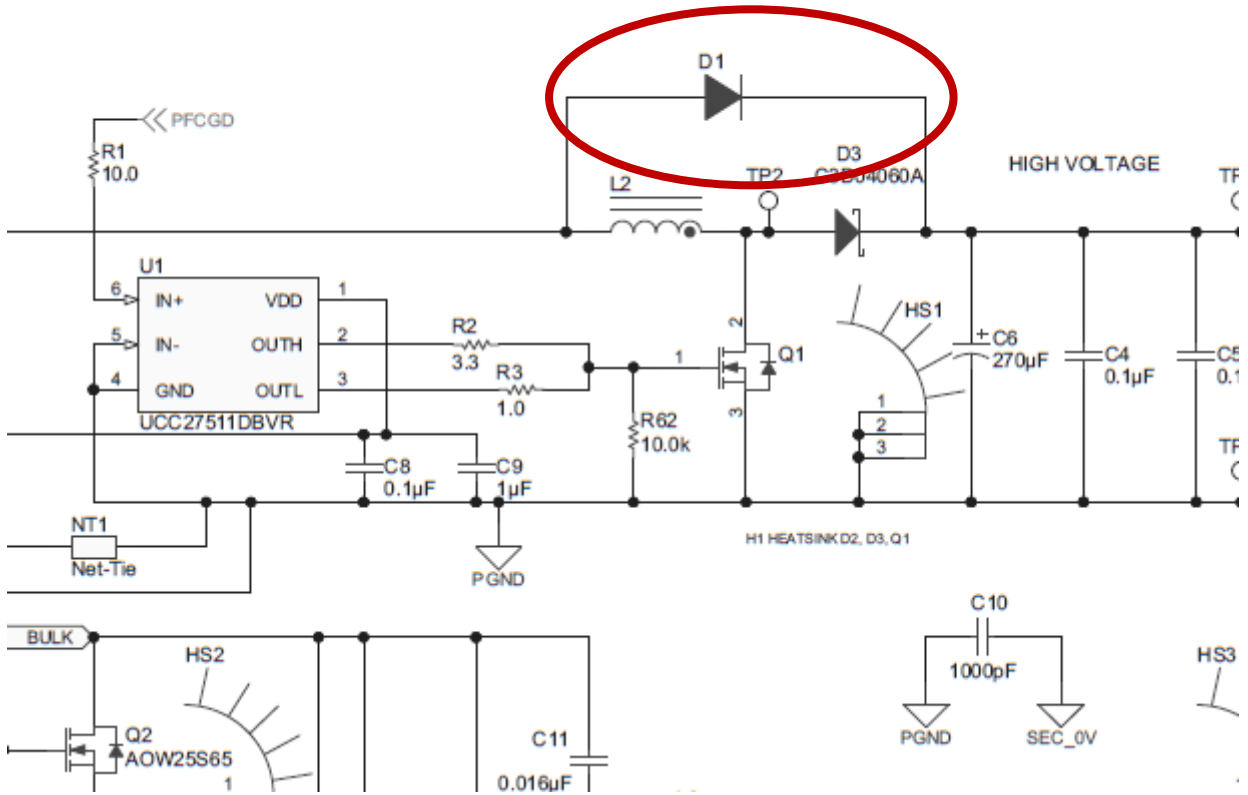
UCC29950: START UP PLAN AND FEEDBACK WITH DIFFERENT VALUES Rtop & Rbttm



Adding D1 implies Vbulk side expects to see initial instantaneous voltage from AC line to start the controller

UCC29950: APPLICATION FOR 325V OUTPUT FROM “BUCKBOOST” : SEPIC POWER STAGE

5.1.11 VBULK

The VBULK pin is used for PFC output-voltage sensing. Connect the sensing resistors to this pin. The upper resistor in the potential divider must be 30 MΩ and the lower resistor must be 73.3 kΩ. The high impedance reduces the static power dissipation.

Is it not enough to get Vbulk regulation value from any output?

$V_{BULK(reg)}$	V_{BULK} regulation set-point		0.907	0.940	0.973	V
$V_{BULK(llc\_start)}$	LLC operation start threshold		0.70	0.73	0.77	V
$V_{BULK(llc\_stop)}$	LLC operation stop threshold		0.45	0.49	0.53	V

7.3.2 Sense Network Fault Detection

Is this true or is this a bit confusing? Besides, D1 in the App ckt defeats it and will cause uncontrolled Inrush current

In a boost converter, there is a direct conduction path from AC line to the bulk capacitor which ensures that it will be charged to peak of line even if the PFC stage controller is inactive. At start-up the UCC29950 measures AC line voltage and the voltage on the PFC bulk energy storage capacitor. If the UCC29950 measures V_{BLK} to be lower than V_{AC} it enters a latched fault condition. This feature prevents the PFC stage from running if the upper resistor in the voltage sensing network has gone open circuit. If the lower resistor has gone open circuit, then the UCC29950 detects this as an over-voltage event on the output and PFC switching will not start.

Is this true or is this a bit confusing?Can UCC29950 be used in our topology of SEPIC buckboost with Vbulk=325v?

7.3.1 Sense Networks

The UCC29950 uses fixed scaling factors to measure the signals at its pins. The circuit position of the voltage sensing resistors is shown in Figure 9. The current sensing resistors are shown in Figure 13.

The resistors in the V_{BLK} sensing network, R_{TOP} and R_{BOT} in Figure 9 have been chosen to minimize the power dissipation and ensure correct operation over the expected tolerance bands. The impedance in this network may be reduced by choosing lower value resistors provided that the potential division ratio is unchanged or kept within the limits given below.

The nominal ratio is 30 MΩ/73.33 kΩ = 409.28. This has been chosen to give a nominal V_{BULK} regulation setpoint of 385 V. This voltage is the ideal operating point for the PFC. It prevents direct conduction into the bulk capacitor at high line and prevents false OVP tripping due to load transients - especially under high load conditions where the voltage ripple on the bulk capacitor is maximum. It is possible to change the nominal setpoint within the limits below.

If the ratio is increased above the nominal value then there is a risk of triggering a sense network fault condition at startup - as described in the next section. The maximum ratio is not an absolutely fixed value but is likely to be about 425 with a corresponding V_{BULK} regulation setpoint of 400 V. The minimum ratio is governed by the desire to avoid direct conduction into the bulk capacitor when operating at high line. V_{BULK} must be greater than 374 V to avoid this condition on a 264 VRMS line. The corresponding minimum ratio is about 395.

WHY these limits in a general use controller such as UCC29950