PSR and SSR Flyback Aux Winding OVP and UVLO Fault Sensing Design tips and Troubleshooting

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Abstract:

There are many flyback controllers on the market that use the aux winding voltage to sense input voltage, output voltage for fault detection. In discontinues current mode DCM valley switched flyback converters the aux winding is also used to detect when the flyback transformer is de-energized and where to valley switch. However, if your aux winding voltage is quite noisy it could cause input under voltage lockout (UVLO) or output over voltage protection (OVP) to falsely trigger causing your design to shut down unexpectedly and not power up. TI primary side regulated (PSR) DCM flyback controllers that use this kind of aux winding sensing for OVP and UVLO are the UCC28700/1/2/3/4, UCC28710/1/2/3, UCC28910/1. The UCC28740/2 secondary side regulated (SSR) controllers also use aux winding voltage fault sensing for fault detection as well. These controllers all use FM/AM/FM modulation to reduce switching losses and audible noise. The purpose of this application note is to give design guidance to resolve and avoid false OVP and UVLO faults caused by noise on the aux winding.

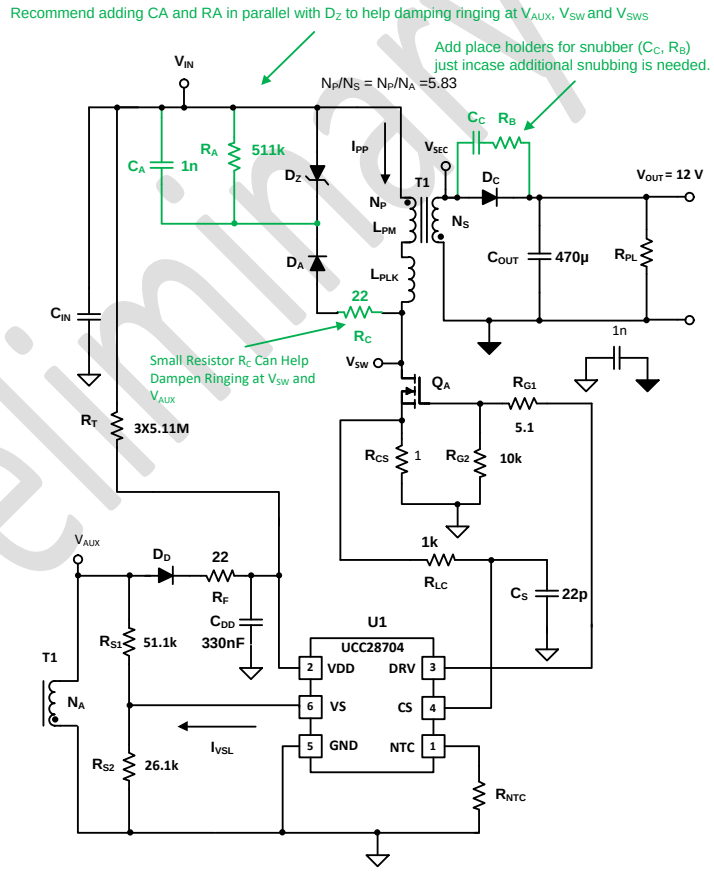


Figure 1, DCM Flyback Converter Using Aux Winding Sensing to Detect Input UVLO and OVP.

Brief Review of DCM FM/AM/FM Flyback Control Law (Figure 2):

The DCM controllers presented in this application note use Frequency Modulation (FM) and Peak Current (AM) Modulation to control the output voltage. At maximum load the flyback converter will be working close to quasi resonant (QR) operation a maximum switching frequency ($f_{sw(max)}$)(Region 1). As the load decreases the converter will go from operating at $f_{sw(max)}$ down to 25 kHz switching frequency approaching region 3 to control the output. Decreasing the switching frequency to control the output voltage will also reduce the flyback converters switching losses as the load decreases. As the load continues to decrease and the converter enters region 3. In region 3, the AM modulation region, the converter operates at a fixed switching frequency and modulates the peak current from its maximum value ($I_{PP(max)}$)down to one forth its peak value ($I_{PP(max)}$ /4). This is done to reduce energy stored in the transformers magnetizing inductance before is enters the lower FM regions 1 and 2. In regions 1 and 2 the converter will control the output by using frequency modulation to control the output voltage while maintain the peak primary current to one 4th its maximum $I_{PP(max)}$ /4.

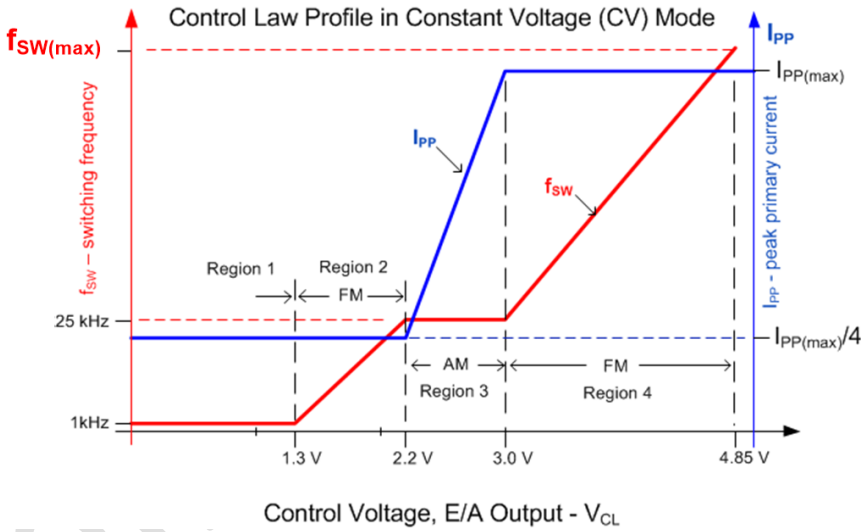


Figure 2, Control Law UCC28704 similar to UCC28742

Input (V_{IN}) and Output (V_{OUT}) Voltage Sensing for UVLO and OVP Fault Protection:

When the flyback converter is energizing the transformer (T1) during t_{on} the input voltage (V_{IN}) can be sensed through T1's primary to auxiliary winding turn's ratio (N_P/N_A) and the voltage measured across the Aux winding (V_{AUX}). Please refer to figure 1, 3 and equation 1 for details.

$$V_{IN} \approx \left| V_{AUX} \times \frac{N_P}{N_A} \right| \quad (1)$$

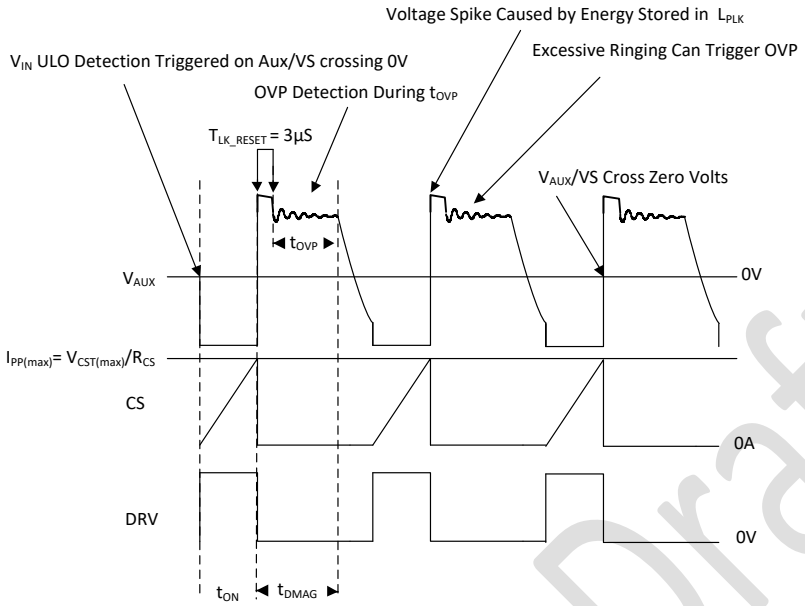


Figure 3, Aux/VS, CS and DRV Signals at Max Load Minimum Line Voltage

During time t_{on} T1's primary magnetizing inductance (L_{PM}) is being energized; as well as, T1's primary leakage inductance (L_{LK}). After the transformer is energized during t_{ON} the flyback controller will drive the gate of Q1 low through the DRV pin of the controller turning off Q1. Energy that was stored in L_{PM} of T1 will be delivered to the secondary during time t_{DMAG}. During time T_{LK_RESET} the energy stored in L_{PLK} will be discharged and clamp through the RCD clamp (R_A, R_C, C_A, D_A), (FIG. 1). The switch node is coupled through T1's Np/Na turns ratio and will put a voltage spike on the aux winding (V_{AUX}). The flyback converters output voltage (V_{OUT}) can be sensed for OVP detection after T_{LK_RESET} and the end of t_{DMAG}. Please refer to figure 3 and equation 2 for details.

$$V_{OUT} \approx \left| V_{AUX} \times \frac{N_S}{N_A} \right| (2)$$

To prevent false firing of the OVP shut down, the flyback controllers presented in this paper have V_{AUX} leakage spike blanking (T_{LK_RESET}) and will not monitor V_{OUT} for OVP during this time. This time will vary with the flyback converter's primary peak current (I_{PP}). For example if you were using the UCC28704 and were controlling the maximum current T_{LK_RESET} would not sense the output voltage at the begging of t_{DMAG} for 3 µs (Figure 3). When the UCC28704 is operating in the AM range T_{LK_RESET} will decrease with I_{PP}. When I_{PP} is controlled down to its minimum value $I_{PP(min)}$, T_{LK_RESET} will be decreased to 750 ns (Figure 4.) Please note this blanking time will vary based on the flyback controller as well. It is recommended that you should read the specific flyback controller's data sheet that you are using in your design for details on T_{LK_RESET} values based on I_{PP}.

When operating in the AM range when I_{PP} is decreased T_{LK_RESET} blanking time also decreases as well. Please check the data sheet of the part you are using, because T_{LK_RESET} changes are different with different flyback controllers.

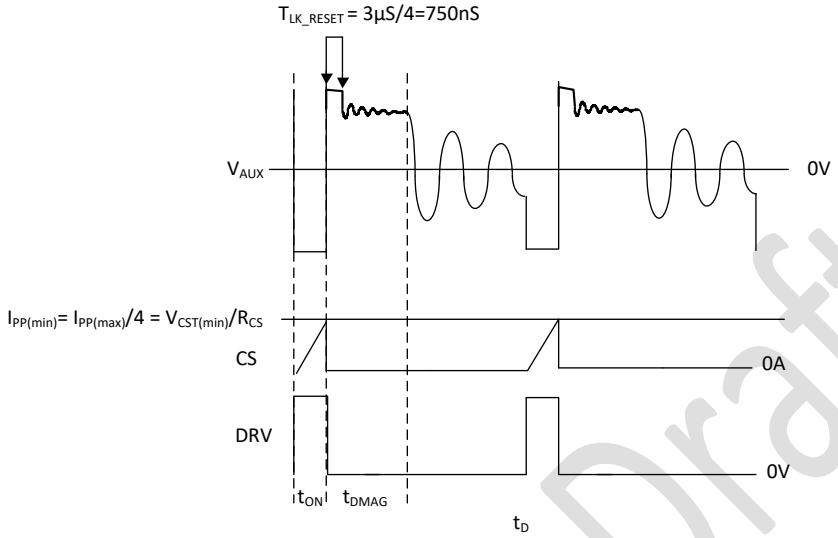


Figure 4, Aux/VS, CS and DRV at Max Load Minimum Line Voltage

Input Under Voltage Lockout (UVLO) Protection:

The VS pin of these flyback controllers have and internal clamp on the VS pin that clamps the VS pin to roughly ground (GND) to while Q1 is on (t_{on}), (Fig. 3 and 4). During this this time the current coming out of the VS pin (I_{VSL}) in combination with RS1 and the Np/Na turns ratio will be used to program and determine what the input voltage level of the flyback converter will start at ($V_{IN(run)}$) and what input voltage the converter will stop switching at ($V_{IN(stop)}$). Please note the value $I_{VSL(run)}$ start and $I_{VSL(stop)}$ stop thresholds will vary based on the flyback controller that is used in the design, please refer to the flyback controller's data sheet for the correct values.

The design presented in Figure 1 will start converter will not start switching until V_{IN} is greater than 67 V and will stop switching when V_{IN} drops below 23.8 V. Please refer to equations 3 through 6 for details.

$$I_{VSL(run)} = 225\mu A \quad (3),\ \text{VS line sensed run current (3)}$$

$$V_{IN(run)} \geq I_{VSL(run)} \times R_{S1} \times \frac{N_P}{N_A} = 225\mu A \times 51.1k\Omega \times 5.83 = 67V,\ V_{IN}\ \text{startup threshold (4)}$$

$$I_{VSL(stop)} = 80\mu A \quad (5),\ \text{VS Line sense stopped current (5)}$$

$$V_{IN(stop)} < I_{VSL(stop)} \times R_{S1} \times \frac{N_P}{N_A} = 80\mu A \times 51.1k\Omega \times 5.83 = 23.8V\ (6)$$

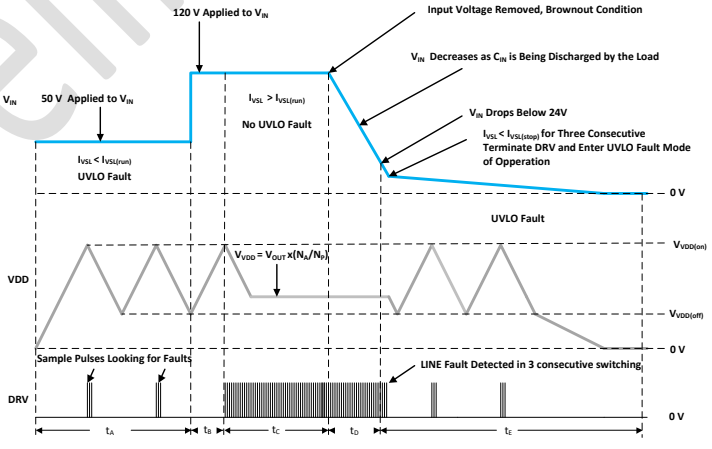
When power is first applied the VDD capacitor (C_{DD}) will trick charge through R_T of figure 1. Please note that some flyback controllers trickle charge the C_{DD} capacitor with an internal JFET startup circuit. The capacitor will continue to trickle charge until the flyback controllers turn on threshold is reached ($V_{VDD(on)}$) at this point it will deliver 3 gate drivers pulse to sample the V_{IN} and V_{OUT} at the controllers

maximum switching frequency ($f_{SW(max)}$) to sample the input and output voltage. The UCC28704 will control the primary current to $I_{PP(max)}$ /4. At this point t_{LK_RESET} will be at it's minimum. If the converter detects a UVLO and/or a OVP fault during this time for three consecutive switching cycles the gate driver will stop switching and the I_{DD} current will discharge C_{DD} to the flyback controllers turnoff threshold ($V_{VDD(off)}$). After $V_{VDD(off)}$ is reached the C_{DD} will be charged up through R_T to $V_{VDD(on)}$ and the flyback controller will sample V_{OUT} and V_{IN} again.

$$V_{VDD(on)} = 21\ V \quad (7)$$

$$V_{VDD(off)} = 8\ V \quad (8)$$

Figure 5, shows an example of how the input fault protection would work with different input voltages. At the beginning of time interval t_A 50 V is applied at V_{IN} the C_{DD} capacitor will be trickle charged up to $V_{VDD(on)}$. The flyback controller will then sample the input through Np/Na turns ratio and will detect an input UVLO fault and stop switching and enter fault mode operation during this time interval. At the beginning of time interval t_B the input voltage is increase to 120 V, however, the flyback controller is still not switching, it has to wait until C_{DD} is charge up to $V_{VDD(on)}$ to gives 3 DRV pulses to sample the input voltage. At the beginning of time internal t_C the flyback controller gives 3 DRV pulses to sample the input voltage, at this point the flyback controller has determined that the UVLO condition no longer remains and the gate driver continues to switch. The C_{DD} capacitor will discharge down to the reflected output voltage determined by the N_A/N_S turns ratio, at this point the flyback controller will be powered by the auxiliary winding (N_A) of T1. At the beginning of time interval t_D the input voltage was removed from V_{IN} simulating a brown out condition. The input bulk capacitor C_{IN} will discharge based on the load on the flyback output. At the beginning of time interval t_E capacitor C_{IN} will have discharged to a point where the input voltage will cause a UVLO fault. After the UVLO fault has been detected in three consecutive switching cycles the flyback controller will terminate the DRV pulses and will renter UVLO fault mode for the rest of time interval. The flyback controller will remain operating in this mode until an input voltage is applied to V_{IN} that causes the I_{VLS} current to be greater than $I_{VSL(run)}$.



While Gate Driver (DRV) is Switching Flyback Converter is Sampling for OVP, LINE and OCP FAULTS

- If a fault is detected for three consecutive switching cycles DRV stops switching
  1. C_{VDD} is discharge until the voltage at VDD reaches VDD(off)
  2. C_{VDD} is trickle charged by R_T or an internal trickle charge startup circuit until the voltage at VDD reaches $V_{VDD(on)}$ reaches

Figure 5, Example of UVLO Fault Detection

Output Over Voltage (OVP) Protection:

The flyback controllers' presented in this paper will sense the output voltage on V_{AUX} through a resistor divider formed by R_{S1} and R_{S2} and flyback controllers sense pin (VS). If the VS pin exceeds the V_{OVP} threshold for three consecutive switching cycles it will determine that an OVP event has occurred and gate driver switching will stop.

$$V_{OVP} = 4.6\,V \quad (9)$$

$$V_{OUT} \geq \frac{V_{OVP}(R_{S1}+R_{S2})}{R_{S2}} \times \frac{N_S}{N_A} \quad (10)$$

The schematic in figure 1 represents a flyback converter that was designed to step down an input voltage (V_{IN}) of 75V to 390V DC to regulated 12 V, 10W output. The N_S/N_A turns ratio was selected/designed to be one. So in this example the flyback converter would shut down if the V_{OUT} for three consecutive switching cycles was greater than 13.6V, equation 11.

$$V_{OUT} \geq \frac{4.6V(26.1k\Omega+51.1k\Omega)}{26.1k\Omega} \times 1 = 13.6\,V \quad (11)$$

If an OVP fault is detected DRV switching will stop and the CDD capacitor will be discharged down to $V_{VDD(off)}$ and the CDD capacitor will be trickle charge through R_T up when V_{CDD} reaches $V_{VDD(on)}$ the controller will then give three DRV pulses at $f_{SW(max)}$ controlling the primary current to $I_{PP(max)}$ /4 and t_{LK_RESET} blanking is set to its minimum of 750 ns. Please remember that VS will detect an OVP from the end of T_{LK_RESET} to the end of t_{DMAG}. Please refer to figure 3 and 4 for details. The C_{DD} and DRV behavior during an OVP fault behaves in similar to UVLO fault presented in figure 5.

$$V_{OUT} \geq \frac{4.6V(26.1k\Omega+51.1k\Omega)}{26.1k\Omega} \times 1 = 13.6\,V \quad (11)$$

Not Recognizing a UVLO or OVP Fault:

A lot of first time designers using aux OVP and UVLO detection have reported that they can't get there designs to startup. Either they have no gate drive pules or VDD looks like a saw tooth presented in figure 6. They just don't know the flyback controller is protecting against a fault.

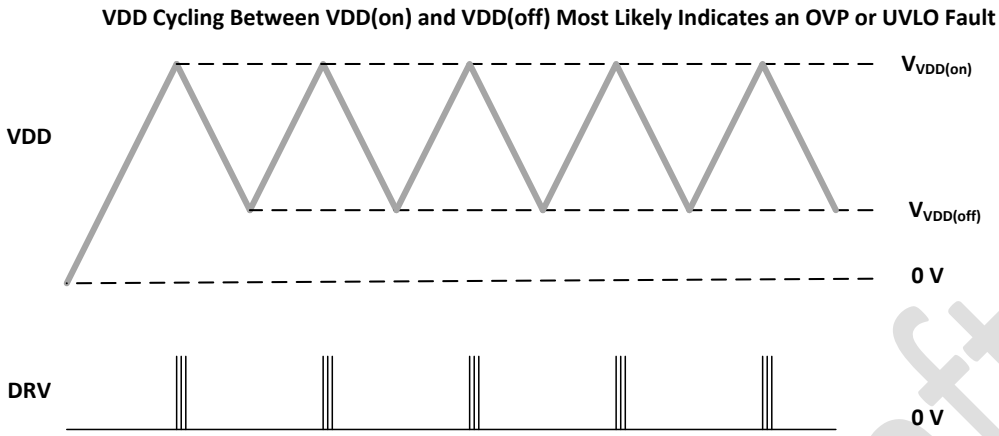


Figure 6, VDD Cycling During a Fault

Separate Bias Supply Startup Issue and Resolution:

When trouble shooting engineers sometimes apply and external bias supply to the VDD pin of the flyback controller and bring up the input voltage and get no DRV pulses. What the issue here is when VDD was brought above the $V_{VDD(on)}$ threshold the flyback controller gave three DRV pules to sample for faults. Since there was no voltage at V_{IN} a UVLO fault was detected and DRV stopped delivering gate drive pules and the separate bias supply prevented the flyback controller from resetting the fault and further sampling. Remember to reset the fault VDD needs to cycle between $V_{VDD(off)}$ and $V_{VVD(on)}$.

To resolve this issue is simple. Apply the input voltage to V_{IN} that is greater than would trip a UVLO fault. Then bring the bias voltage to VDD above $V_{VDD(on)}$. The other option is adjust the bias voltage at VDD below $V_{VDD(off)}$ and then above $V_{VDD(on)}$ to reset and clear the UVLO fault.

Not Having a Clean Aux Winding Signal:

The waveform in figure 7 is a simulation of a flyback converters switch node (V_{SW}), the aux winding voltage (V_{AUX}), and the flyback current sense signal (V_{CS}) of a flyback converter that uses a TVS clamp and no provisions for dampening aux winding ringing. This simulation was based on the flyback converter presented in figure 1 without the circuitry that was highlighted in green.

The flyback converter was designed to trigger OVP when V_{OUT} and V_{AUX} were greater than 13.6V. This flyback converter did not have any previsions for dampening the switch node (V_{SW}) ringing cause by parasitic inductance and capacitance at the switch node. The noise at V_{SW} is couple through the auxiliary to primary turns ratio (N_A/N_P) and will falsely trip OVP fault protection.

The flyback controller will sample for an OVP (t_{OVP}) after T_{LK_RESET} has timed out to the end of the transformer demagnetizing time (t_{DMAG}). From the waveform in figure 7 it can be observed that the ringing on V_{AUX} is greater than 13.6 V during the over voltage protection sampling time (t_{OVP}). This will cause the design to shut down and not regulate the output voltage correctly

Also the ringing on Vaux in figure 7 is excessive it rings down below ground during t_{LK_RESET}. This action has been known to trigger a UVLO fault as well and shut down the converter. This is because when the VS pin crosses ground it activates input and UVLO detection.

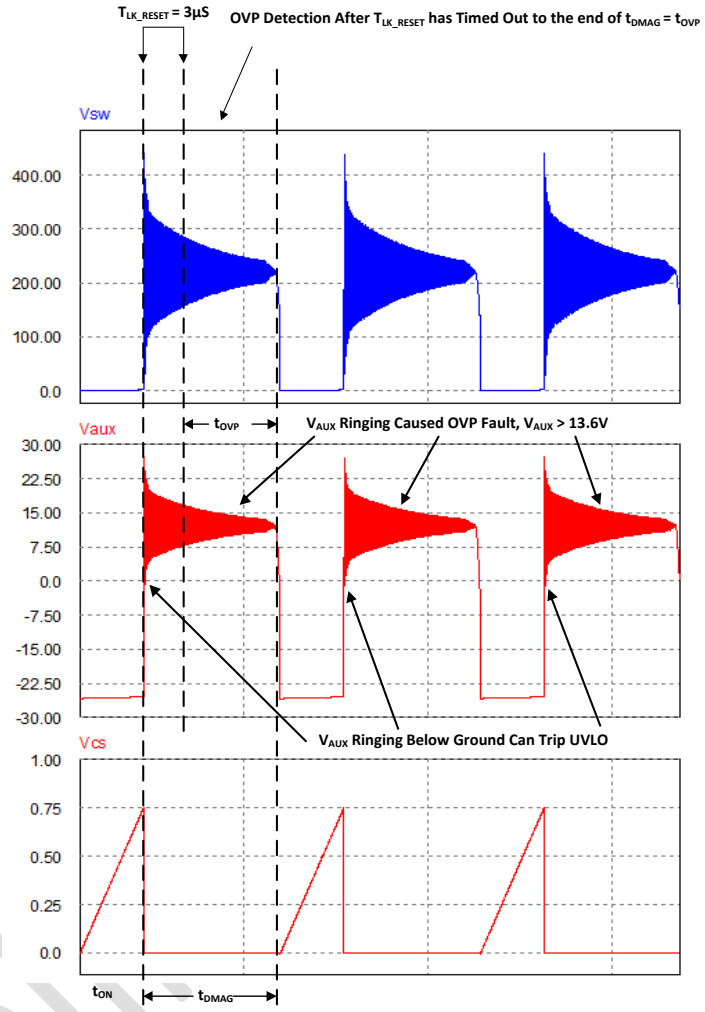


Figure 7, Noisy V_{AUX} Falsely Trigger OVP and/or UVLO Fault Protection

Removing Aux Winding Ringing to Resolve False Triggering of OVP and UVLO Faults:

1. When selecting and designing your transformer (t1) it is recommended that a transformer being selected have a primary leakage inductance (L_{PLK}) of less than three percent of the primary magnetizing inductance (L_{PM}), (Fig 1). This will help reduce switch node (V_{SW}) ringing and ringing at V_{AUX}.

$$L_{PLK} \leq 0.03 \times L_{PM} \quad (12)$$

2. When constructing the designs layout keep the traces in the power stage; as short as, possible. An inch of printed circuit board (L_{TRACE}) trace adds about 10 nH of inductance per inch.

$$L_{TRACE} \approx \frac{10nH}{IN} = \frac{10nH}{2.54\ CM} \quad (13)$$

3. It is recommended that you use an RCD clamp (R_A, R_C, C_A, D_A) over a TVS clamp (D_A, D_Z), Figure The reason for this is an RCD clamp will provide dampening at the switch node, where TVS will only clamp the voltage when the switch node rings above the clamp voltage and provides very little dampening. Generally we set the R_A and C_A time constant of the clamp to greater than 10 times the maximum switching period, equation 6 and 7. Please note for safety the designer want to use D_Z to clamp V_{SW}.

$$R_A \times C_A \geq \frac{10}{f_{SW(mx)}} = \frac{10}{100kHz} = 100us \quad (6)$$

$$R_A \times C_A = 511\ k\Omega \times 1nF = 511us \quad (7)$$

4. If you have excessive ringing across the secondary V_{SEC} winding it will couple into V_{AUX} through the auxiliary to primary turns ratio, figure 8. This ringing will most likely trigger and OVP and or load regulation issues and will require adding an RC snubber, (R_B, C_C).

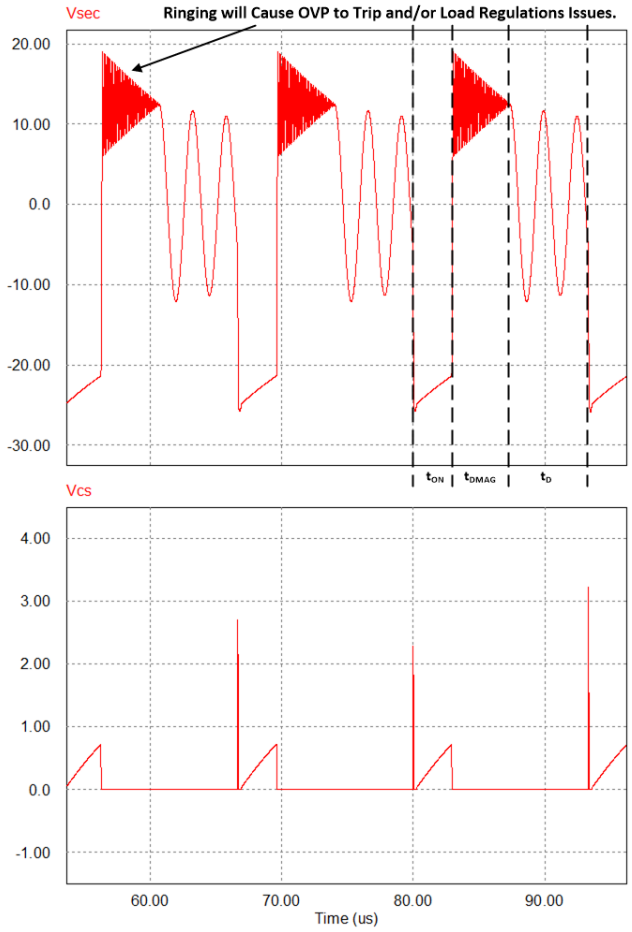


Figure 8, Flyback Secondary Voltage with Excessive ringing.

Before setting up the snubber circuitry (R_B and C_C) we are going to evaluate the waveforms in figure 8 and the simplified flyback converter presented in figure 9. The major contributors to high frequency ringing are the interaction or resonant ringing between parasitic inductances (L_{PRIP}, L_{SECP}) and parasitic capacitance (L_{PRIP}, L_{SECP}).

During interval t_{on} flyback transformer T1 is being energized. During time interval to t_{DM} switch Q1 is off energy stored in the transformer is delivered to the secondary. The high frequency ring observed during this period is cause by the ringing energy between L_{PRIP}, L_{SECP}, C_{SW1} and C_{SW2}. During time internal t_D the energy stored in T1 has already been delivered to the secondary. The low frequency ring during this period is between is cause by the interaction of T1's secondary side magnetizing inductance (L_{SM}) and the secondary's switch node parasitic capacitance (C_{SW2}):

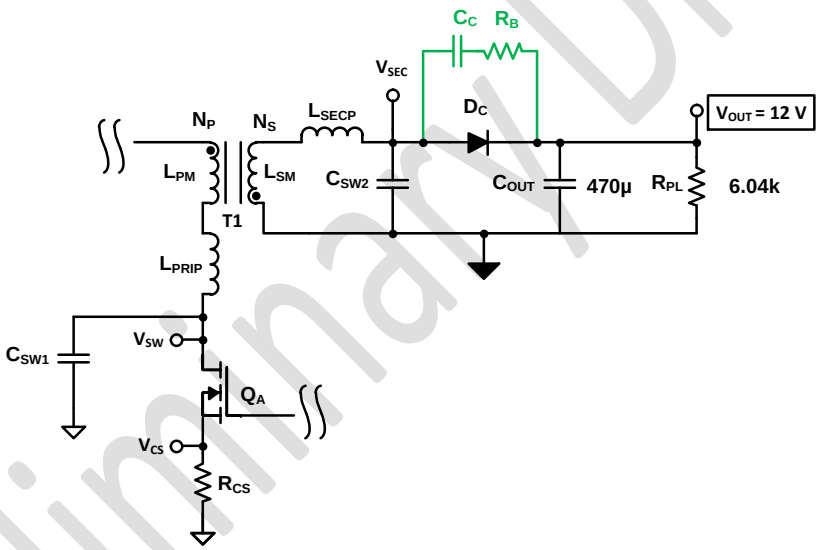


Figure 9, Simplified Flyback Schematic with Parasitic.

To setup the RC snubber you will need to know what the primary magnetizing inductance (L_{PM}) is the primary turns (N_P) and (N_S), to calculate T1's L_{SM}. For example if we setting up a snubber for a design that a L_{PM} is 680 µH and primary to secondary turns ratio (N_P/N_A) of 5.8 the L_{SM} of the transformer would be 20 µH. Please refer to equations 8 and 9 for details.

$$\frac{N_P}{N_A} = 5.8 \text{ (8)}$$

$$L_{SM} = \frac{L_{PM}}{\left(\frac{N_P}{N_S}\right)^2} = \frac{680\mu H}{5.8^2} \approx 20\mu H \text{ (9)}$$

The next step is to measure the frequency (f_{r1}) or the ringing during time interval t_D to calculate the secondary switch node capacitance (C_{SW2}). In this example f_{r1} was measured at 645 kHz, figure 10.

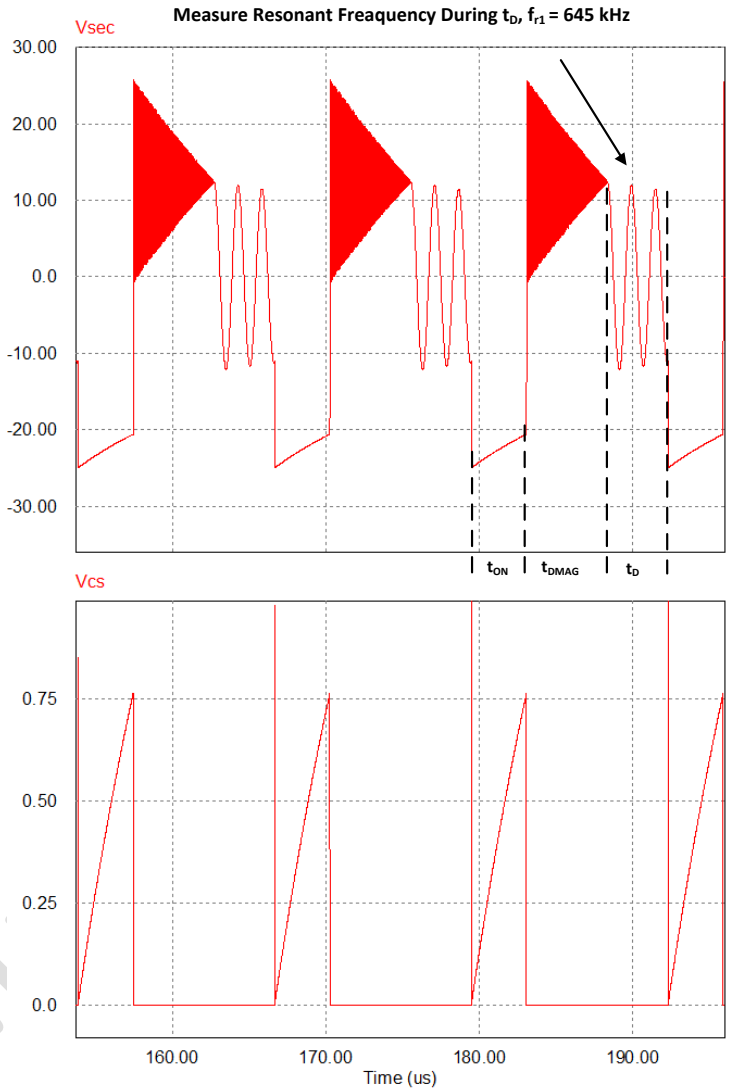


Figure 10, Measuring Low Frequency Ringing to Calculate C_{SW2}

$f_{r1} = 645\ kHz$ (10), Measure low frequency ringing during interval t_D

Based on calculated L_{SM} and measured $f_{r1\ and}$ the secondary switch node parasitic capacitance (C_{SW2}) can be calculated.

$$C_{SW2} = \frac{1}{(2\times\pi\times f_{r1})^2\times L_{SM}} = \frac{1}{(2\times\pi\times 645kHz)^2\times 20\mu H} \approx 3nH \text{ (11)}$$

The next step is to measure the ringing frequency during time interval t_{DMAG} (f_{r2}). This resonant frequency is caused by the interaction of C_{SW2} and L_{SECP}. Based on f_{r2} and C_{SW2} L_{SECP} can be calculated, equation 13. With a measured f_{r2} of 14 Mhz a C_{SW2} of 3nF the calculated L_{SECP} would be roughly 43 nH.

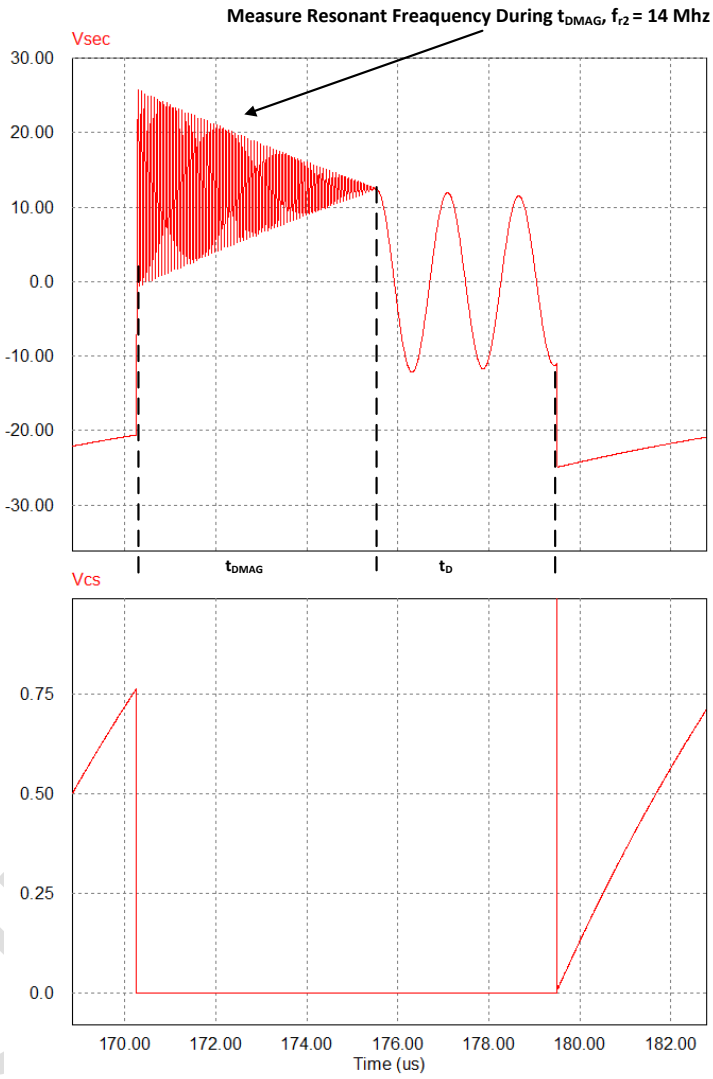


Figure 11, Measure high frequency ringing during time interval t_{DMAG}.

$f_{r2} = 14\ MHz\ kHz$ (12), Measure high frequency ringing during interval t_{DMAG}

$$L_{SECP} = \frac{1}{(2\times\pi\times f_{r2})^2\times C_{SW2}} = \frac{1}{(2\times\pi\times 14Mhz)^2\times 8nF} \approx 43nH \text{ (13)}$$

Snubbing resistor R_B is chosen to crucially dampen the ringing with use of equation 14. In this example to dampen the ringing resistor R_B was calculated and chosen to be roughly 3.83 ohms.

$$R_B = \frac{1}{Q}\sqrt{\frac{L_{SECP}}{C_{Sw2}}} = \frac{1}{1}\sqrt{\frac{43nH}{3nF}} \approx 3.8ohm \text{ (14)}$$

Choose a standard resistor for value for R_B :

$$R_B = 3.83 \text{ (15)}$$

The snubbing capacitor C_C was chosen based on equation (15), based on the converter maximum nominal switching frequency (f_{sw}) using equation 15. This will allowed the snubber to only be active for 1% of the switching period, keeping snubber losses to a minimum.

$$C_C = \frac{0.01}{f_{SW} \times R_B \times 5} = \frac{0.01}{75kHz \times 3.8ohm \times 5} \approx 7nF \text{(16)}$$

Chose a standard capacitance value for C_C :

$$C_C = 6.8nF \text{ (17)}$$

The snubber components that were selected for R_B and R_C were applied to the circuit presented in figure 1 and figure 9. The result was the secondary winding was critically damped please refer to figure 12 for details.

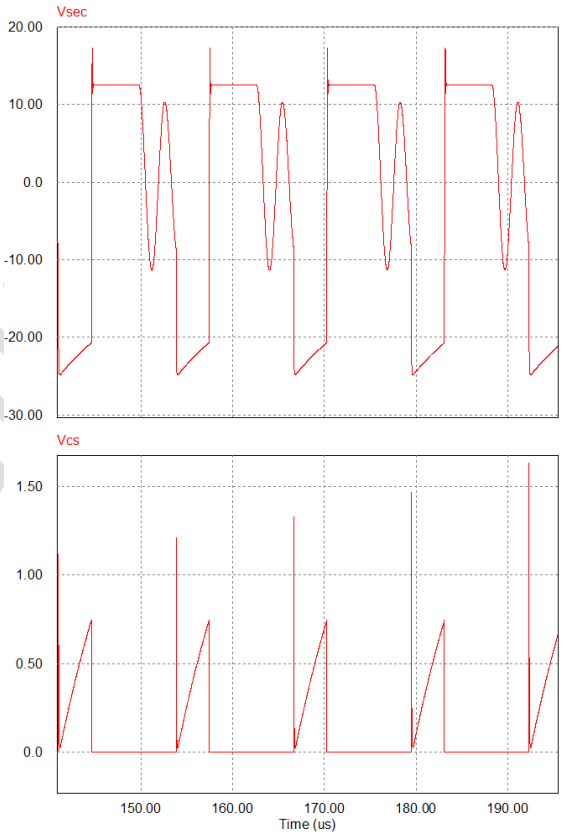


Figure 12, Snubber, RB 3.83 ohms, CC = 6.8nF, PRB =220 mW

Noise on CS Pin Tripping Over Current Protection (OCP):

To help protect the FET from damage these flyback controllers have an over current protection (OCP) circuit that trips when the CS pin sense a CS signal that is 2X the nominal peak. In the case of the UCC28704 this OCP trip point is 1.5V.

To help prevent these controllers from falsely tripping OVP the devices have current sense leading edge blanking to block out the leading edge current sense spikes cause by driving the gate of the FET and the FET's gate to source capacitance. The UCC28704 at the begging of t_{ON} has a leading edge blanking circuit that will blank out the CS signal for a blanking time (T_{CSLEB}) of 255 ns.

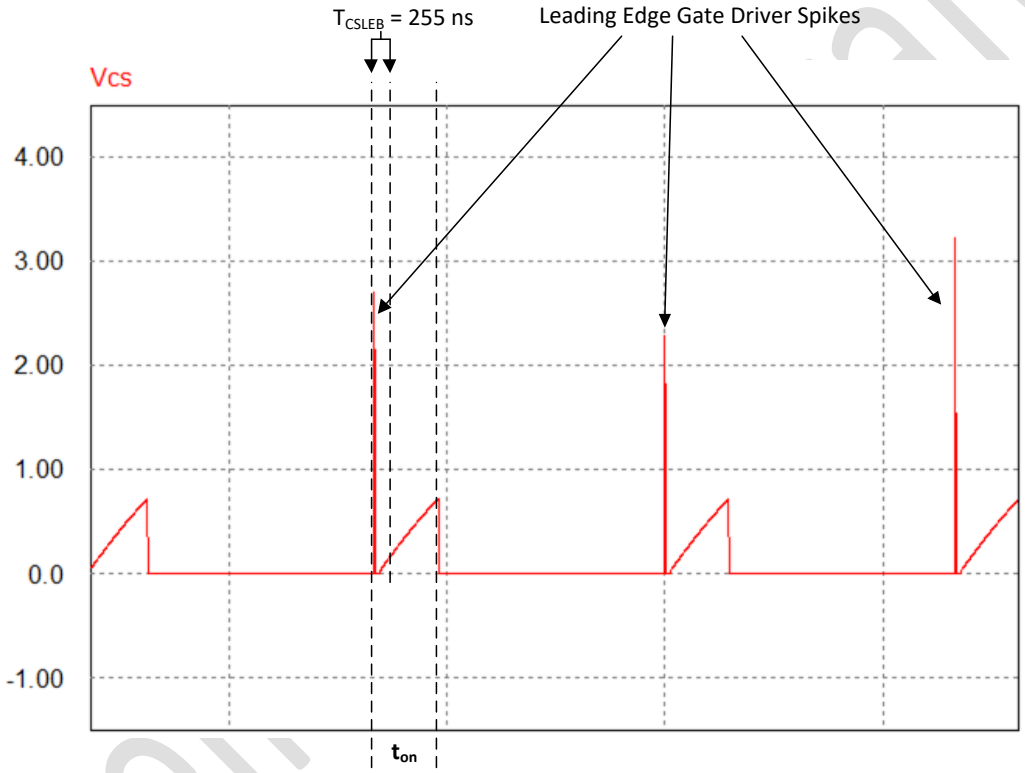


Figure 13, CS Leading Edge Blanking Helps Prevent False OCP shutdown

On occasion I have seen these flyback designs shut down due to noise on the CS pin. This is not related to OVP or input UVLO sensing. This occurs buy noise being coupled into the circuit through parasitic capacitance and/or poor layout. The problem occurs if these noise spikes are outside the T_{CSLEB} blanking window. Please refer to figure

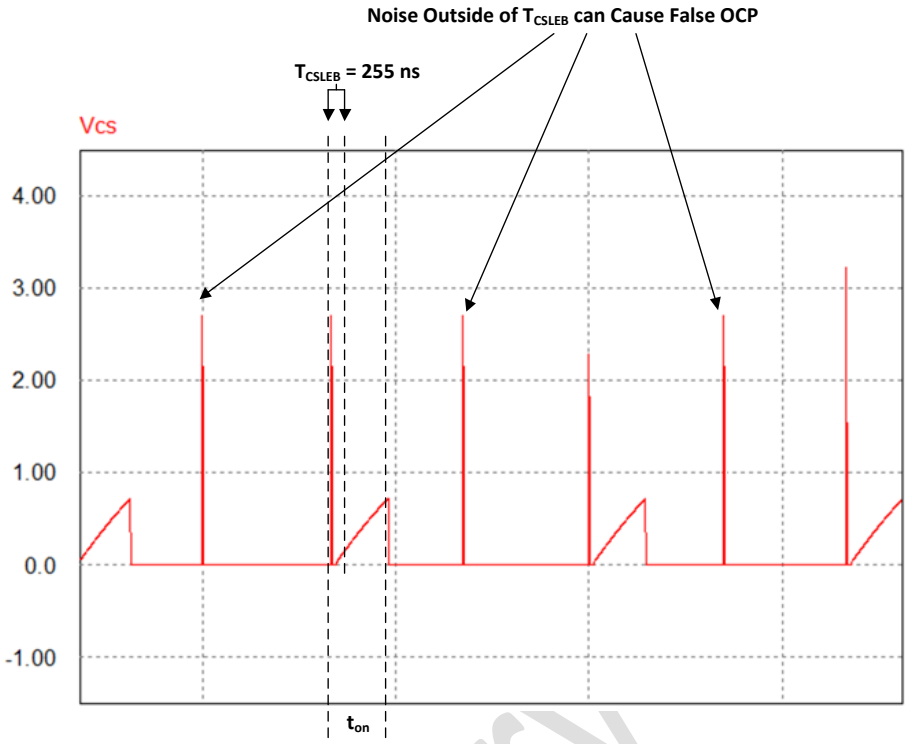


Figure 14, Noise Spikes Outside the TCSLEB Window will Cause a False OCP Fault.

To remove this fault you may have to correct your layout if it was done poorly. The data sheet of the flyback controllers has a section on layout that gives guidance and an example to avoid this issue. Another tool you have at your disposal is to add some current sense filtering.

In figure 1, there is current sense filter formed by R_{LC} and C_s. Resistor R_{LC} was selected based on data sheet recommendations. Capacitor C_S can be used to filter out noise spike and is recommend that you select the filter capacitor pole at least 10 time greater than the converter's maximum switching frequency, equation 18, so the current sense signal is not overly filtered.

$$C_S \leq \frac{1}{2\times\pi\times10\times f_{sw(\max)}\times R_{LC}} = \frac{1}{2\times\pi\times10\times75kHz\times1k\Omega} \approx 212pF \quad (18)$$

In the design of figure 1 very little filtering was needed and C_S was selected to be 22 pF.

Summary:

Remember when designing a DCM flyback controller that uses the transformer's aux winding for voltage sensing to sample the input and output voltage for OVP and UVLO. It is critical that the aux winding waveform be as clean as possible with as little ringing on it as possible. Some designers struggle with this ringing caused by parasitic inductances and capacitances that cause false OVP or UVLO faults. As this application note showed to prevent false OVP and UVLO faults, A RCD clamp and/or a snubber across the flyback converter's output rectifier, should be used to dampen the aux winding ringing.

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