# Derivation and Analysis of a Secondary-Side *LLC* Resonant Converter for the High Step-Up Applications

Pengyu Jia, *Member, IEEE*, and Yang Mei, *Member, IEEE*

***Abstract*—An isolated high step-up converter, which is derived from the reverse structure of a regular *LLC* resonant converter, is proposed in this paper. The proposed converter consists of an inverter stage, a secondary-side resonant tank and an active voltage-doubler rectifier. An additional input diode is introduced into the regular push-pull inverter so to make the magnetizing inductance free from being always clamped by the input voltage, and make up new voltage gain features. The leakage inductance, which always shows a significant value when reflected to the secondary side in a high step-up transformer, can be utilized to make up the resonant tank. Under a simple Pulse-Frequency-Modulation control with 0.5 duty-ratios for both the primary-side and secondary-side switches, high step-up function can be easily realized by the converter with good load regulation ability. Meanwhile, synchronous rectification (SR) can be naturally achieved by the secondary-side switches. The additional input diode can be replaced by a MOSFET with an analog SR chip in order to further improve efficiency, without changing the original control scheme. The validity of the study is confirmed by a 500W prototype with 36V~42V input and 380V output. The peak efficiency can reach 96.9%.**

***Index Terms*—High step-up converter, *LLC* resonant converter, Synchronous rectification, Soft switching, DC-DC converter**

## I. Introduction

The shortage of traditional fossil energy leads to the rapid development of the renewable energy technology, such as photovoltaic array and Lithium ion battery. Due to the low terminal voltage of the photovoltaic cell and the Lithium ion cell, series connection with large quantities of cells is normally necessary in order to pump up the output voltage. However, the hot-spot and shadow effects may significantly decrease the output power of the photovoltaic cell series. Meanwhile, the degradation of one cell will also restricted the power of the series. Parallel connection for the cells with low series number is a solution but it leads to the problem that the terminal voltage is still in a low value range. As a result, high step-up converters are focused on in recent years [1-26].

Traditional isolated hard-switching converters are difficult to realize a good efficiency performance under high step-up applications due to the huge switching loss. Besides, the transformer leakage inductance, which always contributes a great proportion in passive power and leads to high voltage spikes, also limits the voltage conversion ratio. To alleviate these problems, many literatures focused on the non-dissipative snubbers [6-8] and active clamping circuits [9-14] in the PWM chopper converters. By this means, the leakage energy can be recycled and the voltage spikes can be absorbed. However, due to the introduction of the extra non-dissipative snubbers or active clamping circuits, the converter usually shows a big component count and a complex structure. Since soft switching can be easily achieved by a resonant converter and the leakage inductance can be utilized to make up the resonant tank, the resonant converters are usually with fewer components than the PWM chopper ones. With a step-up transformer, the high voltage conversion ratio can be easily obtained by the traditional resonant converters or by their derivations [15-18]. However, the majority of the resonant components are still placed on the primary side in most of the traditional resonant converters, such as the resonant capacitor in a Series Resonant Converter (SRC), or an *LLC* converter. As a result, power loss caused by the primary-side components is still a big issue especially when the large primary-side current is present. To alleviate this problem, many bulky resonant capacitors are needed to be connected in parallel in order to decrease the current stress and lower the Equivalent Series Resistance (ESR). Similarly, the wire with larger cross-section area is also necessary in a primary-side inductor in order to reduce the conductive loss.

In a step-up transformer, the leakage inductance reflected to the secondary side is much larger than that reflected to the primary side. Based on the concept of reducing the quantities of the primary-side components and simultaneously utilizing this secondary-side leakage inductance as part of the resonant tank, some literatures proposed varieties of derived converters from an SRC or an *LLC* converter, in order to achieve higher

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efficiency, such as [19-26]. In [19] a quasi-resonant step-up converter is proposed, which can be considered as a derivation with clamp diodes from a backward *LLC* converter. By introducing a symmetrical voltage quadrupler rectifier, the transformer turns ratio is greatly decreased and the voltage stress of the rectifier diode is reduced to half of the output voltage. However, due to the linear relationship between the switching frequency and the voltage gain, the switching frequency range is much larger than a conventional *LLC*, which results in a bulky transformer. Moreover, synchronous rectification (SR) is hard to be realized in the converter because the count of the diode is great. In [20, 21], an extra inductor is introduced at the AC input port of the rectifier stage and the transformer only plays a role to amplify the voltage from the inverter stage. By this means, the additional inductor can operate like the "resonant magnetizing inductor" of a regular *LLC* converter. Therefore, the output can be well regulated with the feature similar to a regular *LLC*, by adjusting the switching frequency for wide voltage range application. Moreover, the rectifier stage of [21] is implemented by active switches, where SR can be realized without detecting zero-crossing point of the resonant current. However, the conducting time of the high-voltage side rectifier switches is fixed equal to half of the resonant period, which should be calculated and programmed into the controller beforehand. However, the resonant parameters can vary with temperature and aging, so there will be some deviation between the preset conducting time and the precise one. Besides, the converter volumes of [20, 21] are both increased by the additional magnetic component when they are compared with a regular *LLC* converter. There are also some converters utilizing the total reverse structure of a regular *LLC* converter without any additional component to realize high step-up function, such as [22-26]. However, since the magnetizing inductor is always clamped by the input voltage, the regular reverse structure of *LLC* is essentially an SRC [25, 27], which has the unsatisfactory voltage regulation ability. The switching frequency range will become very wide when the converter operates into a light-load condition. Therefore, this scheme is always employed as a DC/DC transformer to provide constant voltage gain [22-24]. In order to overcome this shortcoming, [26] proposed a control strategy based on the state-plane diagram of the resonant variables to satisfy the requirement of wide voltage range application. However, this control strategy is complicated because the accurate conducting time for the primary and secondary side switches needs to be preciously calculated with the detection of both input and output voltages. In [28], a bidirectional GaN AC switch is introduced into the transformer secondary side. With the phase-shifted (PS) control for the primary-side switches and the duty-ratio control for the GaN AC switch, the converter can realize either a step-down or a step-up function so as to achieve wide voltage range. However, different control modes need to be selected by the controller according to the voltage range. Moreover, the extra GaN AC switch results in a floating driver ground. With the GaN device, the cost is also increased.

As mentioned above, the leakage inductance reflected to the secondary side is much larger than that reflected to the primary side in a step-up transformer. Hence, it is suitable to make up a secondary-side *LLC* resonant tank by employing the secondary-side resonant capacitor, which is symmetrical to a traditional *LLC* converter. However, if there is no improvement on a reverse structure of a regular *LLC*, it still works as an SRC since the magnetizing inductor is always clamped by the input, which will show the unsatisfactory voltage regulation ability especially in light-load condition. Based on this concept, an improved secondary-side *LLC* resonant converter is proposed in this paper, which is with the following features: 1) There are no other components on the primary side except the active switches and a diode (or a synchronous rectifier), so the power loss caused by the large input current can be controlled in a minor range. 2) Soft-switching can be achieved by all the active switches and the diode. 3) The minimum component count is very low, so the cost is a great advantage. 4) The output switches are always operated under a natural synchronous rectification state. 5) The load variation has little effect on the switching frequency range.

In this paper, the model of the proposed secondary-side *LLC* (*S-LLC*) converter is derived and meanwhile, the voltage gain behavior is given and analyzed in detail. The operation region of the converter is discussed and the design constraints for the parameter are also presented. Detailed comparisons between the proposed converter and other resonant converters are also given.

## II. THE DERIVATION OF THE PROPOSED CONVERTER

In a traditional primary-side *LLC* (*P-LLC*) resonant converter, the resonant tank is set on the primary side, as shown in Fig.1. It is suitable to be applied as a step-down converter rather than a high step-up one. This is mainly due to the following reasons: 1) The voltage gain curves in a *P-LLC* can be significantly impacted by the quality factor. The peak value of the gain curve decreases with the increase of the power level [29]. Hence, the high step-up function is mainly realized by the step-up transformer. This will lead to a high transformer turns ratio, which can result in an obvious leakage inductance. Note that when analyzing the features of the *P-LLC* converter, the voltage across the magnetizing inductance, $v_{\mathrm{Lm}}$, is always considered to be clamped by the output voltage once the rectifier diode conducts. However, with an obvious leakage inductance, this assumption is no longer accurate and the gain features will deviate from the predicted results. Moreover, when a full-wave rectifier stage is adopted on the high-voltage side, the diode voltage stress will be much higher than twice the value of the output voltage due to the leakage inductance [30]. 2) Large primary-side current will lead to many bulky resonant capacitors under a high step-up application, which are connected in parallel in order to realize low current stress and decrease the ESR loss. 3) There still exist some issues when synchronous rectification (SR) is adopted in a *P-LLC* converter with a high voltage output. It should be pointed out that the primary-side inverter can be replaced by a half-bridge or a push-pull inverter, and the output stage can be replaced by a full-wave rectifier or other rectifier forms as shown in Fig.1. To obtain a high efficiency performance or to realize a

bidirectional power flow function, some literatures focused on the full-active-switch scheme, that means all the diodes are replaced by the active switches [23, 24, 31-35]. In this way, the power loss of the rectifier stage can be greatly reduced due to SR. However, the conducting time of the SR switches are not the same with the primary-side switches. It relies on the accurate detection of zero-crossing point of the resonant current. Normally, zero-crossing point can be achieved by a current transformer (CT) or by an analog SR chip which detects the drain-source voltage and autonomously outputs driving pulses [31-33]. In a CT scheme, an extra circuit is required to transfer the current signal to the corresponding driving pulse. Therefore, the layout of this circuit must be carefully designed so as to reduce the stray parameters. Besides, the signal filtering delay and the CT's leakage and magnetizing inductance can significantly limit the bandwidth. With advanced integrated IC technology, the analog SR chip has more advantages in high switching frequency and high power density when compared with the CT scheme. During a practical design process, it is easy to be implemented on the full-wave rectifier structure by the analog SR chip since the source of the two SR active switches are connected together to the same power ground. Therefore, the auxiliary power supply can be achieved by a common power source or by the output voltage. However, the voltage stress of the secondary-side switch is larger than twice the value of the output voltage in practical [30]. Obviously, designer can choose a full-bridge or a voltage doubler structure as the output stage, in order to decrease the voltage stress of the rectifier switches. But in this case, more auxiliary power supplies for the analog SR chip are needed. Besides, at the present stage, the maximum drain-source detection voltage rating of the SR analog chip is below 250V [36], which limits the application of the *P-LLC* with synchronous rectifier structure in higher output voltage applications.

Based on the idea of utilizing the reverse power-flow path of

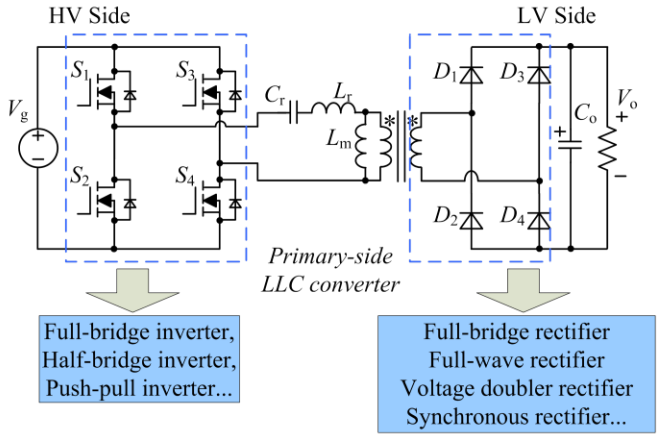


**Fig.1 Primary-side *LLC* (*P-LLC*) resonant converter**

the *P-LLC* in order to realize a high step-up function, a secondary-side *LLC* converter is proposed in this paper, as shown in Fig.2. Compared with the total reverse structure of a regular *P-LLC*, an input diode is introduced to block the power flow back to the power source, which is corresponding to the diode rectifier stage in a *P-LLC* converter. By this means, the magnetizing inductance is not always clamped by the input voltage but has a period of time to participate in the resonant process. The primary-side circuit structure only consists of two active switches and one diode to minimize the cost. Obviously it can be implemented by a full-bridge with a diode, or a half-bridge with a diode, instead. Considering the minimum component number of the converter, here the push-pull circuit structure is adopted as an example.

## III. Operation Principle of the Proposed Converter

The operation of the proposed secondary-side *LLC* (*S-LLC*) resonant converter can be characterized by the relationship of the switching frequency $f_s$ to the series resonant frequency $f_r$, which is defined in (1). Fig.3 illustrates the typical waveforms of an *S-LLC* resonant converter with the switching frequency at, below, or above the series resonant frequency, where $T_s$ denotes the switching period. The switches $S_1$ and $S_2$ alternatively conduct with an approximate 0.5 duty ratio and so do $S_3$ and $S_4$. $S_1$ and $S_4$ operate under the common control pulses while $S_2$ and $S_3$ operate in the same way. The drain-source currents of the switches $S_1$~$S_4$ are denoted by $i_{DS1}$~$i_{DS4}$, respectively. Similarly, their drain-source voltages are denoted by $v_{DS1}$~$v_{DS4}$, respectively. The voltage across the input diode $D_1$ is denoted by $v_{D1}$. From Fig.3 it is apparent that the primary-side switches obtain the ZCS turn-on and the secondary-side switches obtain the ZVS turn-on. However, a ZCS turn-off for the primary-side switches can be only realized when $f_s < f_r$. The ZCS turn-off is necessary for the converter because the reverse-recovery loss of diode $D_1$ will significantly deteriorate efficiency when the hard-switching-off for $S_1$ and $S_2$ is present, because the current decline rates of the diode and the primary-side switches are both the same with each other. Besides, the hard-switching-off of $S_1$ and $S_2$ will result in high voltage spikes between the drain and the source of the primary-side switches, which can cause a voltage breakdown in the switch. From Fig.3 (b) and (c) it is obvious that $i_{Lm}>i_{Lr}$ when $S_1$ and $S_4$ are switched off. Therefore, during the turn-off process, current $i_s$ is a negative value and this instantaneous current will rapidly accumulate charge in the drain-source capacitance of $S_1$, so the voltage spikes arise. Similar situation can be found in $S_2$. Therefore, the first condition that $f_s < f_r$ is recommended for the design.

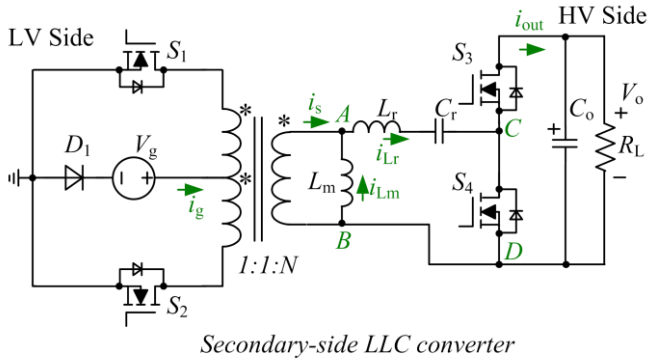


**Fig.2 The proposed secondary-side *LLC* (*S-LLC*) resonant converter**

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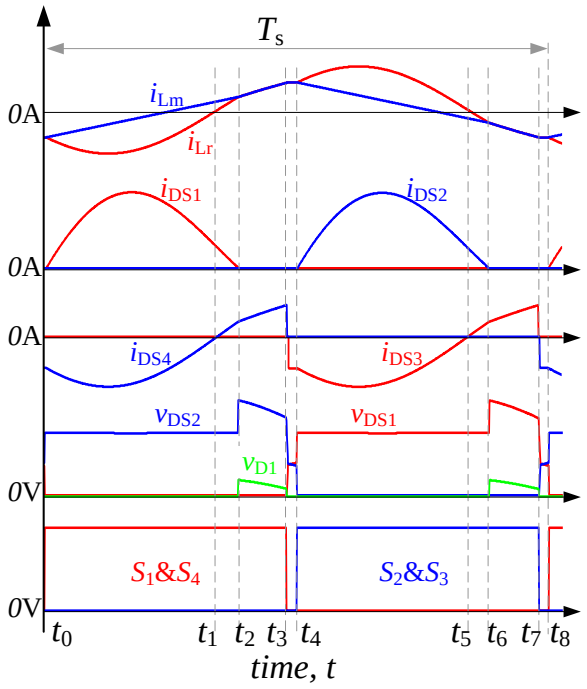
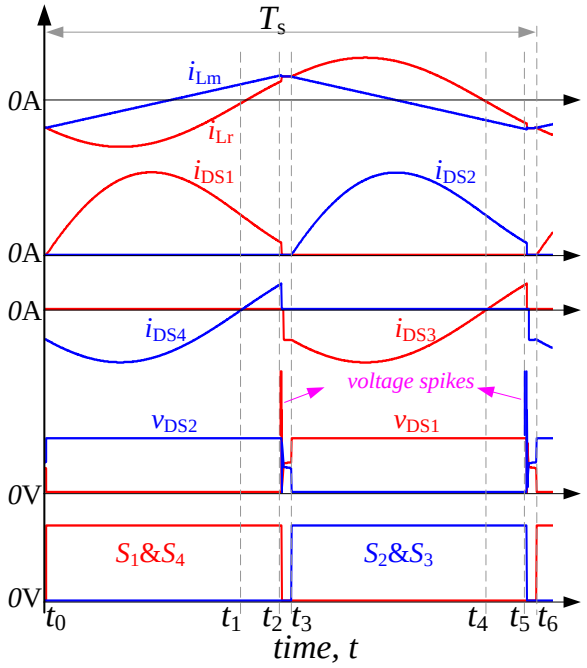
$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

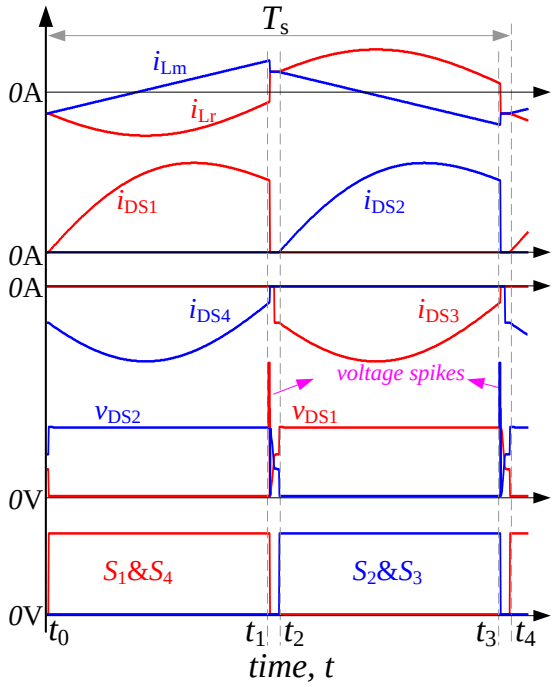
Corresponding to the typical waveforms in Fig.3(a), the converter operation modes are given in Fig.4. The waveforms in one switching period can be divided into eight parts. Due to the symmetrical operation process, only the first four modes are discussed here for simplicity. The reference positive directions are defined in Fig.2. The current directions of the converter during different stages are marked by red arrows.




(a) $f_s$<$f_r$




(b) $f_s$=$f_r$




(c) $f_s$>$f_r$

**Fig.3 Typical waveforms of the *S-LLC* converter**

Mode I ($t_0$<$t$<$t_1$): $S_1$ and $S_4$ are switched on at $t_0$. The current $i_{DS1}$ slowly increases from zero so $S_1$ realize a ZCS turn-on. Therefore, the voltage of inductor $L_m$, that is $v_{ab}$, is clamped equal to $NV_g$. As a result, the resonant frequency depends on $L_r$ and $C_r$, which is equal to $f_r$ as defined in (1). The current $i_{DS4}$ flows from the source to the drain of $S_4$ and a natural SR is achieved. A ZVS turn-on can be obtained by $S_4$ at $t_0$ instant. This stage is given in Fig.4(a).

Mode II ($t_1$<$t$<$t_2$): At instant $t_1$, the direction of $i_{Lr}$ changes from negative to positive and so does $i_{DS4}$. The current $i_{DS1}$ keeps a positive value and gradually decreases. At instant $t_2$, $i_{DS1}$ reaches zero, hence, the primary side and the secondary side are decoupled from each other at that moment. This stage is given in Fig.4(b).

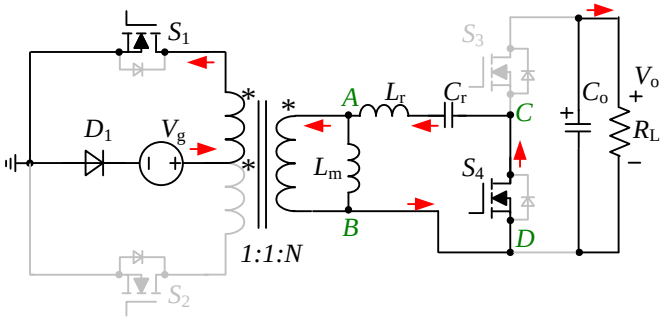
Mode III ($t_2$<$t$<$t_3$): During this stage, there is no power exchange between the primary side and the secondary side. The inductor voltage $v_{ab}$ is no longer clamped. Therefore, the resonance is dependent on $L_m$, $L_r$ and $C_r$. The resonant frequency is given in (2). This stage is given in Fig.4(c).

$$f_{rm} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2}$$

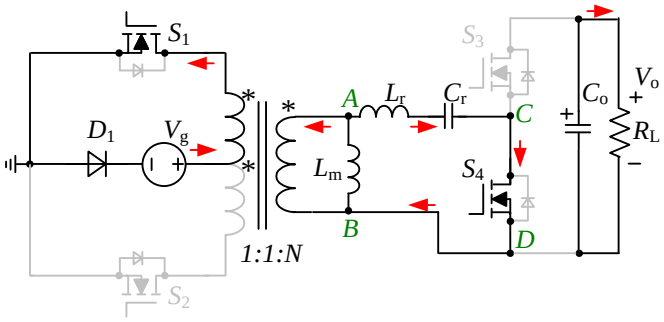
Mode IV ($t_3$<$t$<$t_4$): The duration from $t_3$ to $t_4$ is the dead-time, denoted as $t_d$, which must be introduced in order to avoid a shoot-through in bridge-arm and the short circuit situation on the primary side. The switches $S_1$ and $S_4$ are switched off at instant $t_3$. Due to the zero current of $S_1$, a ZCS turn-off is realized. After $S_4$ is turned off, a soft commutation occurs in $S_3$ and $S_4$: the current $i_{Lr}$ firstly charge the drain-source capacitance of $S_4$ and discharge that of $S_3$, then flow through the body-diode of $S_3$, hence, $v_{DS3}$ is clamped to zero. As a result, a ZVS turn-on can be realized by $S_3$ when the turn-on signal is applied on it. This stage is given in Fig.4(d).

From above it can be concluded that the primary-side

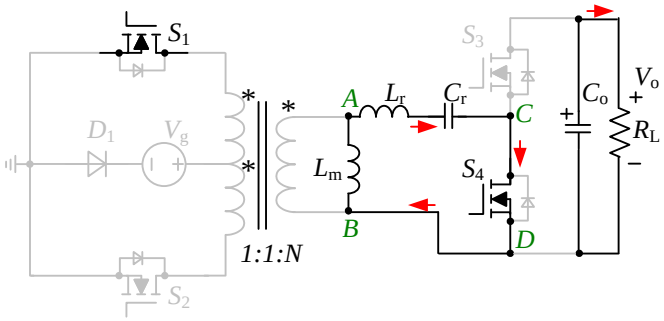
switches can realize both a ZCS turn-on and a ZCS turn-off. Meanwhile, the secondary-side switches can achieve a ZVS turn-on. Besides, the reverse recovery loss of the input diode is also alleviated due to the low decline rate of the diode current.



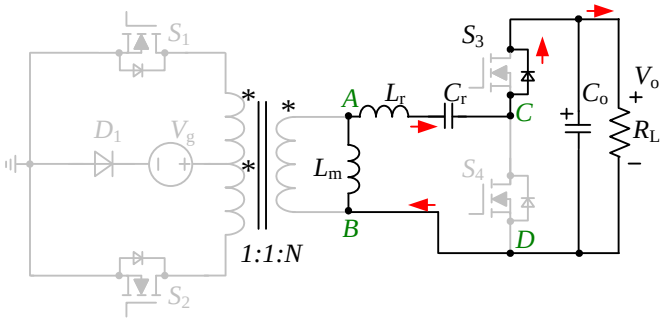

(a) Mode I ($t_0$<$t$<$t_1$)




(b) Mode II ($t_1$<$t$<$t_2$)




(c) Mode III ($t_2$<$t$<$t_3$)

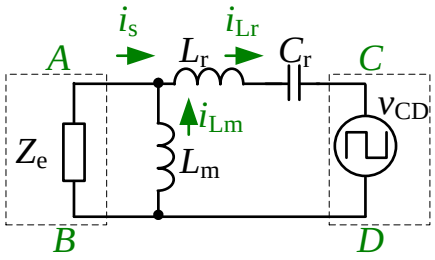



(d) Mode IV ($t_3$<$t$<$t_4$)

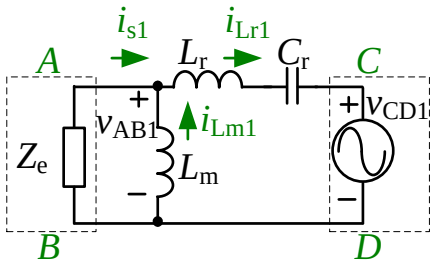
**Fig.4 Equivalent circuits of the proposed converter at different stages**

## IV. MODELING OF AN SECONDARY-SIDE *LLC* RESONANT CONVERTER

Normally, typical time-domain analysis method is hard to describe the relationship of electrical variables in a resonant converter so the First-Harmonic-Approximation (FHA) method is widely used, which produces acceptable design results as long as the converter operates at or close to the resonant frequency. In this section, the modeling process for *S-LLC* is proposed based on the FHA method. Some conclusions are directly showed in this part and the detailed derivation can be found in Appendix I.




(a) Nonlinear nonsinusoidal circuit.




(b) Linear sinusoidal circuit.

**Fig.5 Simplified converter circuit of the proposed converter**

The converter circuit of Fig.2 is simplified into Fig.5, where the obtained primary-side variables are referred to the secondary side. In the linear sinusoidal circuit Fig.5(b), only the fundamental harmonics of voltage and current are considered while all higher-order harmonics are ignored, where the subscript "1" is added in the variables to denote their fundamental components.

Due to the existence of diode $D_1$, the input current $i_g$ only flows in a positive direction. Besides, the input voltage can be reflected to the secondary side only if $D_1$ conducts, which means $v_{ab}$ equals $NV_g$ in this mode. During this period, there exists the energy exchange between the primary side and the secondary side. It needs to be pointed out that there is a phase difference between the fundamental harmonic of $v_{ab}$ and the fundamental harmonic of $i_s$ if $f_s$ < $f_r$. Hence, a complex-impedance $Z_e$ is placed to denote the AC equivalent impedance of the primary-side circuit. Considering the transformer turns ratio, $Z_e$ can be expressed as (3),

$$Z_e = -\frac{8N^2V_g}{\pi^2 I_g}\left[\sin\left(\frac{f_m\pi}{2}\right) - j\cos\left(\frac{f_m\pi}{2}\right)\right] \tag{3}$$

where $j$ means the imaginary unit, $f_m$ is defined as the normalized frequency and its expression is given as follows.

$$f_m = \frac{f_s}{f_r} \tag{4}$$

Obviously, the real part of $Z_e$ appears as a negative resistor to generate power. The equivalent model for the branch *AB* can be found in Appendix I.

If we define $M_{g\_DC}$ in (5) to denote the DC voltage conversion ratio reflected to the secondary-side circuit, i.e. the normalized voltage gain, then the complex-impedance $Z_e$ in (3)

can be transferred into another expression as shown in (6).

$$M_{g\_DC} = \frac{V_o}{NV_g} \tag{5}$$

$$\begin{aligned} Z_e &= -\frac{8N^2V_g^2R_L}{\pi^2V_o^2}[\sin(\frac{f_m\pi}{2}) - j\cos(\frac{f_m\pi}{2})] \\ &= -\frac{8R_L}{\pi^2M_{g\_DC}^2}[\sin(\frac{f_m\pi}{2}) - j\cos(\frac{f_m\pi}{2})] \end{aligned} \tag{6}$$

where $R_L$ is the load resistor.

In order to obtain the input-output relationship, some definitions are made as follows. Here we use $R_0$ and $Q$ to respectively denote the characteristic impedance and the quality factor.

$$R_0 = \sqrt{\frac{L_r}{C_r}} \tag{7}$$

$$Q = \frac{R_0}{R_L} \tag{8}$$

According to Fig.5, the DC input voltage and output voltage are converted into switching mode. Because the switches $S_3$ and $S_4$ form a asymmetric voltage doubler configuration as shown in Fig.2 [37, 38], so the DC voltage conversion ratio $M_{g\_DC}$ is approximately equal to twice the value of AC voltage ratio $M_{g\_AC}$ when the fundamental components are considered. So (5) can be transferred as follows.

$$M_{g\_DC} = \frac{V_o}{NV_g} \approx \frac{2V_{CD1\_RMS}}{V_{AB1\_RMS}} = 2M_{g\_AC} \tag{9}$$

Based on Fig.5(b), by expanding and synthesizing, $M_{g\_AC}$ can be finally expressed with the inductance ratio $L_n$ ($L_n$=$L_m$/$L_r$) and normalized frequency $f_m$ ($f_m$=$f_s$/$f_r$) as shown in (10).

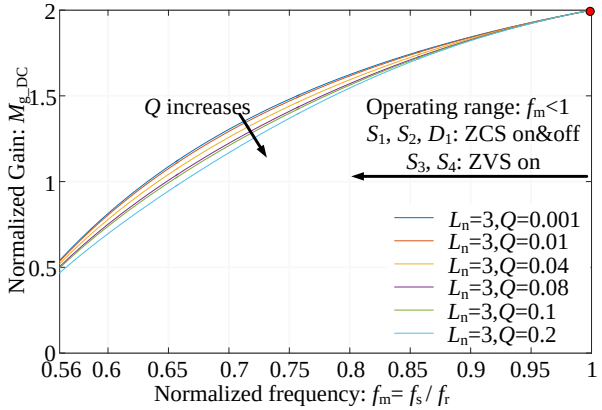
$$M_{g\_AC} = \left|(1+\frac{1}{L_n}-\frac{1}{L_nf_m^2}) + j\frac{R_0}{Z_e}(f_m - \frac{1}{f_m})\right| \tag{10}$$

By substituting (6) into (10) and considering (9), the relationship between $M_{g\_DC}$, $L_n$, $f_m$ and $Q$ can be found. Finally, $M_{g\_DC}$ can be simplified as (11).

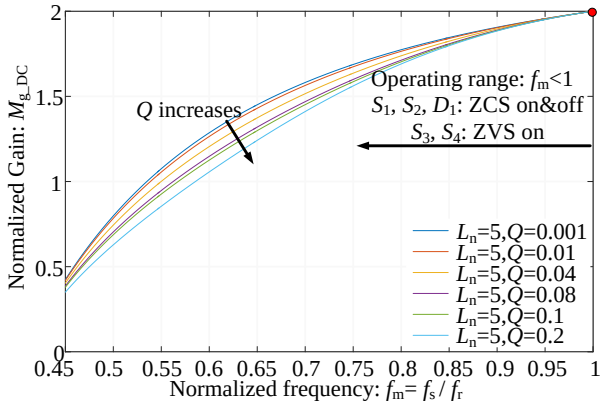
To ensure $M_{g\_DC}$ contains no imaginary part, some constraints can be obtained as follows.

$$\begin{cases} \sqrt{\dfrac{1}{1+L_n}} < f_m < 1 \\ Q < \dfrac{1}{\pi^2(1+\frac{1}{L_n}-\frac{1}{L_nf_m^2})(\frac{1}{f_m}-f_m)[1-\cos(\frac{f_m\pi}{2})]} \end{cases} \tag{12, 13}$$

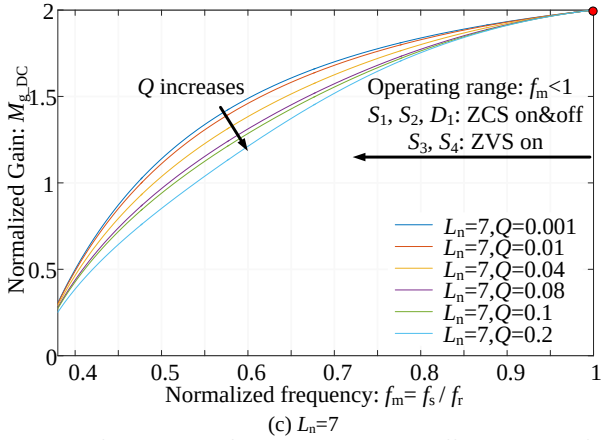
Equation (11) and the circuit model in Fig.5(b) form the basis for the design process. In the gain function shown in (11), $f_m$ is the control variable. $Q$ and $L_n$ are dummy variables because they are fixed values once the circuit parameters are determined. Hence, the voltage gain is adjusted through $f_m$. In order to clearly show the behavior of the voltage gain, $M_{g\_DC}$ is plotted with respect to $f_m$ at certain conditions from a group of values for $L_n$ and $Q$, as shown in Fig.6. Correspondingly, a group of simulated gain curves are given in Fig.7 as the verifications. The deviation increases as $f_s$ gets far from $f_r$ because the converter model is obtained under the assumption that $f_s$ is close to $f_r$. At a very low switching frequency, the converter will lose soft-switching feature and this will be explained in the Section V.B.




(a) $L_n$=3




(b) $L_n$=5




(c) $L_n$=7

**Fig.6 Plots of voltage-gain function ($M_{g\_DC}$) with different values of $L_n$.**

$$M_{g\_DC} = \sqrt{\frac{8[1-Q\pi^2(1+\frac{1}{L_n}-\frac{1}{L_nf_m^2})(f_m-\frac{1}{f_m})\cos(\frac{\pi}{2}f_m)] - 8\sqrt{[Q\pi^2(1+\frac{1}{L_n}-\frac{1}{L_nf_m^2})(f_m-\frac{1}{f_m})\cos(\frac{\pi}{2}f_m)-1]^2 - Q^2\pi^4(f_m-\frac{1}{f_m})^2(1+\frac{1}{L_n}-\frac{1}{L_nf_m^2})^2}}{Q^2\pi^4(f_m-\frac{1}{f_m})^2}} \tag{11}$$

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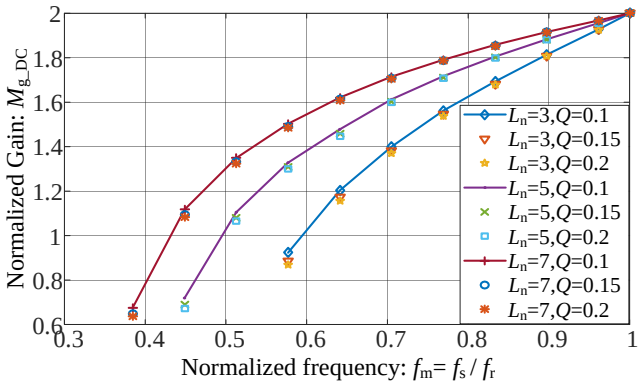



**Fig.7 Simulated points of voltage-gain function ($M_{g\_DC}$) with different values of $L_n$**

From Fig.6 it is obvious that the output voltage shows a monotonic relationship with the switching frequency, which is helpful to designing a closed-loop control system. Moreover, Fig.6 and Fig.7 also provide a hint that the quality factor $Q$ has little effect on the switching frequency range. Therefore, under a certain voltage gain, the switching frequency nearly does not change even if the load varies. This brings much convenience to the design process for a transformer. It is also a main advantage when compared with a total reverse structure of a regular *P-LLC*, which has a very wide switching frequency range when the converter operates into light-load condition [22-27].

## V. Design Considerations

### A. Selection for the transformer turns ratio

When designing an *S-LLC* converter, the turns ratio $N$ of the step-up transformer should be firstly determined. From Fig.3(a) it can be concluded that $f_s$ should be set close to $f_r$ so as to reduce the time duration $t_2$~$t_3$ since there is no active power transferred from input stage to the output stage in this duration. Hence, considering the input voltage range, $N$ can be calculated as follows. Please note that the turns ratio should not be set exactly equal to the value from (14) and some margin should be retained in order to counteract the gain decrease caused by the power loss.

$$N > \frac{V_o}{2V_{g\_\min}} \tag{14}$$

### B. Selection for resonant parameters

The resonant tank is made up by $L_r$, $L_m$ and $C_r$. The parameters not only determine the switching frequency range, but also affect the value range of $Q$. As given in (13), the maximum value of $Q$ should be limited. Otherwise, the predicted $M_{g\_DC}$ value may contain imaginary part and the FHA model is failure. According to (13), the permissible value of $Q_{max}$ is plotted with respect to $f_m$ at different $L_n$ conditions, as shown in Fig.8. It is clear that $Q_{max}$ is not a constant value. This value depends on not only the inductance ratio $L_n$, but also the normalized frequency $f_m$. From Fig.8 it is also clear that the permissible $Q_{max}$ decreases with the increase of $L_n$. To avoid the burdensome iterative process, $Q_{max}$ can be selected less than 0.2 in order to simplify the design process of the resonant tank. As defined in (8), a small $Q$ value can be realized by two methods. One is selecting a large $C_r$ and a small $L_r$, this leads to a small $R_0$ value, and the other way is increasing the load resistance $R_L$. Therefore, it can be concluded that the converter is suitable to be a step-up converter rather than a step-down one, because the load resistance usually shows a large value in a high-voltage output situation, which can decrease $Q$ value and bring convenience to the design process. For a practical design example, the nominal power $P$ and the output voltage $V_o$ are usually given as the specifications, which means the minimum value of $R_L$ is specified. In this condition, $C_r$ and $L_r$ should be adjusted to make up the permissible $Q_{max}$.

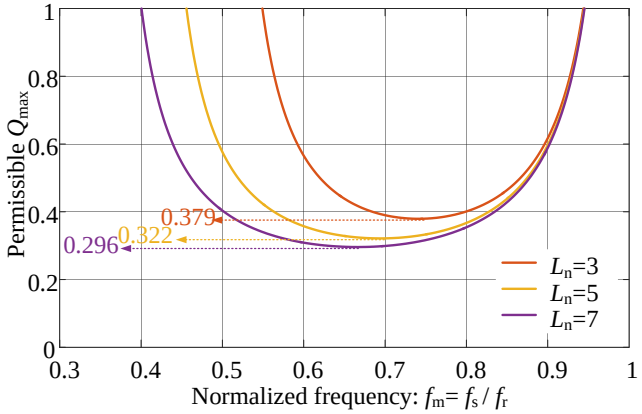


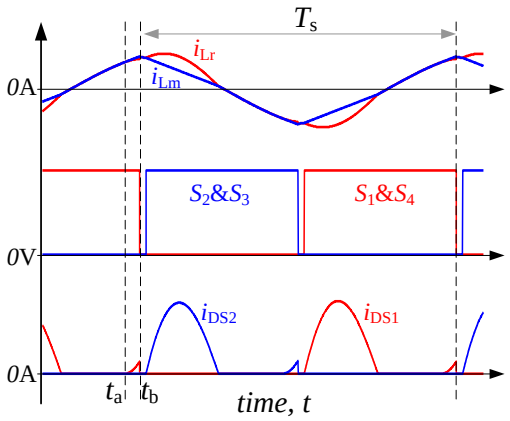

**Fig.8 Plots of $Q_{max}$-$f_m$ function with different values of $L_n$**

Once $L_r$ and $C_r$ are determined, the inductance ratio $L_n$ needs to be selected. From Fig.6, it is apparent that a small $L_n$ leads to a steep slope of the $M_{g\_DC}$ - $f_m$ curves. This narrows the switching frequency range and brings convenience to the transformer design. However, a too small $L_n$ may bring some problems. Typical waveforms under two different groups of circuit parameters are shown in Fig.9. Corresponding to the figures, the resonant parameters of the converters are the same with each other except the magnetizing inductance $L_m$, as well as the $L_n$ value. A small $L_n$ value can certainly narrowed the switching frequency range, but the ZCS turn-off for the primary-side switches may be lost, as shown in Fig.9(a). From $t_a$ to $t_b$, the magnetizing inductance $L_m$ is divorced from the resonant process because the slope of $i_{Lm}$ exceeds that of the resonant current $i_{Lr}$. This leads to the undesirable modes where the drain-source current is not zero. To avoid this situation, the slop of $i_{Lm}$ should be restrained. Obviously, a large inductance can decrease the slope of $i_{Lm}$ in order to eliminate the undesirable mode. Therefore, the boundary value for $L_m$ should be calculated. A simple method for estimating the minimum value of $L_m$ is given in Appendix II, under the assumption that the converter operates in the vicinity of the series resonant frequency $f_r$. It can be selected according to (15). From another point of view, there exists a minimum value for $f_s$ once the main circuit parameters are determined, according to (15). When $f_s$ is very low, the undesired operating mode can be also present.

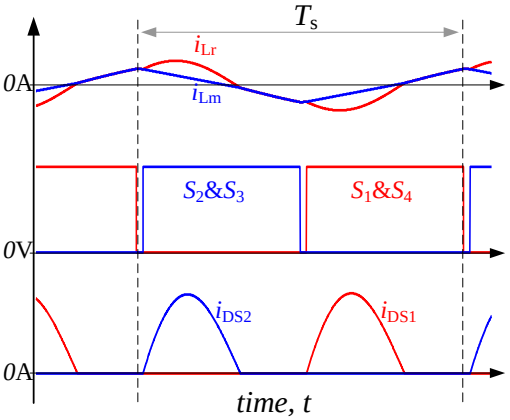
$$L_m > \frac{0.0353R_L}{f_s} \tag{15}$$

A flowchart for the design process of the proposed *S-LLC* converter is given in Fig.10, where the input voltage range $V_{g\_min}$~$V_{g\_max}$, nominal output voltage $V_o$ and maximum power point $P_{max}$ are given as the specifications. It should be noted that

the resonant inductor can be implemented only by the secondary-side leakage inductance, or by the synthesis of the leakage inductance and an additional inductor.




(a) $L_n$=2.5, $Q$=0.06




(b) $L_n$=5, $Q$=0.06

**Fig.9 typical waveforms corresponding to different $L_n$ values**

### C. Component stress

During the design process, the selection for the active switch and diode is mainly dependent on their voltage and current stresses. It is difficult to derive a precise time-domain solution for the device stress in a resonant converter when there are three or more resonant elements. Because the expressions that need to be solved become a group of differential equations with the third or higher order with respect to state variables. In this condition, the mathematical software or the simulation tool is usually recommended to help designers for the device selection. However, to simplify the design process, some approximate computation methods for the component stress can be still used instead, which are given as follows.

The key waveform of the input current $i_g$ is illustrated in Fig.11. It can be considered as a group of half-wave pulses, of which the natural resonant frequency is closed to $f_r$. If the peak value of the sinusoidal curve is denoted by $A_m$, the average value of input current, which is denoted by $I_g$, can be derived as follows.

Therefore, the amplitude of $i_g$, which is also the current stress value for $S_1$, $S_2$ and $D_1$, can be solved as shown in (17). Correspondingly, the current stress for the switches $S_3$ and $S_4$ can be calculated by dividing $A_m$ by $N$.

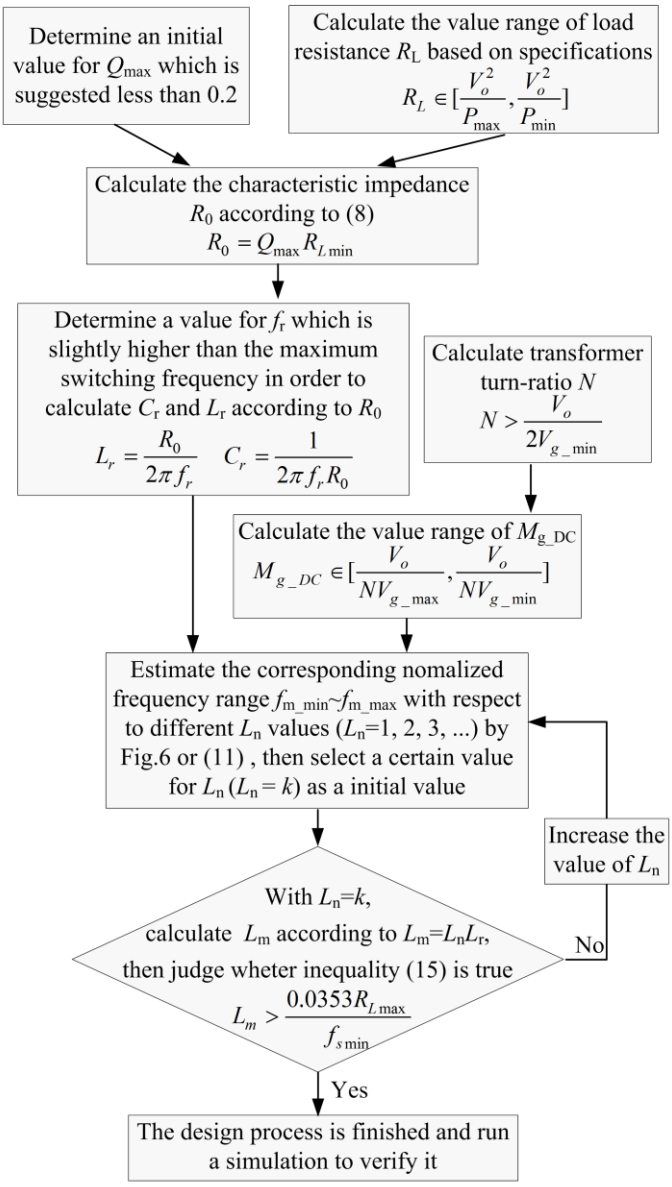



**Fig.10 Flowchart for the design process of the *S-LLC* converter**

$$I_g \approx 2 f_s \int_0^{1/(2f_r)} A_m \sin(\omega_r t) dt \tag{16}$$

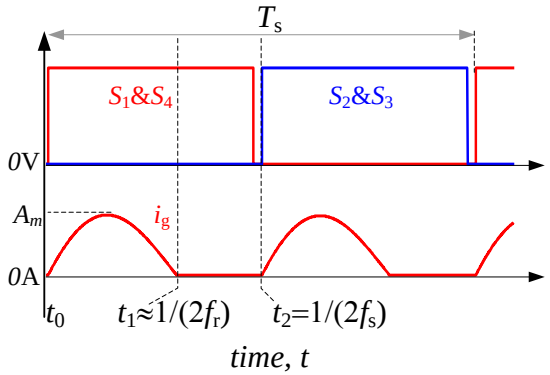



**Fig.11 Waveforms of the control signals and input current**

$$i_{g\_max} = A_m = \frac{\pi I_g}{2 f_m} = \frac{\pi P}{2 f_m V_g} \tag{17}$$

As for the voltage stress, it is obvious that the voltage

stresses of $S_3$ and $S_4$ are equal to the output voltage. Although the push-pull configuration is adopted as the input circuit, the voltage stresses of $S_1$ and $S_2$ are larger than $2V_g$ due to the operating Mode III. During these stages, the magnetizing inductor $L_m$ participates in the resonance. The inductor voltage $v_{ab}$ varies with the resonant process and meanwhile, this value reflected to the primary-side winding so $v_{DS1}$ and $v_{DS2}$ also change. The maximum values of $v_{DS1}$ and $v_{DS2}$ are equal to twice the value of $v_{ab}/N$, according to Fig.4(c). To simplify the computation process, here we suppose that the magnetizing current shows a triangular shape so the maximum current value of $i_{Lm}$ can be given as (18). This value can be approximately considered as the 1st order harmonic amplitude. If we suppose the magnetizing inductance voltage mainly depends on the 1st order harmonic component of $i_{Lm}$ during Mode III, the maximum value of $v_{AB}$ can be calculated in (19). Hence, the voltage stresses of $S_1$, $S_2$ and the input diode $D_1$ (or a SR MOSFET) can be respectively given in (20) and (21). Note that $\omega_s$ can be still used in (19), but (20) and (21) will produce constant results in that case. Here we use $\omega_r$ in (19) intentionally to make the results relevant to the normalized frequency, the result of which will achieve higher accuracy.

$$i_{Lm\_max} = \frac{NV_g}{4 f_s L_m} \tag{18}$$

$$v_{ab\_ModeIII} = \omega_r L_m i_{Lm\_max} \tag{19}$$

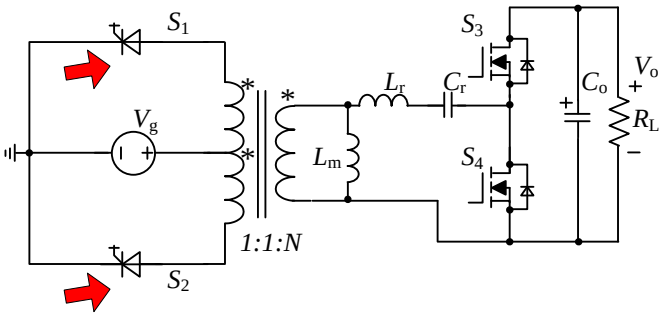
$$\begin{aligned} v_{DS1,DS2\_max} &= 2v_{ab\_ModeIII} / N \\ &= \pi V_g / f_m \end{aligned} \tag{20}$$

$$\begin{aligned} v_{D1\_max} &= v_{DS1,DS2\_max} - v_{ab\_ModeIII} / N - V_g \\ &= (\frac{\pi}{2 f_m} - 1) V_g \end{aligned} \tag{21}$$

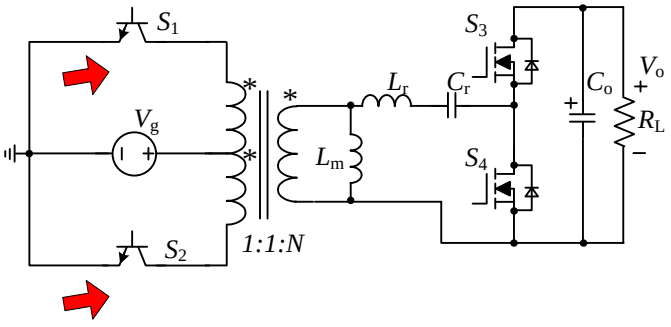
However, it must be pointed out that, because both the MOSFET and the diode are with the junction capacitance, there will be a voltage ringing during Mode III. The amplitude is also related to the stray inductance in the circuit and the junction capacitance value. Therefore, some margin should be retained in the device selection process and a simulation is necessary to verify the predicted results.

### *D. A discussion about the effect of the input diode $D_1$*

As mentioned above, because of the input diode, the magnetizing inductor $L_m$ is not always being clamped by the input voltage and it can participate in the resonant process with $L_r$ and $C_r$. With a simple PFM control, soft-switching can be easily realized by all switches. Hence, the input diode is the salient feature of the proposed converter. Some possible alternatives without the input diode can be found as shown in Fig.12, which employ the gate turn-off (GTO) thyristor or the bipolar junction transistor (BJT) as the primary-side switches in order to block the power back to the source. In this case, the proposed control strategy still works and the soft-switching features can be still obtained as before. However, the switching frequency of the GTO thyristor is not as high as a MOSFET so it will lead to a very large transformer size. Moreover, its forward voltage drop is much larger than that of a MOSFET, so the efficiency will be deteriorated. The BJT is usually applied in low power applications (normally below 100W), such as the auxiliary power supply for the controllers, sensors or driver chips. Its maximum rating can't satisfy higher power requirement. Therefore, they are not suitable for medium power level, but may be some solutions for other applications.




(a) GTO thyristor is applied as the primary-side switch




(b) BJT is applied as the primary-side switch

**Fig.12 Extended examples of the proposed *S-LLC* converter without the input diode**

## VI. EXPERIMENTAL VERIFICATION

A 500W prototype of the proposed converter with 36V~42V input and 380V output is built to verify the theoretical analysis results. The photograph of the prototype is shown in Fig.13.

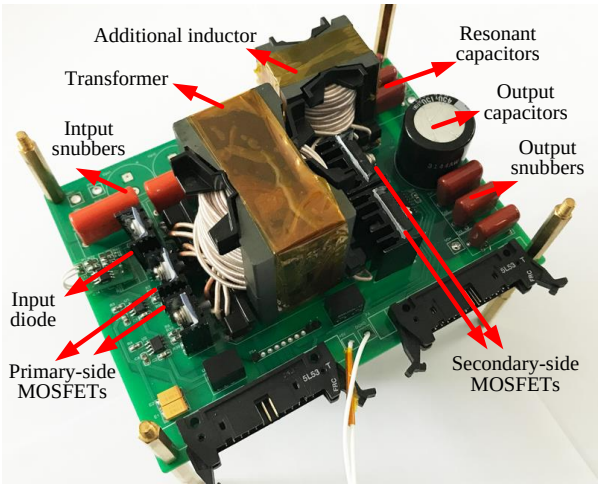



**Fig.13 Photograph of the proposed converter prototype**

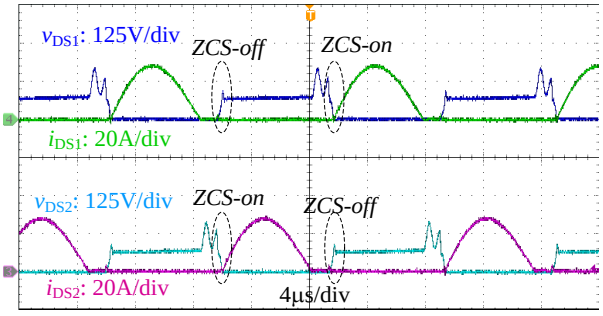
According to the design flowchart in Fig.10, the main circuit parameters are finally determined as shown in Table.I. According to (15), the minimum value of $L_m$ can be calculated corresponding to the load resistance. With the decrease of the output power, $L_{m\_min}$ increases. In our prototype, $L_n$ is determined equal to 6 in order to make sure the converter show a good operation performance above 200W. If power demand further decreases, the converter can be operated in a burst mode

to achieve high efficiency. In Table I, the leakage inductance reflected to the secondary side is denoted by $L_k$. Note that this value is still 7.6μH even though the transformer is manufactured with a sandwich-winding-structure, which is widely applied to reduce the leakage inductance in a transformer [39]. Since the resonant inductance is determined equal to 83μH, an additional inductor $L_a$ is supplemented.

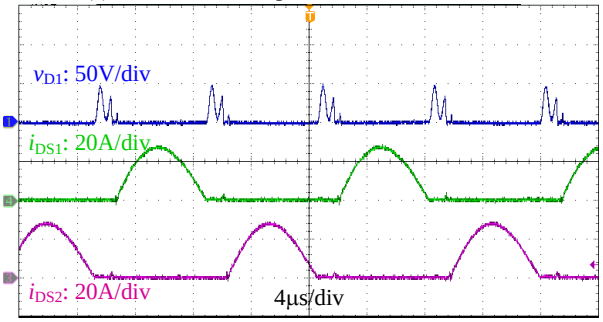
**TABLE I**
**MAIN CIRCUIT PARAMETERS OF THE PROTOTYPE**

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage | $V_g$ | 36V~42V |
| Output voltage | $V_o$ | 380V |
| Leakage inductance | $L_k$ | 7.6μH |
| Additional inductance | $L_a$ | 75.6μH |
| Magnetizing inductance | $L_m$ | 506μH |
| Resonant capacitance | $C_r$ | 50nF |
| Output filter capacitance | $C_o$ | 150μF |
| Transformer turns ratio | $N_{p1}$: $N_{p2}$:$N_s$ | 4:4:24 |
| Primary-side winding resistance | $R_{p1}$,$R_{p2}$ | 2.3mΩ, 2.1mΩ |
| Secondary-side winding resistance | $R_s$ | 19.2mΩ |
| Additional inductor's winding resistance | $R_{s\_a}$ | 19mΩ |
| Nominal Power | $P$ | 500W |
| Primary-side MOSFET | $S_1$, $S_2$ | IXFP80N25X3 |
| Secondary-side MOSFET | $S_3$, $S_4$ | IPW60R040CFD7 |
| Input diode | $D_1$ | V40100C-E3/4W |
| Transformer core | $T_1$ | PQ50/50-3C95 |
| Additional inductor core | $T_2$ | PQ35/35-3C95 |

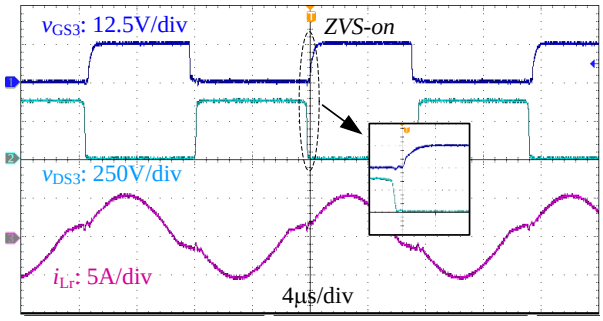
The key waveforms of the prototype are given in Fig.14 and Fig.15. It is obvious that all active switches realize the soft-switching. The ZCS turn-on and turn-off are obtained by the primary-side switches. The waveforms of driving pulses and the corresponding drain-source voltage of $S_3$ and $S_4$ are zoomed in. It is obvious that $v_{DS3}$ and $v_{DS4}$ already falls to zero before the rising edges of the driving pulses are applied. Therefore, the ZVS for $S_3$ and $S_4$ are achieved. Due to the low decline rate of the input current, the reverse-recovery problem of the input diode is also alleviated.



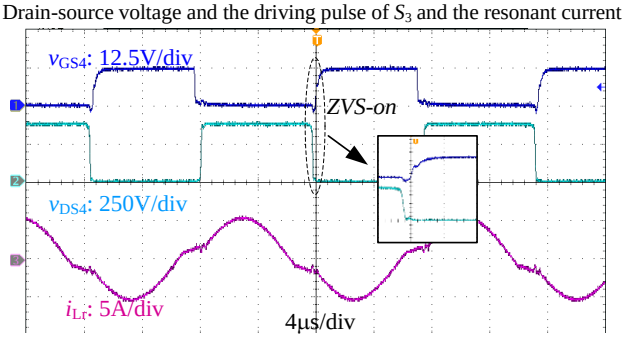

(a) Drain-source voltages and currents of $S_1$ and $S_2$




(b) Voltage of the diode $D_1$ and currents of $S_1$ and $S_2$

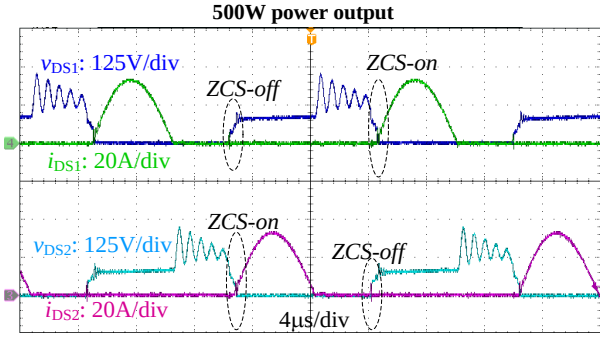



(c) Drain-source voltage and the driving pulse of $S_3$ and the resonant current $i_{Lr}$

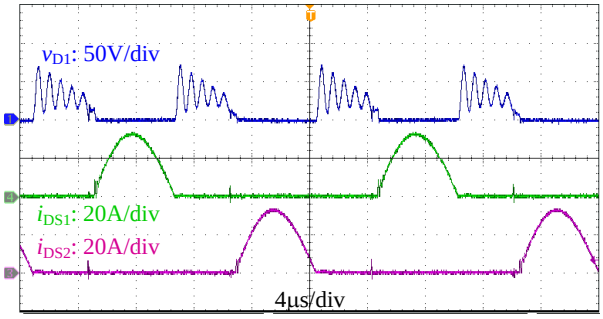



(d) Drain-source voltage and the driving pulses of $S_4$ and the resonant current $i_{Lr}$

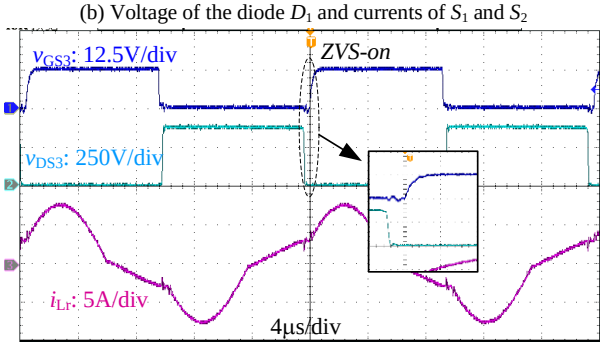
**Fig.14 Key waveforms of the prototype with 36V input voltage under 500W power output**



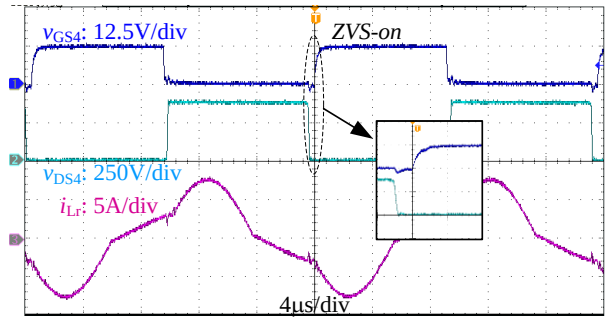

(a) Drain-source voltages and currents of $S_1$ and $S_2$




(b) Voltage of the diode $D_1$ and currents of $S_1$ and $S_2$




(c) Drain-source voltage and the driving pulses of $S_3$ and the resonant current $i_{Lr}$




(d) Drain-source voltage and the driving pulses of $S_4$ and the resonant current $i_{Lr}$

**Fig.15 Key waveforms of the prototype with 42V input voltage under 500W power output**

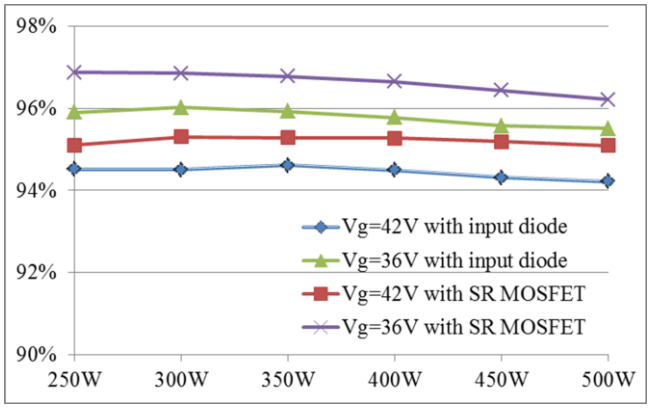



**Fig.16 Efficiency curves of the prototype with an input diode and a synchronous rectifier MOSFET**

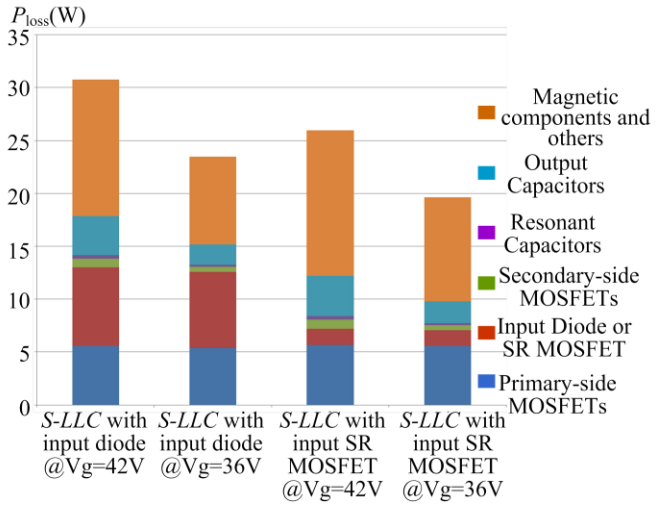
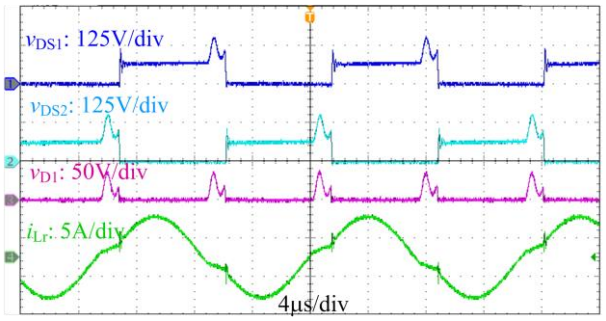
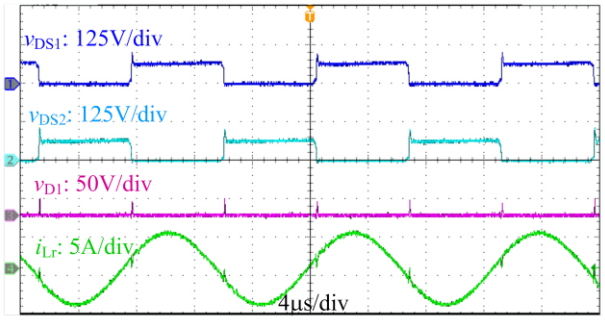



**Fig.17 Simulated power loss breakdown illustrations**

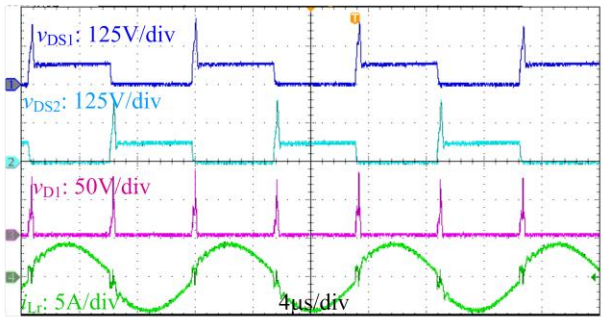
The efficiency curves of the prototype are given in Fig.16. To make an efficiency comparison, the input diode is replaced by a MOSFET (FDPF045N10A), which is driven by a synchronous rectification driver chip NCP4303A. It significantly reduces the primary-side power loss and brings benefit to the efficiency. Under nominal load condition, the converter efficiency is 95.5%@$V_g$=36V and 94.2%@$V_g$=42V with an input diode. The highest efficiency point is 96%@ $V_g$=36V at 300W power level. After the synchronous rectification is applied, the nominal efficiency is promoted to 96.2%@$V_g$=36V and 95.1%@$V_g$=42V. Meanwhile, the highest efficiency can reach 96.9%@$V_g$=36V at 250W power level.




(a) $f_s$=68kHz<$f_r$




(b) $f_s$=78kHz=$f_r$




(c) $f_s$=88kHz>$f_r$

**Fig.18 Key waveforms when the converter operates with different switching frequencies ($V_g$=36V, $R_L$=289Ω)**

Corresponding to the nominal power condition, the simulated loss breakdown illustrations are also provided in Fig.17. Because the actual loss for each component can't be measured in practical, we use the parameter information provided by manufacturer's datasheet to build the loss model for each component, including the primary and secondary-side MOSFETs, input diode, resonant capacitors, output capacitors. By subtracting the sum of these simulated losses from a practical measured loss in experiment, the "magnetic components and others" item in the pie chart is obtained. It needs to point out that the power losses of the transformer and inductor cores are related to the switching frequency. However, there is no information about the core loss in the datasheet corresponding to a switching frequency range below 100kHz. Therefore, the transformer loss is hard to be accurately predicted as an individual part. So does the extra inductor.

It also needs to be pointed out that the switching frequency of the converter almost does not change under a desirable voltage gain (please refer to the $M_{g\_DC}$ - $f_m$ plots in Fig.6). This characteristics is similar to a basic chopper converter that the voltage conversion ratio is only related to the duty ratio of the pulse. From 250W to 500W power condition, the switching

frequency range is 62kHz~65kHz under 36V input condition while it is 50kHz~53kHz under 42V input condition.

In order to make a comparison, the key waveforms of experimental results of the prototype operating below, at, and above the resonant frequency are also given in Fig.18, respectively. Since the practical resonant frequency is 78kHz according to the measured circuit parameters, the switching frequencies of comparison experiments are selected to 68kHz and 88kHz, respectively. Theoretically, as explained in Section III, there will be voltage spikes on the primary-side switches if $f_s \geq f_r$. This is verified by Fig.18(c), where the drain-source voltages of $S_1$ and $S_2$ show serious spikes and so does the diode $D_1$. However, this phenomenon is not obvious in Fig.18(b). As illustrated in Fig.3(b), the spikes are caused by the switching dead-time and the energy of spikes are also related to it. Due to the tiny switching dead-time (250ns) in the experiment, the spikes are significantly alleviated by the junction capacitance of the switches and diode.

## VII. THE COMPARISON FOR DIFFERENT RESONANT CONVERTERS IN A HIGH STEP-UP APPLICATION

Some literatures have proposed different methods that utilizing the forward or backward power flow in a traditional *LLC* converter, or some derived resonant converters, to achieve the step-up function [18-26, 28]. In this section, a brief comparison between the proposed *S-LLC* and some other resonant converters is made under the specifications given in Section VI.

Firstly, a normal design process for a traditional *P-LLC* converter is given as follows. Since the operating frequency is usually set near the natural resonant frequency to achieve high efficiency, the step-up turns ratio $N$ is determined by $N=V_o/V_g$ in a regular *LLC* with full-bridge or push-pull inverter stage, and with a full-bridge or a full-wave rectifier stage. According to a 36V~42V input range and 380V output voltage, $N$ is determined equal to 9.1~10.5. Hence, $N$=9.1 is as a conservative selection. A small inductance ratio ($L_n=L_m/L_r$) usually results in a small magnetizing inductance, which can lead to a high magnetizing current and produce significant conduction loss, while a large $L_n$ can result a wide switching frequency range which is not conducive to a transformer design. Therefore, the inductance ratio is usually selected in the range from 3 to 6 empirically [29, 40], so to achieve a balance between the switching frequency range and the magnetizing current value. The quality factor $Q$ is selected based on a given $L_n$ and the required maximum gain. It is obtained from the gain-curve plots as shown in Fig.19, which is created beforehand and as a common tool in the design process for a regular *P-LLC* [29, 40]. The selection of $Q$ must ensure that its corresponding attainable peak gain is larger than the required gain (380V/9.1/36V=1.12) so to cover the whole voltage range. With the mentioned design process, Table II gives a group of resonant parameters for the *P-LLC* with different $L_n$ values equal to 3~6, respectively. The resonant frequency $f_r$ is set to 70kHz and 80kHz, respectively. Hence, the theoretical switching frequency range is close to the *S-LLC* prototype.

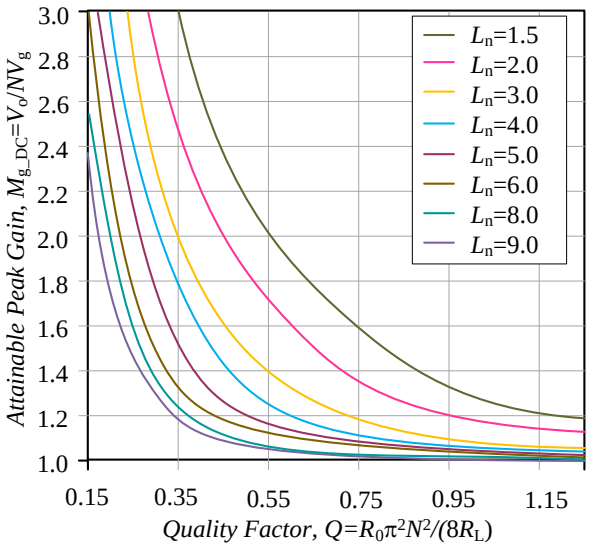



**Fig.19 Gain-curve plots used in a regular *P-LLC* design process [29]**

If the output rectifier stage is realized by the full-bridge or a full-wave rectifier structure, which means the natural voltage gain of the rectifier stage equals 1, the voltage step-up function is mainly realized by the turns ratio and the resonant tank. In this case, the transformer turns ratio is nearly equal to 1/9.1. Although the turn ratio can be reduced to 1/4.6 after a voltage doubler is adopted, however, the conductive loss of the rectifier diode still greatly reduces the efficiency. Active switches can be applied instead of the diode to improve efficiency and realize the SR function as the *S-LLC* converter does. However, the duty ratio of the driving pulse for the secondary-side switch depends on the time instant of the current zero-crossing point. As mentioned before, a CT or an analog SR chip can achieve this function. The analog SR chip with advanced IC integrated technology is a preferred solution but its maximum drain-source detection voltage rating is below 250V at the present stage [36] (Note that the output is 380V in the prototype.). The CT scheme requires additional signal conversion circuit to generate driving pulses, where the layout must be carefully considered so as to reduce stray parameters. Besides, the signal filtering delay and the effect of the CT's leakage and magnetizing inductance can also limit its bandwidth. This greatly increases the converter complexity. In addition, the ESR loss in the *P-LLC* converter is still a big issue. This loss is proportional to the square of the resonant current RMS value. That means the resonant capacitor ESR in the *P-LLC* converter needs to be decreased to $1/N^2$ of the value of the ESR in the *S-LLC* converter under the same ESR loss condition. This will result in a very large count of resonant capacitors in parallel in the *P-LLC*.

In order to reduce Peak/RMS value of the resonant current, [18] proposed a notch filter which can be introduced into a traditional *P-LLC* so as to improve efficiency. However, compared with a traditional *P-LLC*, at least two more components need to be introduced. Moreover, the SR problem still exists and the main resonant components are still placed on the primary side.

**TABLE II**
**A GROUP OF RESONANT PARAMETERS WITH DIFFERENT INDUCTANCE RATIO IN A *P-LLC*. (*P*=500W, $V_{IN}$=36V~42V, $V_{OUT}$=380V)**

| $Q=R_0\pi^2N^2/(8R_L)$ | 1: *N* | $L_r$ | $L_m$ | $C_r$ | $f_{s\_min}$~$f_{s\_max}$ | $f_r$ |
|---|---|---|---|---|---|---|
| 0.7 | 1: 9.1 | 4μH | 12μH | 997nF | 70-80kHz | 80kHz |
| 0.57 | 1: 9.1 | 3.2μH | 13μH | 1224nF | 60~80kHz | |
| 0.49 | 1: 9.1 | 2.8μH | 14μH | 1424nF | 50-80kHz | |
| 0.44 | 1: 9.1 | 2.5μH | 15μH | 1622nF | 45-80kHz | |
| 0.67 | 1:9.1 | 4.2μH | 13μH | 1155nF | 55~70kHz | 70kHz |
| 0.58 | 1:9.1 | 3.8μH | 15μH | 1399nF | 50~70kHz | |
| 0.48 | 1:9.1 | 3.1μH | 16μH | 1650nF | 45~70kHz | |
| 0.45 | 1:9.1 | 3μH | 17μH | 1812nF | 40~70kHz | |

Different converters with secondary-side resonant tank are proposed in [19-26, 28] and some of them are with SR features for the rectifier stage [21-26]. Table III gives a brief performance comparison between the proposed *S-LLC*, the *P-LLC* and some resonant converters mentioned above. In order to make a fair comparison, the component count is estimated under the assumption that the converters try to use the same inverter structure and the same rectifier structure. Obviously, the regular *P-LLC* is with the minimum component count.

The total reverse structure of a regular *P-LLC* is utilized to achieve high step-up function in [22-24, 26]. Therefore, they are with the same component count as a *P-LLC*. However, since the resonant tank is not a typical $L_r$-$L_m$-$C_r$ but an $L_r$-$C_r$ configuration, the converter's feature is similar to an SRC as discussed in [25]. To simplify the SR realization for the rectifier stage, the converters in [22-24] are operated with fixed switching frequency to provide constant voltage gain. Literature [26] provided a novel control strategy to achieve a wide voltage range, but it is complicated and the realization of SR is hard to be preciously controlled. Compared with *P-LLC*, [20] and [21] both employed one additional inductor at the input AC port of the rectifier stage. Although the proposed *S-LLC* also introduced one extra element (the input diode), the size and weight of a diode are much less than a power inductor. Moreover, the SR realization for the rectifier stage in [20] is still complex as a *P-LLC*. Literature [21] proposed a control scheme to achieve a natural SR realization, but the high-voltage side switches are always operated with constant conducting time and the voltage gain still needs to be regulated by adjusting the switching frequency for both primary-side and secondary-side switches. Therefore, the control algorithm is more complex than a simple PFM control in the proposed *S-LLC*. The converter in [19] belongs to the quasi-resonant converter with a secondary-side resonant tank. It utilized the voltage quadrupler rectifier to significantly reduce the transformer turns ratio but it needs 6 diodes at high-voltage side, so SR is costly and hard to be implemented. It is operated with a simple PFM control strategy, but the transformer size is large due to the wide switching frequency range. The converter in [28] can be considered as an improvement of the reverse structure of a regular *P-LLC*. Two GaN switches are employed to form an equivalent bidirectional switch on the secondary side. By this means, the leakage inductance can be utilized, which accumulates energy during the conducting time of the GaN switch and boost the voltage when it is off. Compared with the *P-LLC* converter, it introduces at least two GaN switches. Besides, it leads to a floating driver ground and the control algorithm is complex. Moreover, its realization for SR in the converter is similar to a *P-LLC*.

In the proposed *S-LLC* converter, both the duty ratio and the switching frequency for the secondary-side switches are the same with the primary-side switches. Meanwhile, no current zero-crossing detection is needed when an input diode is applied. So this significantly simplifies the control system. Compared with the total reverse structure of a regular *P-LLC*, the proposed *S-LLC* converter introduces only one input diode or a rectifier switch. Since the quality factor has little effect on the slope of the gain curves, its voltage regulation ability always shows a good performance in both light-load and heavy-load condition. This is also an improvement when compared with a total reverse structure of a regular *P-LLC* [22-27]. Under the specification in Section VI, the efficiency of the *S-LLC* can reach 94.2%~95.5%@500W with an input diode, and can reach 95.1%~96.2%@500W with a SR switch. In both situations, the same PFM control strategy is applied. Moreover, due to the common ground connection of the primary-side switches, the auxiliary power supply of driver chips for $S_1$ and $S_2$ can also powers the analog SR chip. So it is a simple solution to achieve high step-up function with high efficiency.

## VIII. CONCLUSIONS

A secondary-side *LLC* (*S-LLC*) resonant converter which is

**TABLE III**
**PERFORMANCE COMPARISON**

| | the proposed *S-LLC* | the regular *P-LLC* | [18] | [19] | [20] | [21] | [22-24] | [26] | [28] |
|---|---|---|---|---|---|---|---|---|---|
| **Component count** | low | very low | medium | high | low | low | very low | very low | medium |
| **Complexity of SR** | simple | complex | complex | very complex | complex | simple | simple | complex | complex |
| **Control strategy** | PFM | PFM | PFM | PFM | PFM | PFM with constant conducting time | fixed switching frequency | calculate the conducting time on line based on the state-plane diagram | PS and duty-ratio control |
| **Voltage gain** | variable | variable | variable | variable | variable | variable | fixed | variable | variable |
| **Volume** | small | small | medium | large | medium | medium | small | small | small |

suitable for achieving high step-up function is proposed in this paper. Different from the reverse structure of a regular *LLC* converter, an input diode (or a SR switch) is introduced so as to make the magnetizing inductance free from being always clamped by the input voltage. Besides, the rectifier stage consists of active switches instead of diodes. Under a simple PFM control with the same 0.5 duty ratio for both the primary-side and secondary-side switches, high step-up function can be easily realized by the converter with good load regulation ability. In order to further improve the efficiency, the input diode can be replaced by a synchronous rectifier MOSFET with an analog SR chip, without changing the control strategy. All the switches and the diode can achieve the soft-switching and this leads to a good efficiency performance. The modeling process and the corresponding design considerations for the proposed converter are given in detail. A 500W prototype has been built and the experimental results show good agreements with the theoretical analysis.

## APPENDIX I

### *A. Equivalent model of branch AB in* Fig.5

Some key waveforms are given in Fig.A1 in order to show the modeling process of FHA method for the *S-LLC* converter. The fundamental components of $i_{Lr}$ and $i_s$ are illustrated with dash line to clearly show their phase difference with corresponding voltages. Under the assumption that the converter operates in the vicinity of the series resonant frequency $f_r$, the inverter stage, resonant tank and the rectifier stage can be respectively modeled by FHA method. The subscript "1" is added in the variables to denote their fundamental components. According to Fig.5, the first harmonic of $v_{AB}$ can be expressed as follows, where $\alpha$ denotes its initial angle and $\alpha = 0$ according to Fig.A1.

$$v_{AB1}(t) = \sqrt{2}V_{AB1\_RMS}\sin(2\pi f_s t + \alpha) \tag{A1}$$

Although the voltage value of $v_{AB}$ is not equal to $\pm NV_g$ in the time duration $t_1$~$t_2$, however, when $f_s$ is close to $f_r$, this time duration is very limited. To simplify the modeling process, the waveform of $v_{AB}$ can be approximately considered as the square waveform. This is reasonable since similar simplification process can be also found in a regular *P-LLC* converter's rectifier stage, to obtain the AC load equivalent resistance. When a typical *P-LLC* operates below the natural resonant frequency, the rectifier diode is in discontinuous current mode. Correspondingly, the voltage across the AC input port of the rectifier stage is neither $\pm V_o$ nor zero. However, under the assumption that $f_s$ is near $f_r$, this voltage can be approximately considered as a 50% square wave, so the AC load equivalent resistance can be simplified equal to $8R_L/\pi^2$ ($R_L$ is the load resistance) [23, 34, 40].

As a result, (A1) can be transferred into (A2).

$$\begin{aligned} v_{AB1}(t) &= \sqrt{2}V_{AB1\_RMS}\sin(2\pi f_s t + \alpha) \\ &= \frac{4NV_g}{\pi}\sin(2\pi f_s t + \alpha) \end{aligned} \tag{A2}$$

Therefore, the relationship between $V_{AB1\_RMS}$ and $V_g$ can be obtained in (A3).

$$V_{AB1\_RMS} = \frac{2\sqrt{2}NV_g}{\pi} \tag{A3}$$

Because the fundamental harmonic of $i_s$ has a phase angle $\theta$ with $v_{AB}$, so the expression of $i_{s1}$ can be given in (A4).

$$i_{s1}(t) = \sqrt{2}I_{s1\_RMS}\sin(2\pi f_s t + \alpha + \theta) \tag{A4}$$

Considering the relationship between $i_{s1}(t)$ and average input current $I_g$, (A4) can be expressed in another form.

$$\begin{aligned} i_{s1}(t) &= \sqrt{2}I_{s1\_RMS}\sin(2\pi f_s t + \alpha + \theta) \\ &= \frac{\pi I_g}{2N}\sin(2\pi f_s t + \alpha + \theta) \end{aligned} \tag{A5}$$

Therefore, the inverter stage, i.e. the branch *AB* in Fig.5, appears like a complex-impedance. Here we use $Z_e$ to denote that. So we can obtain its expression as shown in (A6)

$$Z_e = -\frac{8N^2V_g}{\pi^2 I_g}(\cos(-\theta) + j\sin(-\theta)) \tag{A6}$$

where $j$ means the imaginary unit. Obviously, the real part of $Z_e$ appears like a negative resistor to generate power. According to the Fig.A1, the phase angle $\theta$ can be calculated by (A7)

$$\theta = \frac{1}{2}\left(\frac{T_s}{2} - \frac{T_r}{2}\right)\cdot\frac{2\pi}{T_s} = \frac{\pi}{2} - \frac{\pi f_m}{2} \tag{A7}$$

where $f_m = f_s/f_r$. Therefore, $Z_e$ can be simplified as shown in (6).

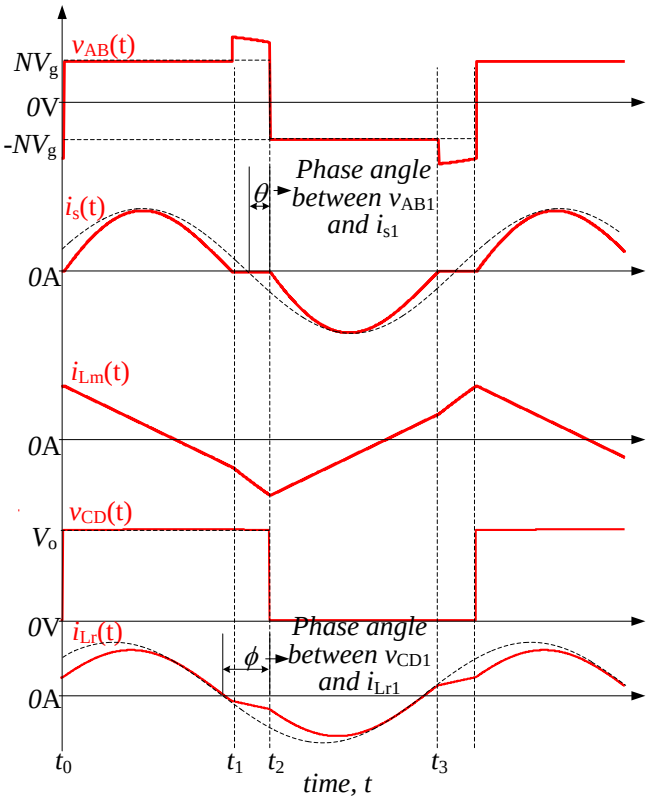



**Fig.A1 Key waveforms of the *S-LLC* converter**

### *B. Equivalent model of branch CD in* Fig.5

The switches $S_3$ and $S_4$ conduct alternatively with the same duty ratio (0.5) so $v_{CD}$ can be considered as a unipolar square-wave voltage source. Therefore, the fundamental component of $v_{CD}$ can be given as follows, where $\beta$ denotes its initial phase angle.

$$\begin{aligned} v_{CD1}(t) &= \frac{2V_o}{\pi}\sin(\omega_s t+\beta) \\ &= \sqrt{2}V_{CD1\_RMS}\sin(\omega_s t+\beta) \end{aligned} \tag{A8}$$

Meanwhile, the following equation can be obtained.

$$V_{CD1\_RMS} = \frac{\sqrt{2}V_o}{\pi} \tag{A9}$$

The current through the branch *CD* is the same with $i_{Lr}$. The fundamental of $i_{CD}$ is defined as follows.

$$\begin{aligned} i_{CD1}(t) &= i_{Lr1}(t) \\ &= \sqrt{2}I_{CD1\_RMS}\sin(\omega_s t+\beta+\phi) \end{aligned} \tag{A10}$$

where $\phi$ is the phase difference between $v_{CD1}$ and $i_{Lr1}$. Note that the branch *CD* appears like a voltage source.

*C. Calculation of the voltage conversion ratio reflected to the secondary side*

The voltage conversion ratio reflected to the secondary-side circuit (i.e. normalized voltage gain) is defined in (5), and it can be transferred into (A11) according to (A3) and (A9).

$$\begin{aligned} M_{g\_DC} &= \frac{V_o}{NV_g} \\ &= \frac{1}{N}*\frac{V_o}{V_{CD1\_RMS}}*\frac{V_{CD1\_RMS}}{V_{AB1\_RMS}}*\frac{V_{AB1\_RMS}}{V_g} \\ &\approx \frac{2V_{CD1\_RMS}}{V_{AB1\_RMS}} \\ &= 2M_{g\_AC} \end{aligned} \tag{A11}$$

According to Fig.5(b), (A11) can be transferred into (A12).

$$\begin{aligned} M_{g\_DC} &\approx 2M_{g\_AC} \\ &= \frac{2V_{CD1\_RMS}}{V_{AB1\_RMS}} \\ &= 2\left|\left(\frac{Z_e \parallel j\omega_s L_m}{Z_e \parallel j\omega_s L_m + j\omega_s L_r + \frac{1}{j\omega_s C_r}}\right)^{-1}\right| \\ &= 2\left|\left(1+\frac{1}{L_n}-\frac{1}{L_n f_m^2}\right)+j\frac{R_0}{Z_e}\left(f_m-\frac{1}{f_m}\right)\right| \\ &= 2\left|\begin{array}{l}\left[\left(1+\frac{1}{L_n}-\frac{1}{L_n f_m^2}\right)+\frac{Q\pi^2 M_{g\_DC}^2}{8}\left(f_m-\frac{1}{f_m}\right)\cos\left(\frac{f_m\pi}{2}\right)\right] \\ -j\left[\frac{Q\pi^2 M_{g\_DC}^2}{8}\left(f_m-\frac{1}{f_m}\right)\sin\left(\frac{f_m\pi}{2}\right)\right]\end{array}\right| \end{aligned} \tag{A12}$$

where $Q=R_0/R_L$, $L_n=L_m/L_r$ and $f_m=f_s/f_r$.

According to (A12), $M_{g\_DC}$ can be expressed as shown in (A13). Hence, (A14) can be derived and the solution for (A14) can be obtained as shown in (11).

$$M_{g\_DC} \approx 2\sqrt{\left[\left(1+\frac{1}{L_n}-\frac{1}{L_n f_m^2}\right)+\frac{Q\pi^2 M_{g\_DC}^2}{8}\left(f_m-\frac{1}{f_m}\right)\cos\left(\frac{f_m\pi}{2}\right)\right]^2+\left[\frac{Q\pi^2 M_{g\_DC}^2}{8}\left(f_m-\frac{1}{f_m}\right)\sin\left(\frac{f_m\pi}{2}\right)\right]^2} \tag{A13}$$

$$\left[\frac{Q\pi^2}{8}\left(f_m-\frac{1}{f_m}\right)\right]^2 M_{g\_DC}^4+\frac{1}{4}\left[Q\pi^2\left(1+\frac{1}{L_n}-\frac{1}{L_n f_m^2}\right)\left(f_m-\frac{1}{f_m}\right)\cos\left(\frac{\pi f_m}{2}\right)-1\right]M_{g\_DC}^2+\left(1+\frac{1}{L_n}-\frac{1}{L_n f_m^2}\right)^2=0 \tag{A14}$$

## APPENDIX II

Under the assumption that the converter operates in the vicinity of the series resonant frequency $f_r$, the minimum value of $L_m$ can be calculated by considering the switching frequency is equal to $f_r$. Note that $M_{g\_DC}$ always equals 2 if $f_m$ equals 1 as shown in Fig.6.

The state equation for $i_{Lm}$ can be given in (B1). The slope for $i_{Lm}$ is $NV_g/L_m$.

$$L_m\frac{di_{Lm}}{dt} = 4L_m f_s i_{Lm\_max} = NV_g \tag{B1}$$

The magnetizing inductance $L_m$ only contributes passive power to the converter, which can be calculated in (B2)

$$q_{passives} = 2L_m i_{Lm\_max}^2 f_s = \frac{N^2V_g^2}{8L_m f_s} \tag{B2}$$

If $L_m$ is sufficiently large, $q_{passive}$ equals zero. There is only active power distributed in the converter. In this condition, the amplitude of $i_{Lr}$ can be calculated by (B3), where $p_{active}$ denotes the active power.

$$i_{Lr\_amplitude\_activepower} = \frac{\pi p_{active}}{2NV_g} \tag{B3}$$

When a practical $L_m$ value has been taken into account, the amplitude value of $i_{Lr}$ can be revised into (B4), according to (B2) and (B3).

$$\begin{aligned} i_{Lr\_amplitude} &= \frac{\pi\left(\sqrt{p_{active}^2+q_{passive}^2}\right)}{2NV_g} \\ &= \frac{\pi NV_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}} \end{aligned} \tag{B4}$$

Therefore, the time-domain expression for $i_{Lr}$ can be given in (B5).

$$i_{Lr}(t) = \frac{\pi NV_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}\sin(\omega_s t+\gamma) \tag{B5}$$

According to Fig.9, $i_{Lr}$ increases to $i_{Lm\_max}$ at $t_b$ instant. Hence, (B6) can be derived.

$$\frac{\pi NV_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}\sin(\omega_s t_b+\gamma) = i_{Lm\_max} \tag{B6}$$

Then, the slope of $i_{Lr}(t=t_b)$ can be obtained according to (B7).

$$\frac{di_{Lr}(t)}{dt}\Big|_{t=t_b} = \frac{\omega_s \pi N V_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}\cos(\omega_s t_b+\gamma)$$
$$= \frac{\omega_s \pi N V_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}\sqrt{1-\left(\frac{2i_{Lm\_max}}{\pi N V_g\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}}\right)^2} \quad \text{(B7)}$$

According to (B1), the slope of $i_{\mathrm{Lm}}$ is $NV_{\mathrm{g}}/L_{\mathrm{m}}$, which must be less than the slope of $i_{\mathrm{Lr}}$ at $t_{\mathrm{b}}$ instant. Therefore, inequality (B8) can be obtained.

$$\frac{NV_g}{L_m} < \frac{\omega_s \pi N V_g}{2}\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}\sqrt{1-\left(\frac{2i_{Lm\_max}}{\pi N V_g\sqrt{\frac{16}{R_L^2}+\frac{1}{64L_m^2 f_s^2}}}\right)^2} \quad \text{(B8)}$$

By substituting $i_{\mathrm{Lm\_max}}$, which can be derived from (B1), into (B8), the constraint for $L_{\mathrm{m}}$ can be derived as shown in (B9).

$$\frac{\omega_s \pi}{2}\sqrt{\frac{16L_m^2}{R_L^2}+\frac{\pi^2-16}{64\pi^2 f_s^2}} > 1 \quad \text{(B9)}$$

With further simplification, (B9) can be transferred into (15).

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