Comparison of GaN- and Silicon FET-Based Active Clamp Flyback Converters

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ABSTRACT

This session demonstrates how an active clamp flyback converter achieves zero voltage switching (ZVS) and recycles the leakage energy of the transformer to improve efficiency in higher frequency operation. Although it is well known that switch-node capacitance determines the circulating energy for ZVS, the capacitance-nonlinearity impact from each of the two primary-side switches and from the secondary synchronous rectifier has not been well understood. In this session, design tradeoffs with differing nonlinearity of junction capacitances from each of the switching devices are investigated across full load to deep light load operation, and then proper control strategies to overcome the capacitance nonlinearity are proposed. Additionally, analytical equations and design procedures are developed with consideration to the nonlinearity impact. Finally, the above studies and control method are supported with experimental results and simulation results on a 30 W adapter using state-of-the-art GaN and silicon FETs.

I. INTRODUCTION

With the rapid development of portable devices and the quick charging technology of batteries, the increasing load demand requires the travel adapter to have significant power density improvement. Moreover, the migration of high-current USB Type- C™ cables and the new USB Power Delivery (PD) standard urge the need for more efficient power conversion [1][2]. Three start-of-the art topologies for travel adapters have been proposed: conventional passive-clamp flyback (PCF) [3][4][5], active-clamp flyback (ACF) [6][7][8] and three-level LLC resonant converters [9]. Figure 1 shows the circuit diagram of the three topologies and Table 1 summarizes the technology comparison of three power stage designs for a 65 W notebook adapter. Both ACF and three-level LLC can achieve soft switching, which eliminates switching loss in high frequency operation (higher than 130 kHz). These converters reduce the passive component size of the transformer, EMI filter and output capacitors for higher power density designs.

A PCF circuit contains a high voltage diode in series with a TVS or an R-C circuit; in contrast, an ACF is constructed with a high voltage FET in series with a clamp capacitor. Therefore, migrating PCF to ACF, as in Figure 1(a), mainly introduces one more switch and an additional high-side driver to be equipped with soft switching capability. On the other hand, migrating PCF to the three-level LLC, as in Figure 1(b), requires three additional primary high-side switches and three high-side drivers to generate the desired PWM pattern, which significantly increases the BOM cost.

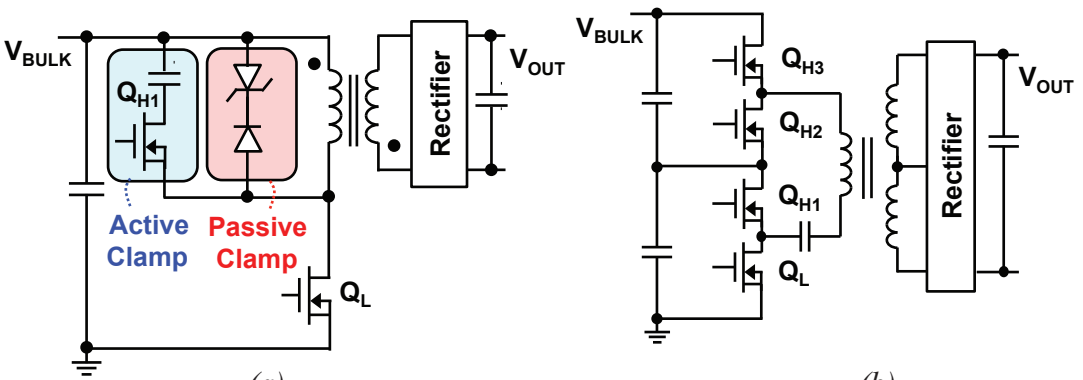


Figure 1 – Topology comparison: (a) PCF and ACF and (b) three-level LLC.

Figure 2 compares the efficiency of a 65 W output across a wide AC input voltage range, including the output cable loss. From a full-load efficiency perspective, ACF can provide close to 2% higher efficiency than PCF. Although three-level LLC provides even higher efficiency than ACF, the BOM cost is not easily justified for the cost-sensitive adapter market.

Product	Topology	Power Density	$f_{SW(min)}$ (kHz)	Primary Switch	High-Side Driver
A	PCF	11W/in^3	150	1 pcs	0 pcs
B	ACF	14W/in^3	120	2 pcs	1 pcs
C	Three-level LLC	17W/in^3	300	4 pcs	3 pcs

Table 1 – Comparison of three 65 W notebook adapter designs.

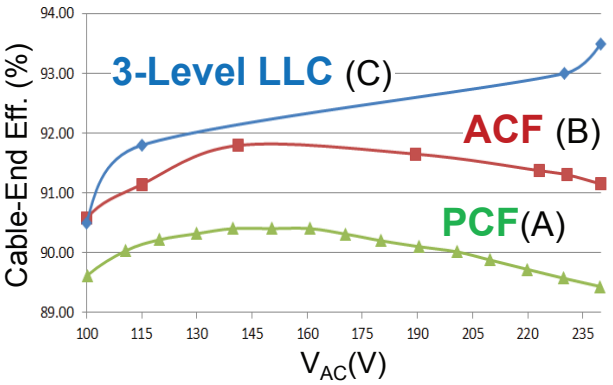


Figure 2 – Cable-end efficiency comparison of three topologies in high frequency operation.

A. Review of DCM Flyback with Passive Clamp

As shown in Figure 3(a), after the low-side switch (Q_L) turns off, high di/dt current flows through the leakage inductance of the transformer (L_k) and creates a high voltage stress on Q_L, so the L_k energy needs to be dissipated on a passive clamp circuit to prevent the voltage stress from damaging Q_L. From the loss Equation (1), the closer the clamp voltage of TVS (V_{CLAMP}) is to the reflected voltage (NV_{OUT}), the higher the clamping loss (P_{CLAMP}). It also shows P_{CLAMP} proportionally increases with f_{SW}, which becomes one of the hurdles for high frequency design when the peak magnetizing current ($I_{m(+)}$) is held constant. After the magnetizing current (I_m) is demagnetized to 0 A, the flyback converter operates in discontinuous conduction mode (DCM), so the magnetizing inductance (L_m) and the switch-node capacitance (C_{SW}) start to resonant and the DCM ringing dies out gradually. Since Q_L still turns on at a high voltage across the bulk input capacitor (V_{BULK}) for the next cycle, an additional turn-on switching loss ($P_{SW(DCM)}$) is created on Q_L. The $P_{SW(DCM)}$ expression in Equation (2) is also proportional to f_{SW}, which becomes another hurdle for high f_{SW} design. Figure 4 quantifies the percentage of the two losses respective to the full power on a 30 W adapter design. Even though both losses only contribute 2% at 100 kHz switching, they will contribute more than 5% each at 300 kHz switching, which becomes the dominate loss of the DCM flyback converter.

$$P_{CLAMP} = \frac{V_{CLAMP}}{V_{CLAMP} - NV_{OUT}} \frac{1}{2} L_k I_{m(+)}{}^2 f_{SW} \quad (1)$$

$$P_{SW(DCM)} \approx \frac{1}{2} C_{SW} V_{BULK}{}^2 f_{SW} \quad (2)$$

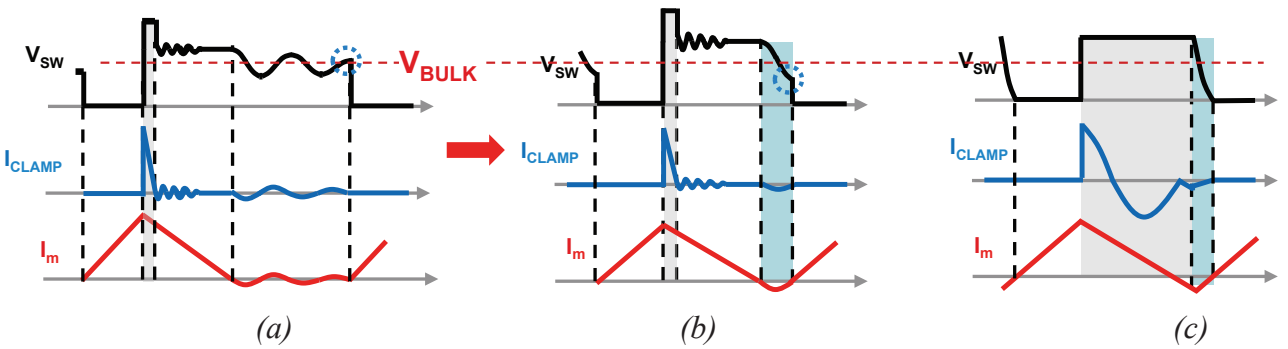


Figure 3 – Waveform comparison: (a) passive clamp + DCM, (b) passive clamp + TM and (c) active clamp + TM.

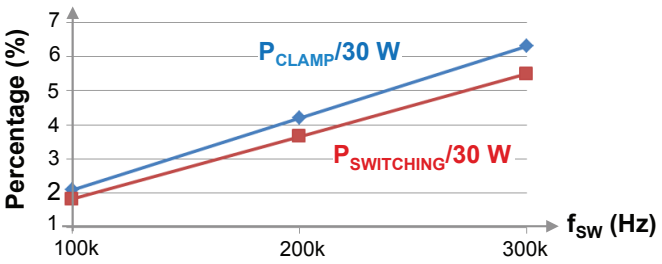


Figure 4 – Clamping loss and switching loss contributions to a 30 W adapter.

B. Review of Transition Mode (TM) Flyback with Passive Clamp

To lower the P_{SW} of Q_L in DCM operation, TM operation turns on Q_L at the first valley of the DCM ringing, as shown in Figure 3(b). Compared with DCM, the switching loss becomes lower, since the turn-on point is lower than the DCM operation. Additionally, the core loss and winding loss of the transformer become lower. The reason behind this lower core loss is that TM requires less peak magnetizing current ($I_{m(+)}$) than DCM to operate at the same f_{SW} and results in lower flux density. The TM winding loss is less because the di/dt of I_m is smaller than DCM and results in lower AC winding resistance [10]. However, the first disadvantage of TM operation is the inability to decay V_{SW} to 0 V. The lowest first valley point is close to $V_{BULK} - NV_{OUT}$, so the switching loss ($P_{SW(TM)}$) in Equation (3) indicates a substantial turn-on loss at a high input voltage condition still exists. The second issue is the clamping loss cannot be eliminated.

$$P_{SW(TM)} \approx \frac{1}{2} C_{SW} (V_{BULK} - NV_{OUT})^2 f_{SW} \quad (3)$$

C. Review of Transition Mode Flyback with Active Clamp

To fully remove the switching and clamping losses, an active-clamp circuit can be used in TM operation, as shown in Figure 3(c). The circuit includes a high-side switch (Q_H) in series with a resonant clamp capacitor (C_{CLAMP}) as in Figure 1(a). During the demagnetizing time of L_m and the on-state of Q_H, C_{CLAMP} resonates with L_k to recycle the L_k energy to the output, so the clamp loss can be eliminated. If Q_H keeps its on-state after the resonance is finished, I_m is further changed in the reverse direction. After Q_H turns off, the negative magnetizing current ($I_{m(-)}$) discharges C_{SW} to bring V_{SW} down to 0 V before turning on Q_L, so the switching loss can also be eliminated. However, the additional negative current enlarges the flux density, so the core loss is higher than TM. Also, the resonance current is a part of the current flowing through the primary and secondary windings of the transformer, so total winding loss is also higher than TM. Therefore, it is possible that negative current that is too large can wash out the efficiency benefit of ACF, if C_{SW} is too large. Table 2 summarizes the loss distributions and trade-off of the three flyback topologies.

II. Operation of Active Clamp Flyback

Figure 5 explains the operation of ACF in detail by dividing the switching waveforms into seven regions and Figure 6 shows the equivalent circuit for each region. In the first region (I), Q_L is in the on-state, as $V_{GS(QL)}$ is high, so V_{BULK} connecting to L_m causes I_m to linearly increase, where L_m stores energy. In the second region (II) where both Q_L and Q_H are off, the peak magnetizing current charges the junction capacitance of Q_L ($C_{OSS(QL)}$), discharges the junction capacitance of the clamp switch, Q_H, ($C_{OSS(QH)}$) and discharges the junction capacitance of the secondary rectifier at the same time. Therefore, the current on Q_L (I_{QL}) decreases, the clamp current (I_{CLAMP}) increases and the secondary rectifier current (I_{SEC}) increases with V_{SW} rising from 0 V to a high level. In the third region (III), Q_H has not turned on yet,

Operation	CLAMP	P_{CLAMP}	$P_{SWITCHING}$	P_{CORE}	$P_{WINDING}$
DCM	Passive	High	Higher	Higher	Middle
TM	Passive	High	Middle	Lower	Lower
TM	Active	**≈0 (to output)**	**≈0 (ZVS)**	**Middle**	**Higher**

Table 2 – Loss comparison of three flyback topologies.

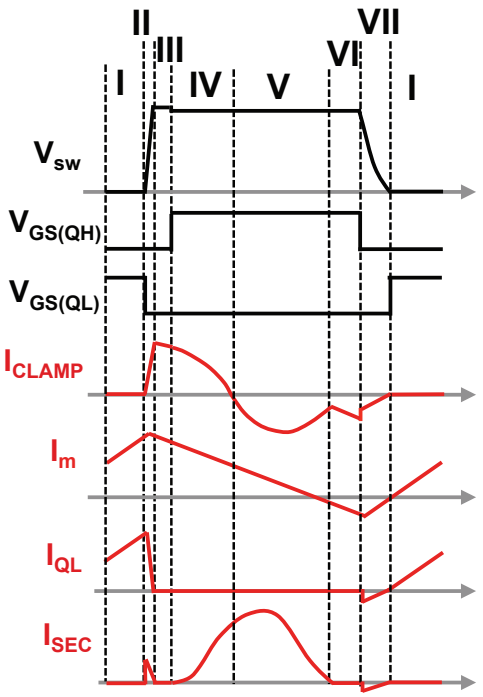


Figure 5 – Switching waveforms of ACF.

so I_m flows through the body diode of Q_H to charge C_{CLAMP} first. In the fourth region (IV), when Q_H is conducted as $V_{GS(QH)}$ is high, NV_{OUT} starts to demagnetize L_m, so I_m starts to decay and L_m releases its energy to the output. At the same time, C_{CLAMP} absorbs the L_k energy by resonating with L_k, so I_{CLAMP} is in the positive direction. In the fifth region (V), I_{CLAMP} starts resonating in the reverse direction, so I_{SEC} becomes higher, which indicates both magnetizing and leakage energy are being released to the output. The sixth region (VI) occurs after the resonance is completed. The secondary diode rectifier turns off naturally at zero current (ZCS), so NV_{OUT} cannot further demagnetize L_m. Instead, the clamp capacitor voltage (V_{CLAMP}) takes over to continue to demagnetize L_m as Q_H keeps conducting, so I_m keeps going in the reverse direction before Q_H turns off. In the last region where Q_H turns off, the negative magnetizing current, $I_{m(-)}$, starts to discharge $C_{OSS(QL)}$, charge $C_{OSS(QH)}$ and charge the junction capacitance of the secondary rectifier, so V_{SW} falls from a high level to 0 V. Finally, back to the first region, Q_L turns on as V_{SW} reaches 0 V, so ZVS is obtained. From the energy balance concept, Equation (4) highlights that the energy stored on L_m with $I_{m(-)}$ should be at least larger than the energy stored in the lumped capacitance (C_{SW}), so as to complete ZVS.

$$\frac{1}{2}L_m I_{m(-)}^{\ 2} \geq \frac{1}{2}C_{SW}V_{SW}^{\ 2} \tag{4}$$

Equation (4) also indicates that larger C_{SW} requires higher $I_{m(-)}$ for ZVS. It is well-known that a GaN FET has much less junction capacitance than a silicon MOSFET. For example, for the similar channel on-resistance ($R_{DS(ON)}$) ranging from 500 mΩ to 600 mΩ, GaN has almost three times less time-related capacitance than silicon (Si). This benefit results in lower peak-to-peak I_m ($I_{m(PK-PK)}$) for less core loss, lower RMS I_{PRI} ($I_{PRI(RMS)}$) for less winding loss and lower RMS I_{CLAMP} ($I_{CLAMP(RMS)}$) for less conduction loss on Q_H. Figure 7 compares the switching current waveforms of ACF and the difference of RMS current for the two state-of-the-art GaN and Si FETs with similar $R_{DS(ON)}$, when a Schottky diode is used as the secondary rectifier. The result shows that GaN enables more than a 22% reduction in $I_{m(PK-PK)}$ and $I_{PRI(RMS)}$, compared with Si FET. Moreover, the performance gap between silicon and GaN for ACF is not just a different magnitude of C_{OSS}, but also the capacitance nonlinearity is significantly different, as shown in Figure 8. For GaN FETs, for example, the capacitance difference of the drain-to-source voltage (V_{DS}) between 20 V and 400 V is not dramatic. Also, when $R_{DS(ON)}$ reduces, the capacitance is proportionally increased. On the other hand, for silicon FET, the capacitance becomes significantly larger as V_{DS} < 20 V. Compared with V_{DS} at 400 V, the capacitance at 20 V is almost 100 times larger for $R_{DS(ON)}$ = 680 mΩ. Furthermore, as the $R_{DS(ON)}$ reduces to 180 mΩ, the value at 20 V is almost 300 times larger. Therefore, it is important to understand how different levels of capacitance nonlinearity between GaN and silicon FETs impact the ACF performance and how to minimize the impact to reduce the efficiency gap between the two distinct devices.

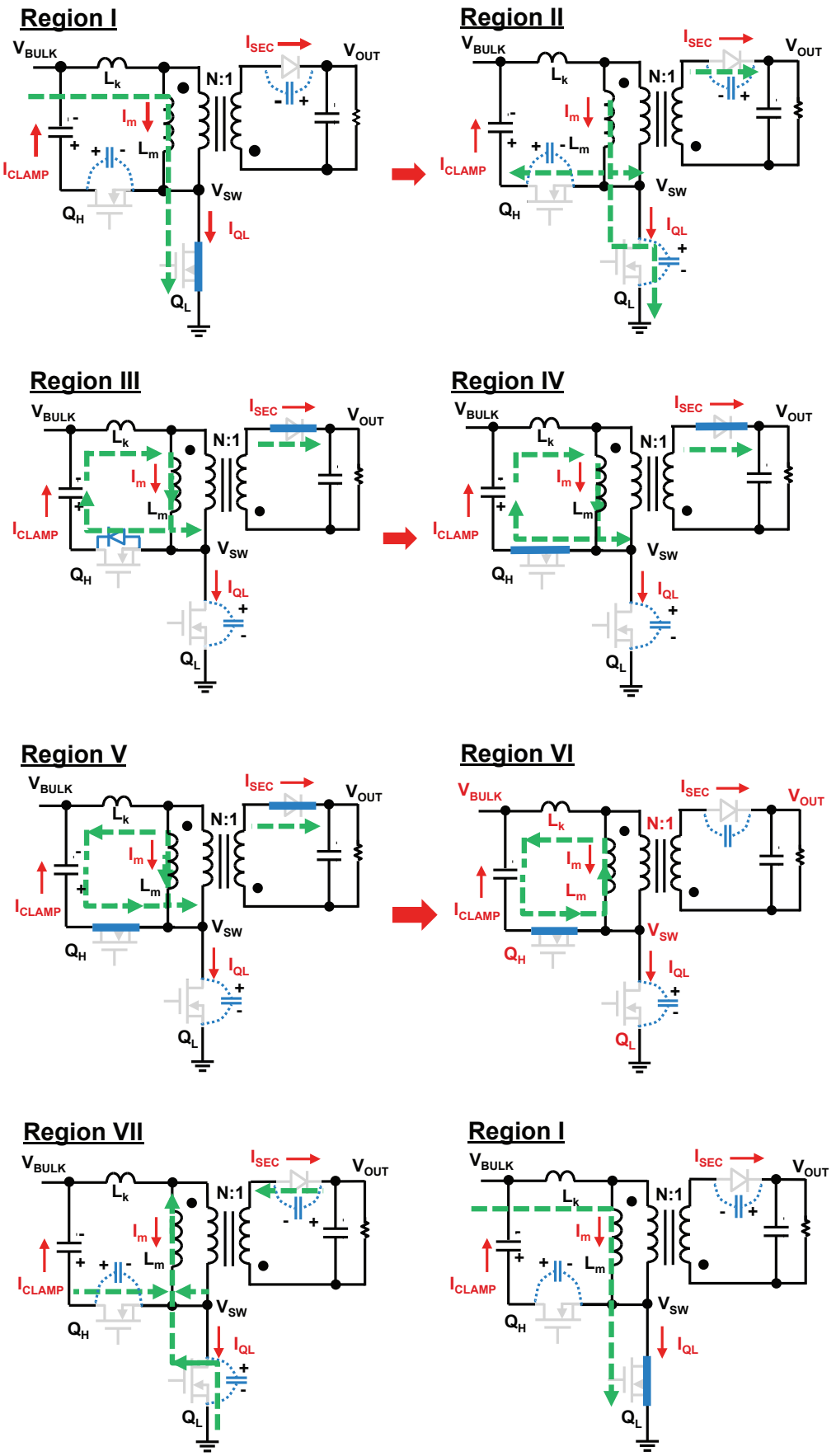
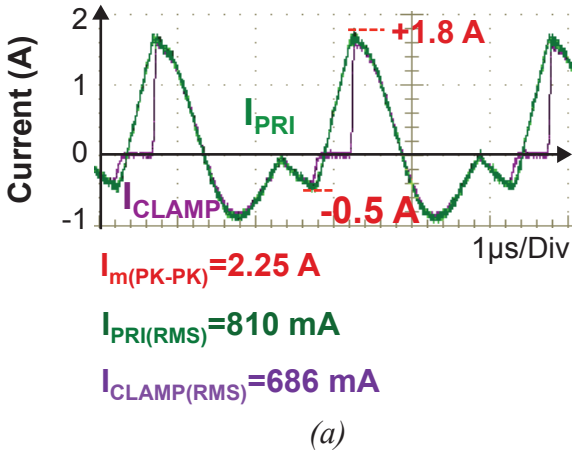
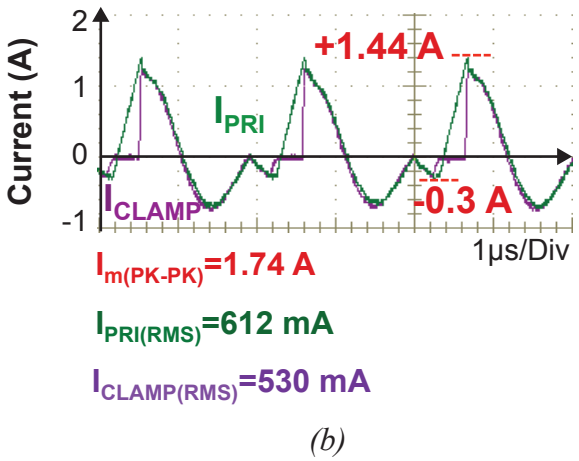


Figure 6 – Equivalent circuit of ACF operation in different switching states.



(a)



(b)

Figure 7 – Comparison of primary current waveforms: (a) Si-based ACF and (b) GaN-based ACF.

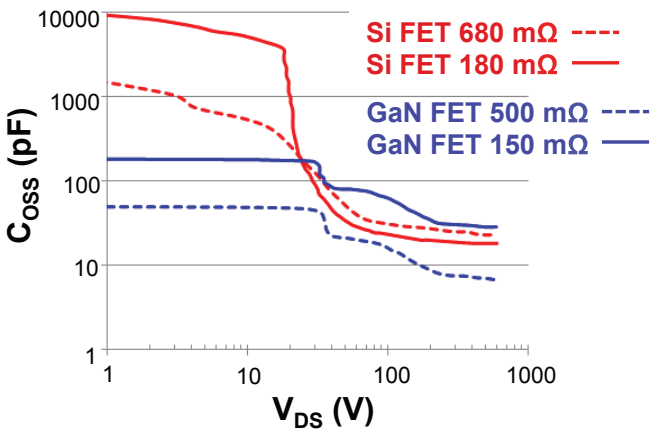


Figure 8 – Comparison of C_{OSS} curve between GaN FET and Si FET with different $R_{DS(ON)}$.

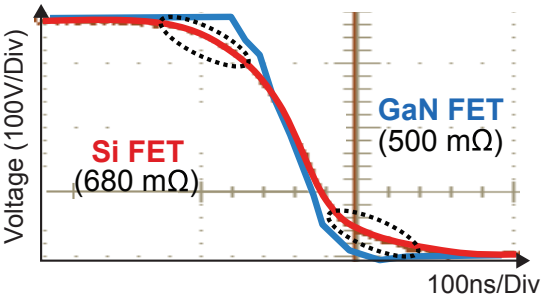


Figure 9 – Comparison of V_{SW} falling edge between GaN FET and Si FET.

III. Nonlinearity Impact of Device Capacitance And Solution

A. Impact on ZVS Voltage Transition

When V_{SW} decays from a high to low level by discharging C_{SW} with $I_{m(-)}$, the falling slope of V_{SW} can be greatly affected by the capacitance nonlinearity, as shown in Figure 9 above. For a GaN FET, C_{OSS} is less nonlinear, so the V_{SW} transition is close to a first-order reduction. For a silicon FET, three different falling slopes are observed on the V_{SW} waveform which exhibits a shallow slope at the beginning, becomes a sharper edge and then returns to a shallow slope at the end. The upper flat region is mainly from the high capacitance region of Q_H C_{OSS} curve and partly from the junction capacitance of the output rectifier, while the lower flat region comes mainly from the high capacitance region of the Q_L C_{OSS} curve. The first system impact is because the silicon FET requires a dead time three times longer for the voltage transition than GaN and the resulting duty-cycle loss limits higher f_{SW} operation. The second impact is that more $I_{m(-)}$ is needed to overcome the two high capacitance regions.

Firstly, it is found that proper C_{CLAMP} selection helps to reduce the impact of the upper flat area on V_{SW}. Figure 10(a) shows an example of a silicon-based ACF with a smaller C_{CLAMP} design of 100 nF which makes the resonance clamp current finish before Q_H turns off. In this case, $I_{m(-)}$ is the only current source to discharge the high capacitance region of Q_H. On the other hand, if C_{CLAMP} can be increased to a point, 600 nF for example, that the resonance cannot be completed at the end of the

Q_H off-time, the negative clamp current ($I_{CLAMP(-)}$) becomes an extra current source to discharge the high capacitance region of the Q_H C_{OSS} curve, in addition to $I_{m(-)}$. With that, not only the time spent on the upper flat area is shortened, but also $I_{m(-)}$ is reduced, from -0.9 A to -0.8 A in this case. The energy-balance Equation (5) is another perspective to understand this effect, where the ZVS criteria contains not only a part of the L_m energy from $I_{m(-)}$, but also a part of the L_k energy from $I_{CLAMP(-)}$.

$$\frac{1}{2}L_m I_{m(-)}^{\ 2}+\frac{1}{2}L_k I_{CLAMP(-)}^{\ 2}\geq\frac{1}{2}C_{SW}V_{DS}^{\ 2} \qquad (5)$$

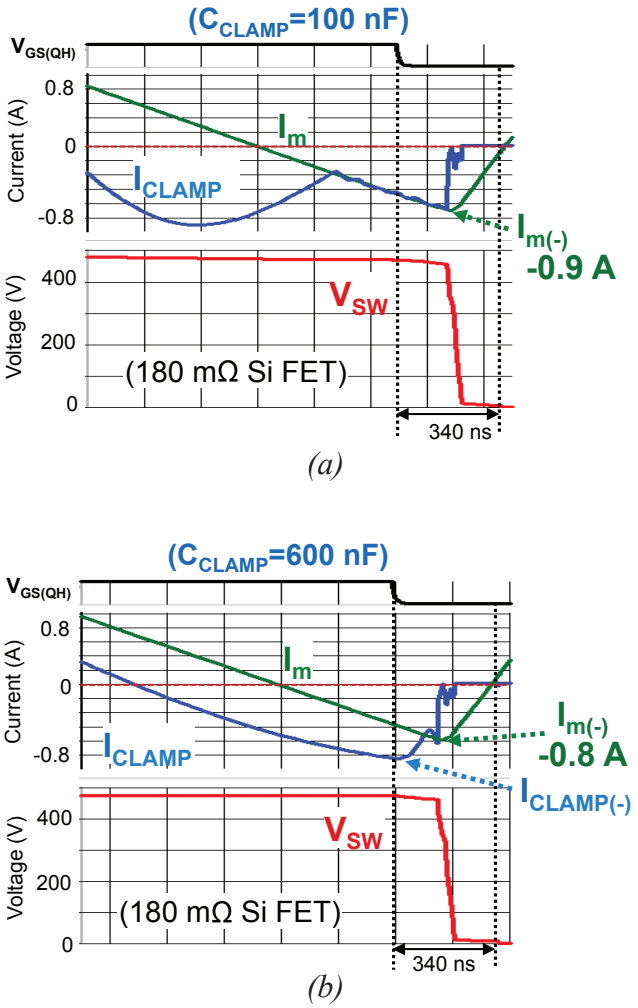


Figure 10 – C_{CLAMP} effect on switching waveforms: (a) C_{CLAMP}=100 nF and (b) C_{CLAMP} =600 nF.

Secondly, it is found that proper Q_L turn-on point selection helps reduce the impact of the lower flat area on V_{SW}. As the C_{OSS} curve of the silicon FET in Figure 8 indicates, if the ZVS target is to turn on Q_L by waiting for V_{SW} to reach to 0 V, large $I_{m(-)}$ is required to discharge the high capacitance region. If it is possible to turn on Q_L at a given V_{SW} before C_{OSS} starts to grow rapidly, $I_{m(-)}$ can be significantly reduced. This technique is referred to as partial ZVS in this paper. As the partial ZVS point is chosen at 20 V for this example, there is a 14% reduction on both RMS primary current for less winding loss and peak-to-peak magnetizing current for less core loss, as shown in Figure 11. The efficiency data in Figure 12(a) demonstrates that performing partial ZVS at 20 V further improves the full-load efficiency 0.5%. Figure 12(b) shows a more detailed study on where the optimal partial ZVS target is for a silicon FET with 680 mΩ. From the total loss reduction with respect to the ZVS point moving from 0 V to 60 V, the result indicates that 20 V obtains the biggest loss reduction, but loss reduction has diminishing returns when the partial ZVS point is higher than 20 V. This effect can be understood from the design trade-off between the RMS current reduction and switching loss increase, as shown in Figure 13. As the partial ZVS point moves higher, $I_{PRI(RMS)}$ continues to reduce. However, a partial ZVS point means a hard switching point of Q_L, so the turn-on switching loss grows at the same time. Since the turn-on loss of the silicon FET can increase rapidly after 10 V, the conduction loss reduction will be gradually washed out by the switching loss increasing. Therefore, this indicates 10 ~ 20 V is suitable for a silicon FET when the turn-on loss grows rapidly above the voltage range, while full ZVS is best for GaN FET.

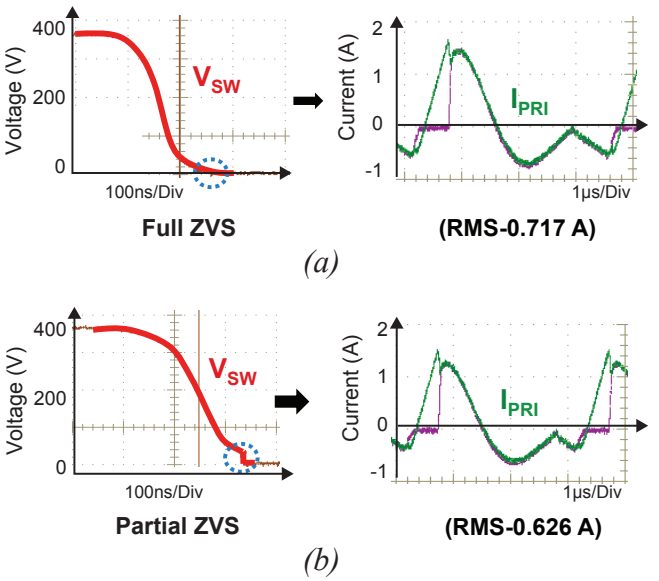


Figure 11 – Impact of ZVS target on switching waveforms: (a) full ZVS and (b) partial ZVS at 20 V.

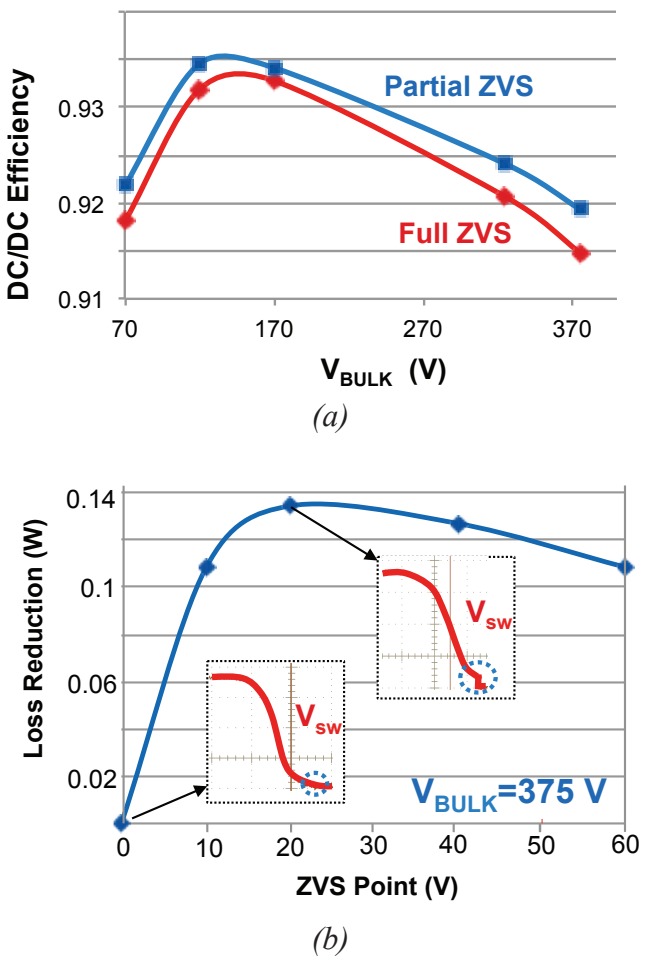


Figure 12 – Improvement of partial ZVS to: (a) full-load efficiency and (b) power loss reduction.

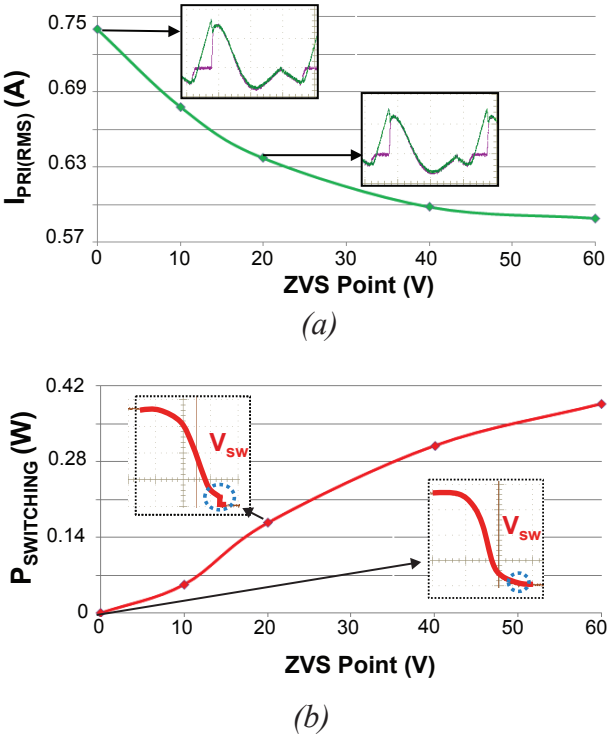


Figure 13 – Design trade-off of partial ZVS: (a) primary RMS current and (b) turn-on switching loss of Q_L.

B. Impact on Resonance Clamp Current

C_{SW} has contributions not only from the C_{OSS} of the two primary switches, but also from the junction capacitance of the secondary rectifier, either a Schottky diode or a synchronous rectifier (SR). Table 3 compares the switching current waveforms with the combination of different primary switches and different secondary-rectification devices. When a diode is used as the rectifier, the shape of the switching current waveform between a GaN and silicon FET is similar, and the main difference is just the different peak-to-peak and RMS current levels. On the other hand, when SR is used as the secondary rectifier, the shape of the current waveform becomes significantly different. When using silicon FETs as the two primary switches, there is only a small current dip on I_{PRI} before the resonance of I_{CLAMP} starts, as a SR is used. The RMS current difference between using a Schottky diode and SR is not much, since the current dip effect on the RMS current is almost negligible. When using GaN FETs as the two primary switches and silicon SR as the rectifier, a big current dip reduces the initial

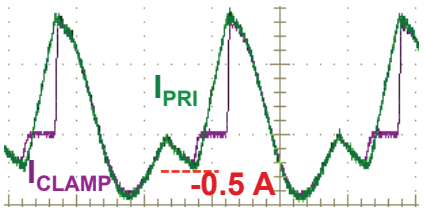
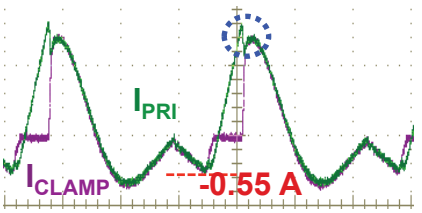
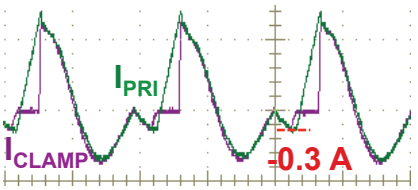
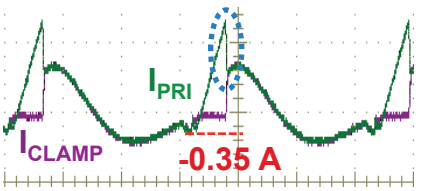
Primary Switch	Secondary Rectifier	
	Schottky Diode	**Sync. Rectifier (SR)**
Silicon FET (650 mΩ)	 **$I_{CLAMP(RMS)}$=686 mA**	 **$I_{CLAMP(RMS)}$=600 mA**
GaN FET (500 mΩ)	 **$I_{CLAMP(RMS)}$=530 mA**	 **$I_{CLAMP(RMS)}$=349 mA**

Table 3 – Switching waveform comparison with different types of secondary rectifiers.

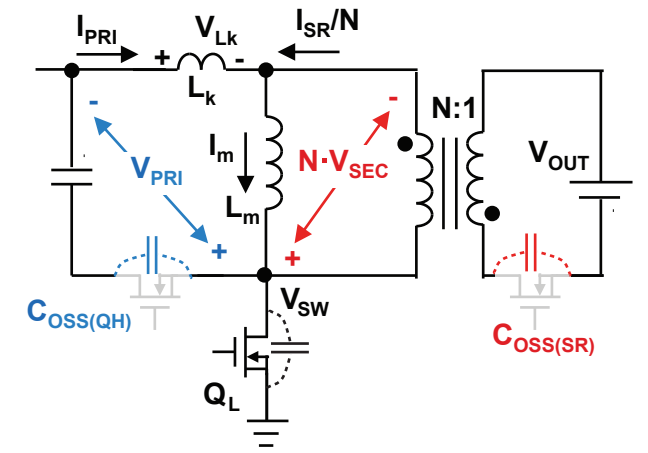
resonance current of I_{CLAMP}, which significantly lowers the RMS current compared with using a Schottky diode. In this example, 34% reduction in the RMS current with this current dipping effect benefits the winding loss reduction as well as conduction loss reduction of Q_H.

According to Faraday's law in Equation (6), the current dip phenomenon on the primary current, i.e. a di/dt current change on I_{PRI}, can be understood by examining the voltage change across the L_k inductance, which is the voltage difference between the reflected voltage from the secondary winding (NV_{SEC}) and the voltage across the transformer primary winding (V_{PRI}), as shown in the equivalent circuit of Figure 14(a).

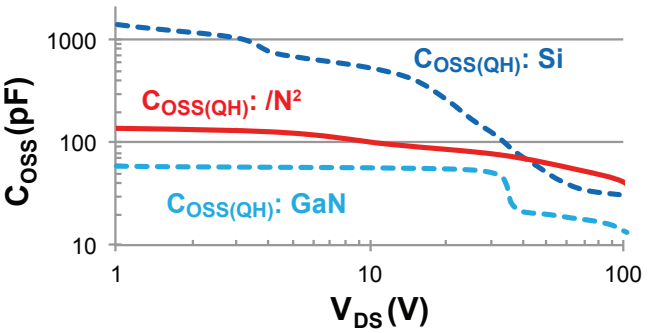
$$\frac{dI_{PRI}}{dt} = \frac{1}{L_k}(NV_{SEC} - V_{PRI}) \quad (6)$$

The negligible current dipping for silicon-based ACF with SR is explained as follows. Since the SR is off as the current dipping occurs, NV_{SEC} is equal to the voltage difference between the drain-to-source voltage on the SR FET and V_{OUT}. Similarly, since Q_H is off as well, V_{PRI} is equal to the voltage difference between the drain-to-source voltage of Q_H and V_{CLAMP}. Since both sides use silicon FET, the C_{OSS} changes significantly as V_{DS} varies. Figure 14(b) compares the capacitance nonlinearity between $C_{OSS(QH)}$ and the junction capacitance of SR ($C_{OSS(SR)}$) reflected to the primary side. The result shows that there is a certain higher V_{DS} range where $C_{OSS(QH)}$ is smaller than the reflected capacitance from SR ($C_{OSS(SR)}/N^2$) and there is another lower V_{DS} range where $C_{OSS(QH)}$ is significantly larger than $C_{OSS(SR)}/N^2$. When peak I_m ($I_{m(+)}$) starts to discharge both, this capacitance difference creates different rising slopes on V_{PRI} and NV_{SEC}, as the simulation result shows in Figure 15(a). In the first portion of the figure, V_{PRI} rises faster than NV_{SEC}, since $C_{OSS(QH)}$ is smaller. In the second portion, V_{PRI} rises much slower than NV_{SEC}, since $C_{OSS(QH)}$ becomes larger. The rising slope variation causes a different voltage polarity across L_k in Equation (6). In the first portion, the voltage across L_k is negative, so the dI_{PRI}/dt is negative. In the second portion, the voltage across L_k becomes positive, so the dI_{PRI}/dt becomes positive. This explains why a current dip occurs at the beginning and disappears afterward in Figure 15(a). Losing the current dipping effect, the initial

resonance current is almost equal to $I_{m(+)}$. Then, the benefit of SR for silicon-based ACF is mainly the reduction of the conduction loss on the secondary rectifier.



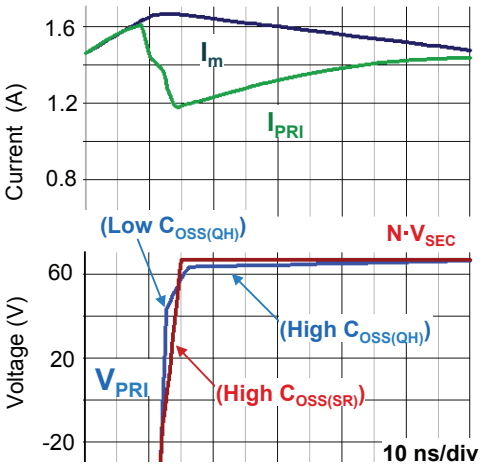
(a)



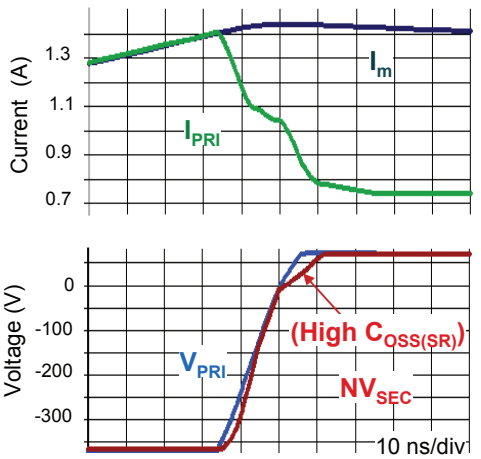
(b)

Figure 14 – Cause of current dipping: (a) voltage difference on primary and secondary and (b) C_{OSS} difference.

For a GaN FET, the current dip effect is more significant, which reduces the initial resonance clamp current. This effect is also explained by the C_{OSS} difference in Figure 14(b), which shows that $C_{OSS(QH)}$ of GaN is always smaller than $C_{OSS(SR)}/N^2$ across all V_{DS} ranges. Therefore, as $I_{m(+)}$ starts to discharge both capacitances, the rising slope of V_{PRI} is always higher than NV_{SEC}. With this, the voltage polarity across L_k in Equation (6) stays negative, which forces dI_{PRI}/dt to also stay negative before resonance starts. In this case, SR for GaN-based ACF does not just reduce the conduction loss on the secondary side, but also benefits the conduction loss reduction on both Q_H and the primary winding of the transformer. Simply speaking, a win-win situation is obtained for both the primary and secondary sides. The efficiency measurement in Figure 16 indicates a 2.5% improvement across a wide line range, as a diode rectifier is replaced by a SR with $R_{DS(ON)}$ = 28 mΩ. This efficiency boost cannot be seen in silicon-based ACF with SR, since the current dipping effect is lost by the high capacitance region of Q_H. However, lower $R_{DS(ON)}$ does not mean more efficiency improvement for a GaN-based ACF topology. The efficiency test result using a 14 mΩ SR is almost the same as using 28 mΩ, so it means that the $R_{DS(ON)}$ benefit is washed out by other additional losses. First, lower $R_{DS(ON)}$ creates higher capacitive loading, so the higher peak-to-peak magnetizing current increases the core loss. Secondly, the lower $R_{DS(ON)}$ FET with a larger gate charge (Q_G) increases the gate driving loss.



(a)



(b)

Figure 15 – Current dipping effect with SR: (a) Si-based ACF and (b) GaN-based ACF.

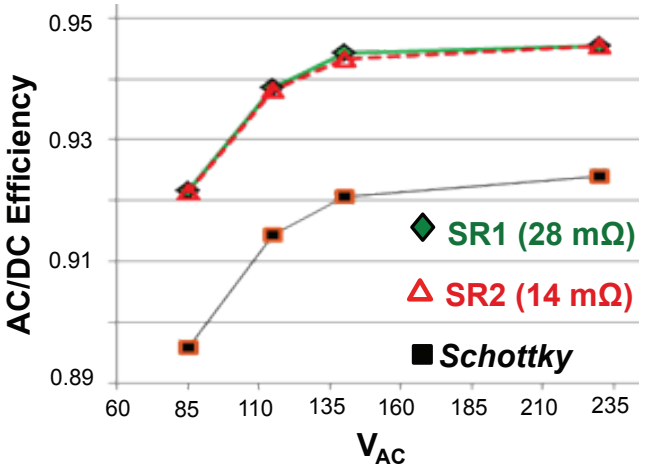


Figure 16 – Impact of current dipping of GaN-based ACF on full-load efficiency.

C. Impact on Light Load Efficiency

The light load efficiency of ACF is also very sensitive to C_{OSS} nonlinearity. As the load current becomes lighter, the conventional peak current-mode control reduces the positive peak current ($I_{m(+)}$) to regulate the output power, while the negative magnetizing current ($I_{m(-)}$) stays the same in the same V_{BULK} condition. $I_{m(+)}$ delivers active energy to the output, while $I_{m(-)}$ stores the circulating energy to achieve ZVS. If $I_{m(+)}$ and $I_{m(-)}$ become more and more comparable as the load becomes lighter, it means that the transformer efficiency becomes worse, since the contribution of the circulating energy is getting higher. For silicon-based ACF with highly nonlinear C_{OSS}, $I_{m(-)}$ is larger, especially at high line, so the impact at a light load becomes more significant and the efficiency deteriorates very quickly. The measurement result in Figure 17(a) shows that the efficiency difference between 50% load and 25% can be as high as 7.3%. On the other hand, for GaN-based ACF, $I_{m(-)}$ is much lower than silicon-based ACF due to its low C_{OSS}. As the load becomes lighter, the $I_{m(-)}$ impact is less severe, so it results in only 2.6% efficiency difference between a 50% load and 25% load. Therefore, it is important to understand what kind of light load mode operation is most suitable for ACF to maintain good efficiency. Conceptually, the most critical requirement of an ideal light load mode for ACF is to maintain $I_{m(+)}$ relatively higher than $I_{m(-)}$. Then, the question is how to maintain regulation of the output voltage if a certain $I_{m(+)}$-to-$I_{m(-)}$ ratio would like to be maintained.

Therefore, burst mode control is proposed in this paper to meet this goal, the PWM pattern of which is shown in Figure 18. $V_{GS(QL)}$ is set as the first pulse to build up the bootstrap voltage of the high-side driver first before Q_H starts switching, and the second $V_{GS(QL)}$ pulse turns on Q_L close to valley switching. The following pulses operate in ZVS condition, since $V_{GS(QH)}$ is enabled. Furthermore, $V_{GS(QH)}$ of the last pulse is purposely disabled to prevent generating unnecessary $I_{m(-)}$ to trigger a large DCM resonance between L_m and C_{SW}, since the excessive ringing can create additional core loss. The output power regulation is based on modulating the burst off-time, as the energy per switching cycle in a burst packet is fixed, i.e. $I_{m(+)}$ is fixed and is chosen at a certain current level which provides a reasonable $I_{m(+)}$-to-$I_{m(-)}$ ratio. After the last pulse per burst packet ends, $V_{GS(QL)}$ and $V_{GS(QH)}$ are completely turned off to terminate the power delivery. As the load becomes lighter, the burst off-time becomes longer before the next burst event.

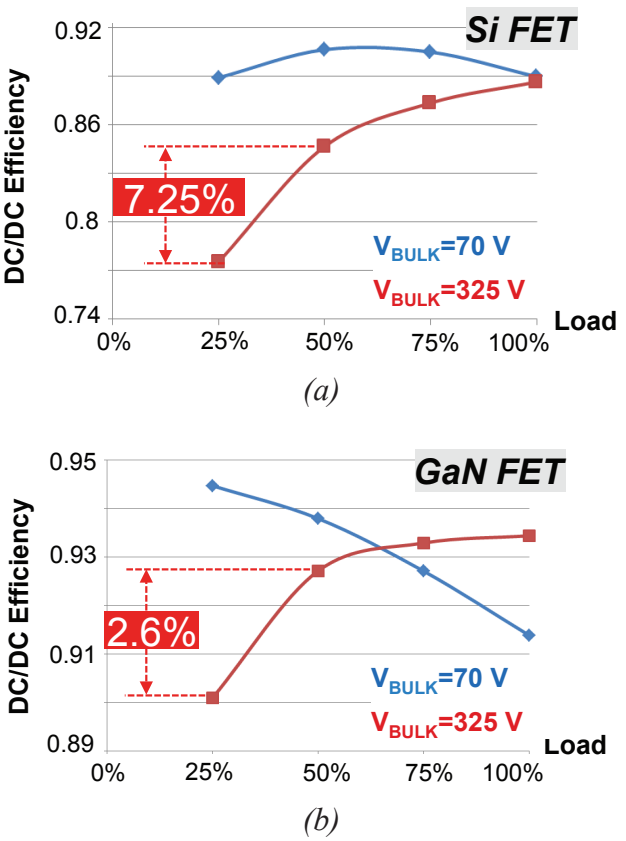


Figure 17 – Light load efficiency of 30 W ACF with diode rectifier: (a) Silicon and (b) GaN.

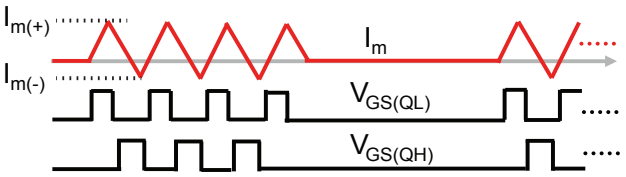


Figure 18 – Proposed burst mode operation for ACF.

Since the proposed burst control is able to keep a high $I_{m(+)}$-to-$I_{m(-)}$ ratio, the light load efficiency can be significantly improved. From the test result under V_{BULK} = 200 V shown in Figure 19(b), there is 2.4% efficiency improvement at a 25% load with the proposed burst control, compared with conventional peak current control. An additional benefit is limiting the f_{SW} variation in peak current control. By the nature of TM operation, as $I_{m(+)}$ reduces with a lighter load, f_{SW} grows higher and higher. The f_{SW} variation in Figure 19(a) shows that as a 100% load is switched at 330 kHz, a 25% load is switched at 600 kHz. This not only brings a challenge for MOSFET driving, but also increases other switching-related losses. As burst mode is applied at a 50% load, the fixed $I_{m(+)}$ limits f_{SW} from changing.

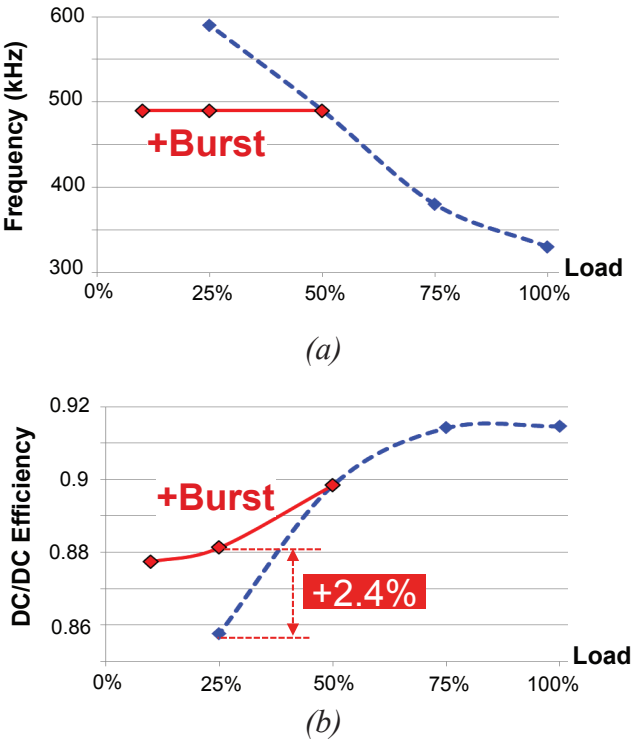


Figure 19 – Benefit of burst mode for silicon-based ACF: (a) f_{SW} change and (b) light load efficiency.

The number of pulses per packet is defined as N_{SW}. The test result in Figure 20(a) shows that as N_{SW} increases (more grouped pulses), the efficiency becomes higher. However, more grouped pulses mean higher output ripple (ΔV_{OUT}) as shown in Figure 20(b). Besides, higher N_{SW} makes the burst frequency (f_{BUR}) enter the audible noise range at heavier loads, so Equation (7) is derived to estimate how f_{BUR} varies with the output load and N_{SW}. This equation contains a ratio of I_{OUT} and $I_{OUT(BUR)}$. $I_{OUT(BUR)}$ is the predetermined output load condition starting at the burst and I_{OUT} is the lighter load condition lower than $I_{OUT(BUR)}$. For example, if the burst starts at a 50% load, operating at a 25% load results in a current ratio of 0.5. In other words, as the load becomes lighter, f_{BUR} will be lower. Another dependency of this equation is the N_{SW} and f_{SW} of each pulse. So, as N_{SW} is higher, f_{BUR} will be further reduced as well.

$$f_{BUR} = \frac{I_{OUT}}{I_{OUT(BUR)}} \frac{f_{SW}}{N_{SW}} \tag{7}$$

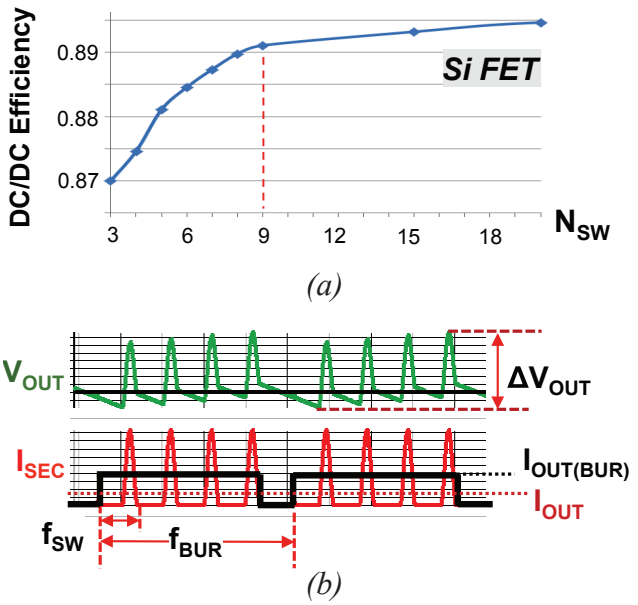


Figure 20 – Impact of N_{SW} determination for burst mode: (a) light load efficiency and (b) output ripple.

The complete control law over a wide load range is shown in Figure 21, which explains how the critical parameters are changed. At a heavier load, $I_{m(+)}$ is gradually reduced by a peak current

loop as the load decreases, so f_{SW} increases. This region is defined as AM operation (amplitude modulation). In AM, the burst mode has not started yet, so the burst frequency is 0 Hz. Further, lower $I_{m(+)}$ reduces ΔV_{OUT}, so the worst-case ΔV_{OUT} always occurs at a full load condition. After $I_{m(+)}$ is reduced to a predetermined peak current threshold ($I_{m(BUR)}$), the burst mode control starts to clamp $I_{m(+)}$ to this level, so f_{SW} is clamped at the same time. Then, f_{BUR} starts to move into a lower frequency range as I_{OUT} reduces. When more pulses are grouped, the control loop enters burst operation at heavier loading. It is possible that when f_{BUR} falls into the audible noise range (below 20 kHz), the transformer can generate disturbing noise. Additionally, ΔV_{OUT} increases with more grouped pulses. It is possible that if N_{SW} is not properly selected, the worst-case ΔV_{OUT} can occur at very light load conditions instead of full load conditions, which increases the output capacitor size needed to meet the output ripple requirement.

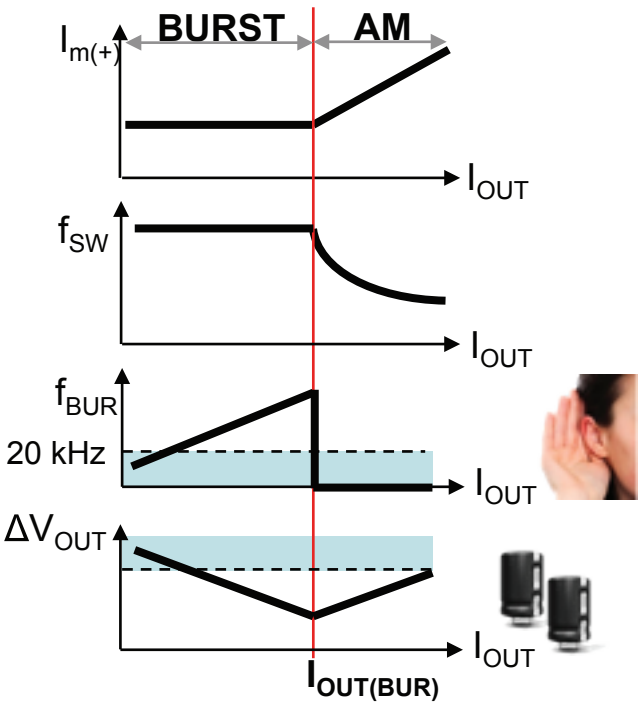


Figure 21 – Control law across wide load range with burst mode.

IV. Analysis And Design Procedure of an ACF Power Stage

A. Analytical Expression of ACF Operating Condition

First, the technique of triangular approximation is proposed to model the resonance current waveform of ACF in complementary switching around the V_{SW} transition, as shown in Figure 22(a). Then, the analytical expression of the switching frequency (f_{SW}) and input power (P_{IN}) can be easily derived from the triangular waveform. The input current of ACF is obtained by averaging the switching current waveform of the low-side switch (I_{QL}).

$$I_{IN} = \int_0^{1/f_{SW}} I_{QL}(t)\,dt = \frac{1}{2}[I_{m(+)}T_r + I_{m(-)}T_{m(-)}]f_{SW} \qquad (8)$$

where T_r is the rising time of I_m from 0 A to $I_{m(+)}$ and $T_{m(-)}$ is the transition time from $I_{m(-)}$ to 0 A. With the triangular approximation, T_r is substituted by $I_{m(+)}L_m/V_{BULK}$ and $T_{m(-)}$ is approximated by $I_{m(-)}L_m/V_{BULK}$. Next, the input power equation can be derived and simplified as

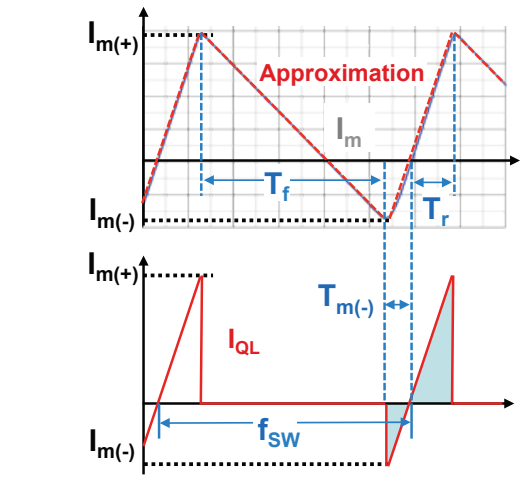
$$P_{IN} = V_{BULK} \cdot I_{IN} = \frac{1}{2}L_m f_{SW}[I_{m(+)}{}^2 - I_{m(-)}{}^2] \qquad (9)$$

Since this equation shows that $I_{m(+)}$ needs to be increased to provide the same power as more $I_{m(-)}$ is needed for ZVS, the physical meaning is that the ACF transformer stores $I_{m(+)}$ as active energy for power delivery, but $I_{m(-)}$ is like a reactive energy. After that, the f_{SW} expression in Equation (10) can be obtained based on the sum of T_r, $T_{m(-)}$ and the falling time from $I_{m(+)}$ to $I_{m(-)}$ (T_f), which is $(I_{m(+)}-I_{m(-)})L_m/V_{BULK}$.

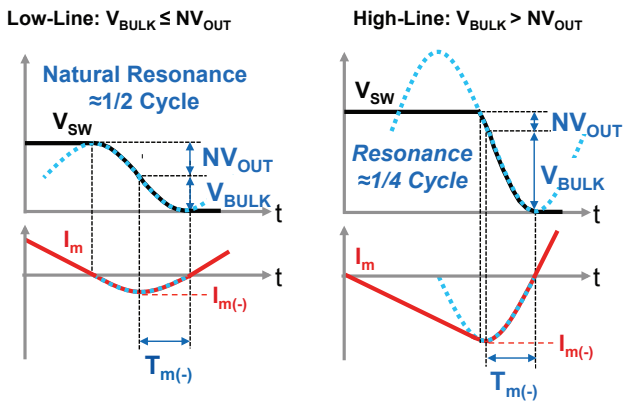
$$f_{SW} = \frac{1}{T_r + T_f + T_{m(-)}} = \frac{D^2 V_{BULK}}{2I_{IN}L_m - DI_{m(-)}L_m + DT_{m(-)}V_{BULK}} \qquad (10)$$

where D is not the duty-cycle of the Q_L on-time but comes from the volt-second balance of I_m. Then, D is defined as

$$D = \frac{T_r + T_{m(-)}}{T_r + T_{m(-)} + T_f} = \frac{NV_{OUT}}{V_{BULK} + NV_{OUT}} \qquad (11)$$



(a)



(b)

Figure 22 – Waveform approximation: (a) triangular approximation and (b) resonance during V_{SW} transition.

As long as the analytical expressions of $T_{m(-)}$ and $I_{m(-)}$ can be obtained, the above equations can be used to calculate the operating condition of ACF. For a LLC resonant converter as a double-ended topology, L_m can be treated as a constant current source while discharging $C_{SW,}$ so a first-order expression is used to express the V_{SW} transition time [11]. Applying this current-source concept to the L_m of an ACF, $T_{m(-)}$ may be simply equal to $C_{SW}V_{SW}/I_{m(-)}$. However, since the ACF as a single-ended topology only generates a small amount of $I_{m(-)}$ for ZVS and the state variable changes as C_{SW} discharges during the V_{SW} transition, the first-order approximation in LLC cannot be applied to ACF. Instead, L_m and C_{SW} have to be treated as a second-order tank circuit to obtain more accurate $T_{m(-)}$ and $I_{m(-)}$. Table 4 summarizes the proposed derivation results for the two parameters under a wide V_{BULK} range. Starting from the $V_{BULK} \le NV_{OUT}$ condition, Q_H can turn off at the zero-crossing of I_m since the voltage swing of the natural resonance between L_m and C_{SW} is enough to bring V_{SW} down to 0 V. Based on the waveforms shown in Figure 22(b), $I_{m(-)}$ can be derived based on the characteristic impedance (Z_n) and the resonance voltage amplitude of NV_{OUT}, while $T_{m(-)}$ is a quarter of the resonance period. In this condition, the overall V_{SW} transition takes half of the resonance period to complete. On the other hand, as $V_{BULK} > NV_{OUT}$, Q_H has to turn off later than the zero-crossing of I_m in order to create large enough $I_{m(-)}$. Then, as shown in Figure 22(b), the initial resonance current between L_m and C_{SW} is not zero, so the voltage swing does not start from the peak of the sinusoidal trajectory but starts close to a quarter of the resonant period. For this case, $I_{m(-)}$ can also be derived based on the characteristic impedance (Z_n) and the resonance voltage amplitude of V_{BULK}, while $T_{m(-)}$ is still a quarter of the resonance period.

	$V_{BULK} > NV_{OUT}$	$V_{BULK} \le NV_{OUT}$
$T_{m(-)}$	$T_{m(-)} = 0.5\pi\sqrt{L_m C_{SW}}$	$T_{m(-)} = 0.5\pi\sqrt{L_m C_{SW}}$
$I_{m(-)}$	$I_{m(-)} = -\frac{V_{BULK}}{Z_n} = -\sqrt{\frac{C_{SW}}{L_m}} V_{BULK}$	$I_{m(-)} = -\frac{NV_{OUT}}{Z_n} = -\sqrt{\frac{C_{SW}}{L_m}} NV_{OUT}$

Table 4 – Summary of $T_{m(-)}$ and $I_{m(-)}$ equations.

B. Analytical Expression of Switching Node Capacitance

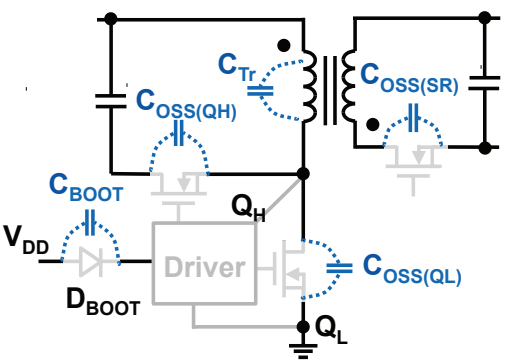
Lumped time-related capacitance (C_{SW}) includes all the passive and active components in ACF, as the equivalent circuit shows in Figure 23(a). C_{Tr} comes from the winding capacitance of the transformer and C_{BOOT} is the junction capacitance of the bootstrap diode, while the rest are contributed by the junction capacitance of both the primary and secondary switches. Conceptually, C_{SW} is expressed as the sum of all capacitors reflected to the primary side in Equation (12).

$$C_{SW} = C_{Tr} + C_{OSS(QL)} + C_{OSS(QH)} + C_{BOOT} + \frac{C_{OSS(SR)}}{N^2} \quad (12)$$

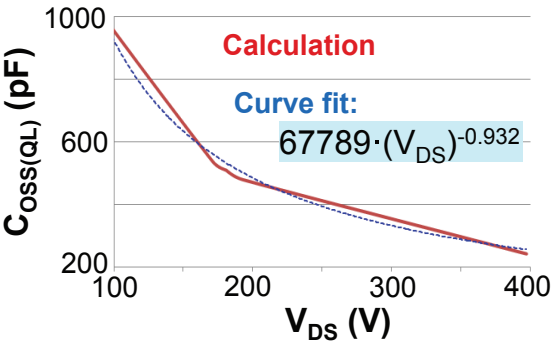
However, the first challenge of calculating C_{SW} is that the capacitance of the active switches is very nonlinear, as illustrated in Figure 8 and Figure 14(b). The second challenge is that the device datasheets do not provide enough data points for the equivalent time-related capacitance under different drain-to-source voltages. For example, a primary 600 V silicon super-junction FET only lists an equivalent time-related capacitance at 400 V, while the datasheet of a 150 V SR FET does not even list any. The third challenge is that as a partial ZVS technique is applied, the value on the datasheet has no meaning, since the value assumes a V_{SW} transition between 400 V to 0 V.

This section provides a general expression of time-related capacitance in Equation (13) and introduces the calculation process to obtain its analytical form under an arbitrary V_{DS} of each device. The assumption is that there is no hysteresis loss effect on the C_{OSS} curve in [12][13], such that the time-related capacitance can be directly calculated through the C_{OSS} curve on the datasheet. The first step is integrating the C_{OSS} curve in the datasheet from the partial ZVS point of V_{th} to a variable V_{DS}, which is V_{BULK}+NV_{OUT} for ACF. Specifically, the integration term is done by discretizing the C_{OSS} curve, calculating the area of each segment and then summing the areas together. A finer V_{DS} segment should be applied to the region with a large capacitance change on the C_{OSS} curve. The second step is dividing the integrated expression by the voltage difference between V_{DS} and V_{th}, so the time-related capacitance can be plotted as the brown-solid curve on Figure 23(b). The third step is curve fitting the numerical values into an analytical expression. The example general form is shown in Equation (13), which is a logarithmic trend-line equation with two variables, X and Y. The two variables can be easily calculated using the plotting tool in Excel software.

$$C_{OSS(QL)}(V_{DS}) = \frac{1}{V_{DS} - V_{th}} \int_{V_{th}}^{V_{DS}} C_{OSS}(V)\,dV \approx X \cdot {V_{DS}}^{Y} \quad (13)$$



(a)



(b)

Figure 23 – Lumped C_{SW} derivation: (a) C_{SW} breakdown of ACF and (b) time-related C_{OSS} of Q_L.

C. Design Procedure and Design Example

First, we must select the turn ratio (N) using four design criteria as a starting point.

(1) The maximum N (N_{max}) is limited by the derated maximum drain-to-source voltage of Q_L ($V_{DS(QL)\_MAX}$) or Q_H ($V_{DS(QH)\_MAX}$). ΔV_{CLAMP} is the difference between the maximum clamp voltage and the reflected output voltage. It can be due to either the ripple voltage of C_{CLAMP} as Q_H is active at heavier loads or the voltage overcharge of C_{CLAMP} by the L_k energy as Q_H is disabled at very light load.

(2) Minimum N (N_{MIN}) is limited by the derated maximum drain-to-source voltage of SR ($V_{DS(SR)\_MAX}$). ΔV_{SPIKE} should account for any additional voltage spike higher than $V_{BULK(MAX)}/N$, when Q_H is active and turns off at a non-zero current situation (ZCS) at heavier loads. When C_{CLAMP} is too large, the non-ZCS situation occurs, since the resonance current between L_k and C_{CLAMP} cannot force I_{SEC} to return to 0 A before Q_H turns off.

(3) The minimum D at $V_{BULK(MAX)}$ (D_{MIN}) introduces more core loss than the basic Steinmetz equation due to the triangular excitation [14], so this constraint creates another limitation on N_{MIN}.

(4) The winding loss distribution between the primary and secondary side of the transformer is the final design criteria. As N increases, the primary RMS current reduces, while the secondary RMS current increases [15][16].

$$N_{MAX} = \frac{V_{DS(QL)\_MAX} - V_{BULK(MAX)} - \Delta V_{CLAMP}}{V_{OUT}} \quad (14)$$

$$N_{MIN} = \frac{V_{BULK(MAX)}}{V_{DS(SR)\_MAX} - V_{OUT} - \Delta V_{SPIKE}} \quad (15)$$

$$D_{MIN} = \frac{N_{MIN} V_{OUT}}{V_{BULK(MAX)} + N_{MIN} V_{OUT}} \quad (16)$$

$$P_{CORE(MAX)} = \frac{8}{\pi^2 [4 D_{MIN}(1 - D_{MIN})]^{\gamma+1}} \cdot (C_m \Delta B^{\alpha} {f_{SW}}^{\beta}) \quad (17)$$

Second, with the f_{SW} expression and a given N, L_m can be calculated based on the predetermined minimum f_{SW} ($f_{SW(MIN)}$) at the lowest ripple voltage ($V_{BULK(MIN)}$) on the bulk input capacitor for the smallest operational AC line voltage. The $f_{SW(MIN)}$ selection of the ACF must consider the impact on full-load efficiency and the EMI filter design.

$$f_{SW(MIN)} = \frac{{D_{MAX}}^2 V_{BULK(MIN)}}{2 I_{IN(MAX)} L_m - D_{MAX} I_{m(-)} L_m + D_{MAX} T_{m(-)} V_{BULK(MIN)}} \quad (18)$$

where $I_{IN(MAX)}=P_{IN(MAX)}/V_{BULK(MIN)}$ and $D_{MAX}=NV_{OUT}/(V_{BULK(MIN)}+NV_{OUT})$, while for $I_{m(-)}$ and $T_{m(-)}$ refer to Table 4.

Third, with the P_{IN} equation, the maximum peak current ($I_{m(+)\_MAX}$) to the peak output power ($P_{OUT(MAX)}$) is calculated as

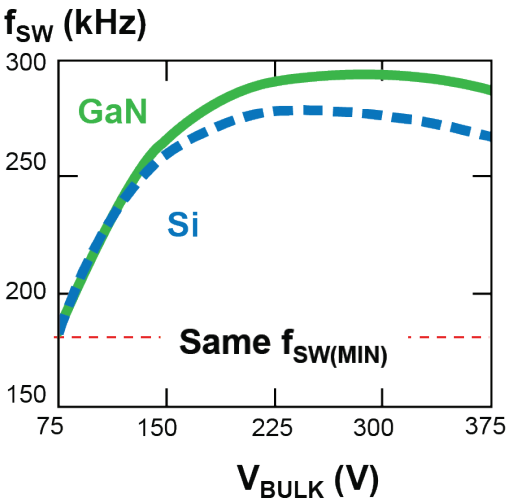
$$I_{m(+)\_MAX} = \sqrt{\frac{2 P_{OUT(MAX)}}{\eta L_m f_{SW(MIN)}} + {I_{m(-)}}^2} \quad (19)$$

Fourth, the turns number on the primary side of the transformer (N_P) is determined with two design considerations. One is to allow the maximum flux density (B_{MAX}) below the saturation limit of the magnetic core (B_{SAT}) at $I_{m(+)\_MAX}$. Another is to consider the AC flux density (ΔB) effect on the core loss due to the peak-to-peak magnetizing current. For high f_{SW} operation, the design consideration of N_P is mainly limited by the core loss, so B_{MAX} usually has an enough design margin below B_{SAT}.

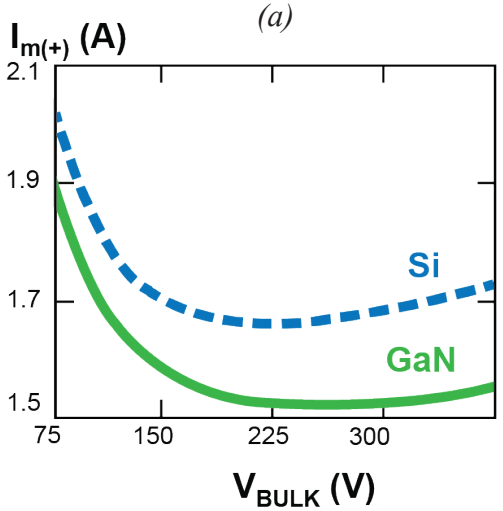
$$N_P = \frac{L_m (I_{m(+)} - I_{m(-)})}{\Delta B \cdot A_e} \quad (20)$$

$$B_{MAX} = \frac{L_m I_{m(+)\_MAX}}{N_P A_e} < B_{SAT} \quad (21)$$

In this paper, the above design procedure is applied to two 30 W ACF designs using GaN and silicon primary FETs with similar $R_{DS(ON)}$. The design constraints are the same: $f_{SW(MIN)}$ of 180 kHz at $V_{BULK(MIN)}$ = 75 V, N=3.25, V_{OUT}=20 V, RM6 transformer using 3F36 core material and 150 V rating SR (BSC360N15NS3). $C_{OSS(QL)}$ is calculated based on partial ZVS at 20 V for the silicon FET and based on full ZVS at 0 V for the GaN FET. Then, it is found that L_m for silicon is 85 μH and L_m for GaN is 95 μH. With that, the above analytical equations can be used to compare the parameter variations for a wide V_{BULK} range. Figure 24 shows the calculation results of $I_{m(+)}$ and $I_{m(-)}$ at high line and it provides a clear message that GaN provides significant core loss and RMS current reductions due to lower peak-to-peak current.



(a)



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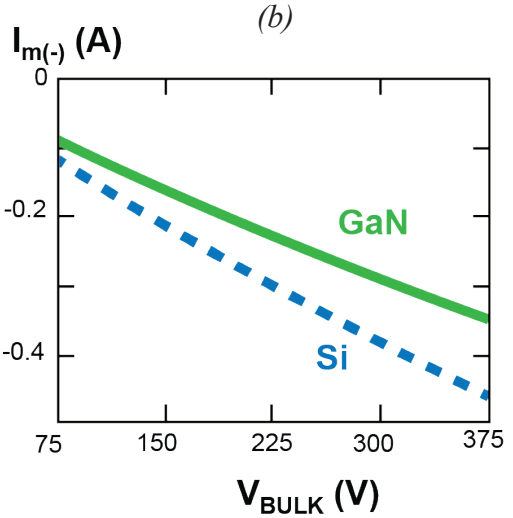
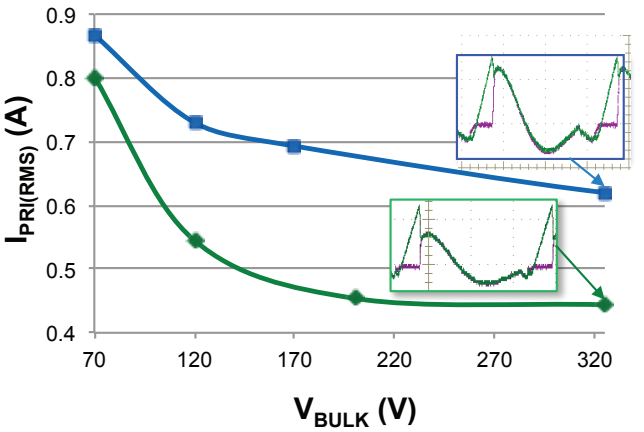


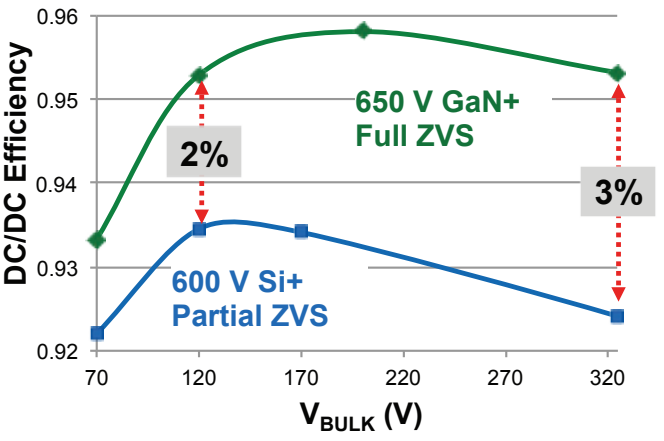
(c)

Figure 24 – Comparison of operating conditions of Si and GaN-based ACF: (a) f_{SW}, (b) $I_{m(+)}$ and (c) $I_{m(-)}$.

The measurement results on the full-load efficiency and primary RMS current of the two power stage designs are compared in Figure 25(a) and (b), respectively. The significant RMS current reduction is contributed to by not only the low peak-to-peak I_m as the calculation results show, but also the current dipping effect as explained in Section I. In the end, the GaN ACF power stage provides superior efficiency over the optimized silicon-based ACF. The difference of 2% at low line and 3% at high line is the efficiency of the DC/DC stage only. As the input stage (including the EMI filter, bridge diode, fuse and inrush current limit NTC resistor) is included, the efficiency difference will be even greater.



(a)



(b)

Figure 25 – Performance comparison on a 30 W adapter: (a) RMS current difference and (b) full-load efficiency.

SUMMARY

This paper provides a comprehensive analysis on how C_{OSS} nonlinearity from primary and secondary switching devices impacts the switching behavior and system efficiency of the ACF across a wide load range. It is found that the superior performance of GaN-based ACF is not just due to ultralow C_{OSS}, but also the current dipping effect on significant primary RMS current reduction. Solutions to minimize the C_{OSS} nonlinearity impact of Si-based ACF are investigated to reduce the efficiency gap with a GaN design. The proper clamp capacitor design and partial ZVS control with an optimal ZVS point are addressed and burst mode control is proposed to exhibit better average efficiency than the state-of-the art light load control. Moreover, analytical equations are derived to simplify power stage design, accounting for C_{OSS} nonlinearity. Based on this proposed design procedure, two 30 W ACF designs with state-of-the-art GaN and silicon FETs are developed and the optimal performances are compared.

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