- The PWR_2 and PWR_3 voltage selections requested by the BGA SSD may not support a 200 mV voltage differential at the tolerance extremes, e.g., for PWR_2 = 1.14 V (1.2 V) and PWR_1 = 0.98 V (0.9 V), the minimum voltage difference may only be 160 mV.

  BGA SSDs designed for such voltage selections are responsible for supporting a smaller difference of the possible voltages considering voltage tolerances.

  Systems that support such voltage selections are recommended to keep the voltage difference as large as practical.
- After the voltage on both the 3.3 V supply and the VIO 1.8 V supply are below 300 mV, there is no specified relationship between them.
- The voltage on all supplies should remain below 100 mV for at least 1 ms before the power-on sequence is attempted.

If the power-off sequencing is not followed, there is a risk that the Adapter may not power-off correctly or the Adapter may be damaged. These results are vendor specific.

4.4. Electrical Requirements for BGA SSDs

4.4.1. BGA SSD Voltage Supply Power-on Sequencing

The host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, the PWR_2 supply, and the PWR_3 supply during power-on:

- After the voltage on the PWR_2 supply or the voltage on the PWR_3 supply reach 300 mV, the voltage on the PWR_2 supply should remain greater than the voltage on the PWR_3 supply by at least 200 mV.
- The voltage on the PWR_1 supply has no timing relationship relative to the voltage on the PWR_3 supply or the voltage on the PWR_2 supply.

If the power-on sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 4-1 shows three power-on ramp examples that follow the recommendations of this section for the case where each of the power rails is assigned a different voltage. The first example shows PWR_2 reaching 300 mV before PWR_3 reaches 100 mV. The second example shows PWR_2 well above 300 mV by the time PWR_3 reaches 100 mV. The third case shows PWR_2 reaching 300 mV at the same time as PWR_3. Note that the PWR_1 rail is not shown since it has no timing relationship to the other rails.

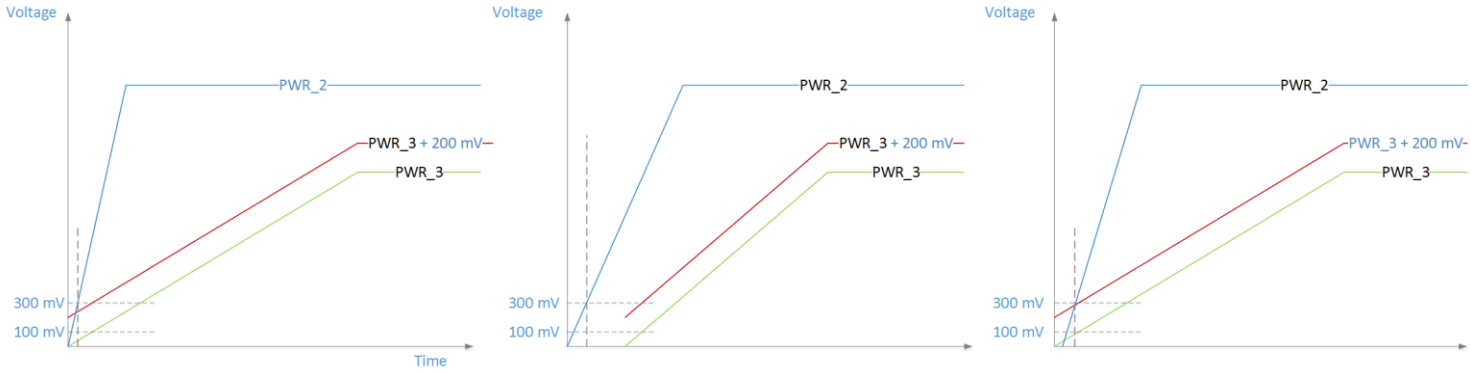

Figure 4-1. Power-on Sequencing Examples

4.4.2. BGA SSD Voltage Supply Power-off Sequencing

The host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, the PWR_2 supply, and the PWR_3 supply during power-off:

- Before the voltage on the PWR_3 supply and the voltage on the PWR_2 supply reach 300 mV, the voltage on the PWR_2 supply should remain greater than voltage on the PWR_3 supply by at least 200 mV.
- After both the voltage on the PWR_2 supply and the voltage on the PWR_3 supply is below 300 mV, there is no specified relationship between them.
- The voltage on the PWR_1 supply has no timing relationship relative to the voltage on the PWR_3 supply or the voltage on the PWR_2 supply.
- The voltage on all supplies must remain below 100 mV for at least 1 ms before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 4-2 shows two power-off ramp examples that follow the recommendations of this section for the case where each of the power rails is assigned a different voltage. Note that the PWR_1 rail is not shown since it has no timing relationship to the other rails.

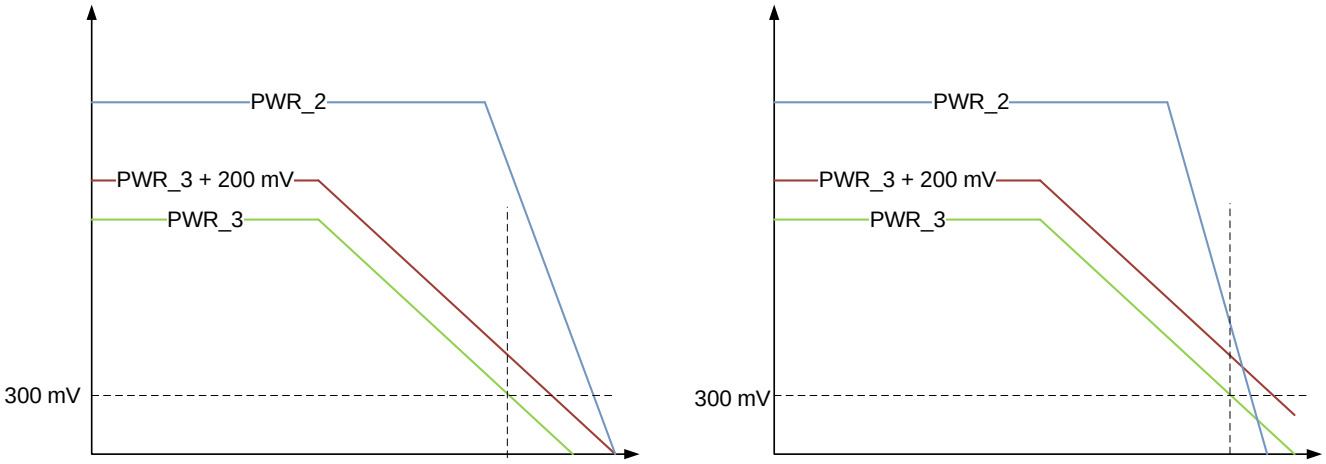

Figure 4-2. Power-off Sequencing Examples

4.4.3. BGA SSD Power Ramp Timing

The power ramp timing is defined as the time the power rail needs to ramp to a valid voltage (see Table 4-3). This timing is recommended for power-on only.

Table 4-3. Power Ramp Timing

Supply Voltage	Max*
3.3 V	35 ms
2.5 V	30 ms
1.8 V	25 ms
1.2 V	20 ms
1.1 V	20 ms
0.9 V	20 ms
0.8 V	20 ms

* The minimum timing may be calculated from the maximum slew rate recommendation in Table 4-4.