DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
8080875

DRAFTER:	K. SINCERBOX	DATE:	02/15/2017
DESIGNER:		DATE:	
CHECKER:	T. LEQUANG	DATE:	02/15/2017
ENGINEER:	B. TAN	DATE:	02/15/2017
APPROVED:	E. REY	DATE:	02/15/2017
RELEASED:	WDM	DATE:	02/15/2017
TEMPLATE INFO:	EDGE# 4218519	DATE:	04/07/2016

DIMENSIONS IN MILLIMETERS

TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER 01295

ePOD, PWP0016A / HTSSOP,
16 PIN, 0.65 MM PITCH

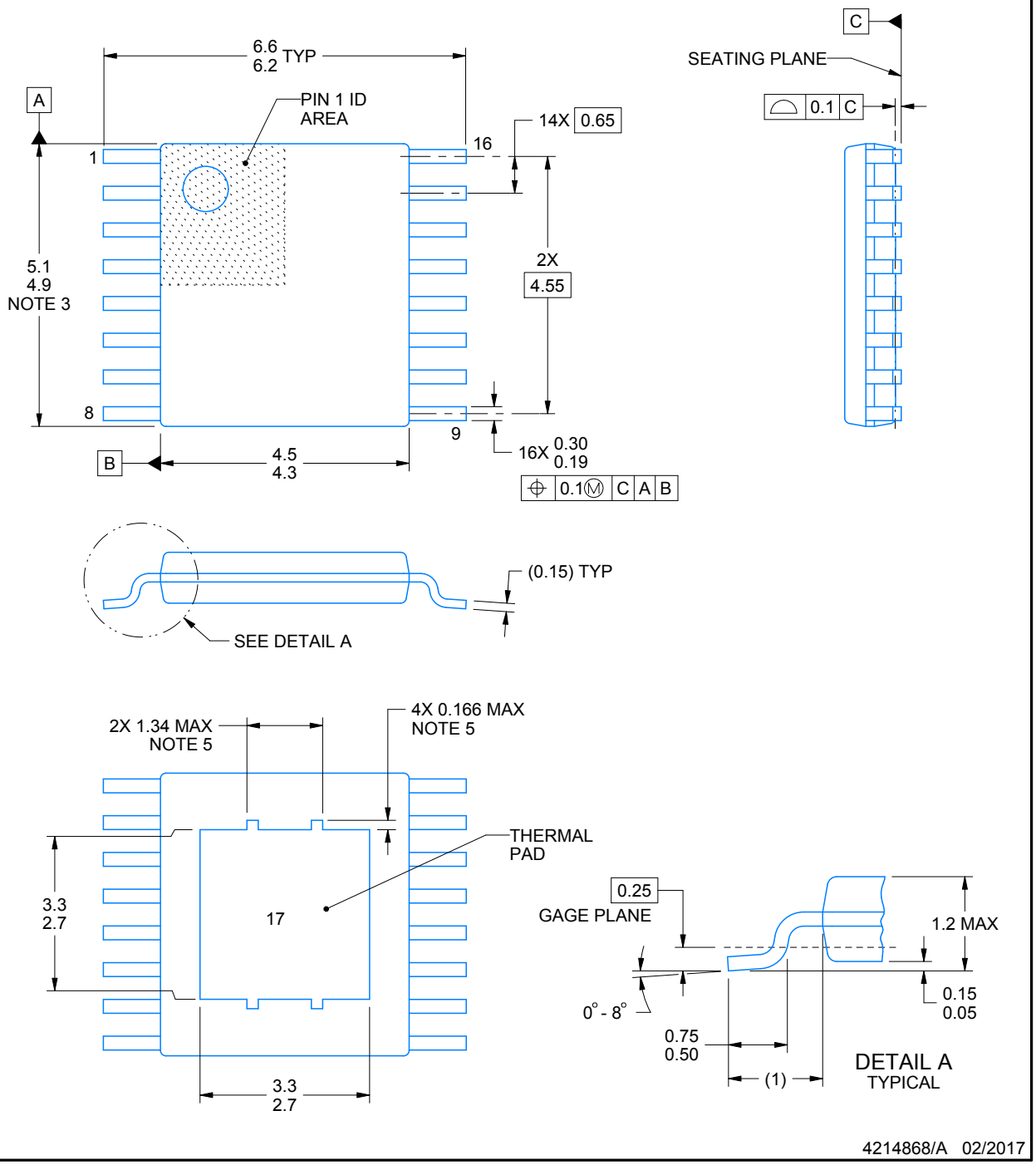
SCALE	SIZE		REV	PAGE
NTS	A	4214868	A	1 OF 5

PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

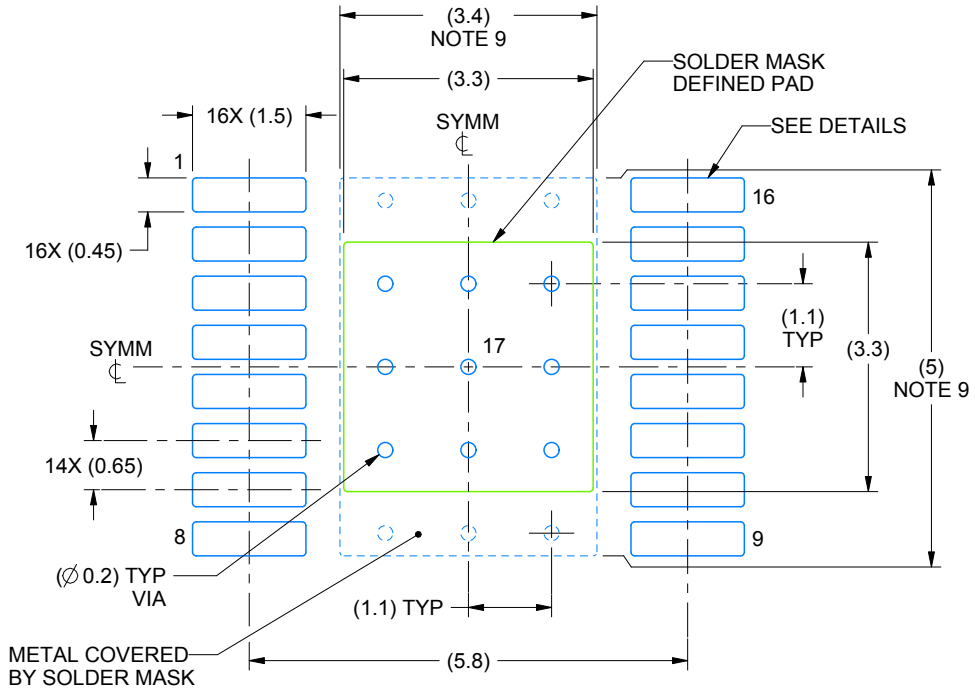
PLASTIC SMALL OUTLINE



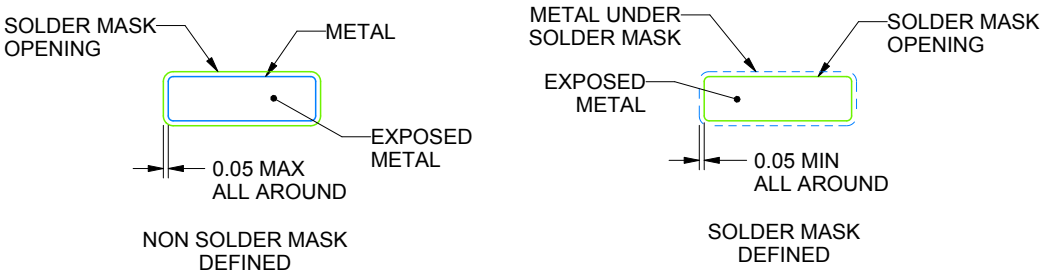
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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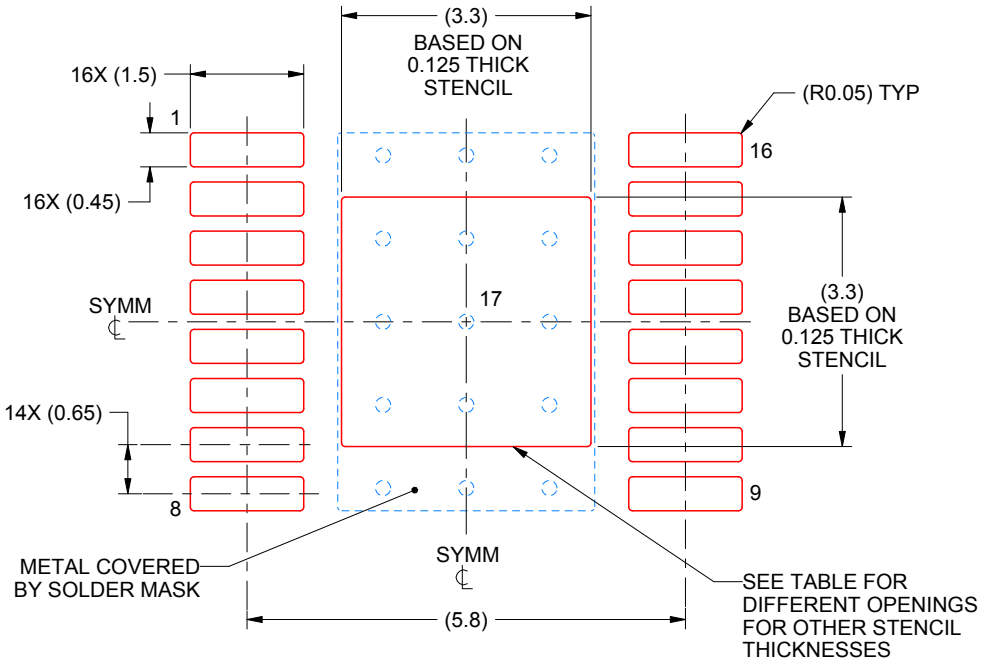
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2161114	02/15/2017	B. TAN / K. SINCERBOX