DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4212697

DRAFTER:	T. LEQUANG	DATE:	02/10/2017
DESIGNER:		DATE:	
CHECKER:	K. SINCERBOX	DATE:	11/09/2017
ENGINEER:	B. TAN	DATE:	11/09/2017
APPROVED:	E. REY & D. CHIN	DATE:	11/09/2017
RELEASED:	WDM	DATE:	11/09/2017
TEMPLATE INFO:	EDGE# 4218519	DATE:	04/07/2016

DIMENSIONS IN MILLIMETERS

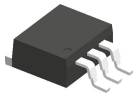
TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER 01295

ePOD, KTT0003B / TO-263,
3 PIN, 2.54 MM PITCH

SCALE	SIZE		REV	PAGE
NTS	A	4215105	A	1 OF 5

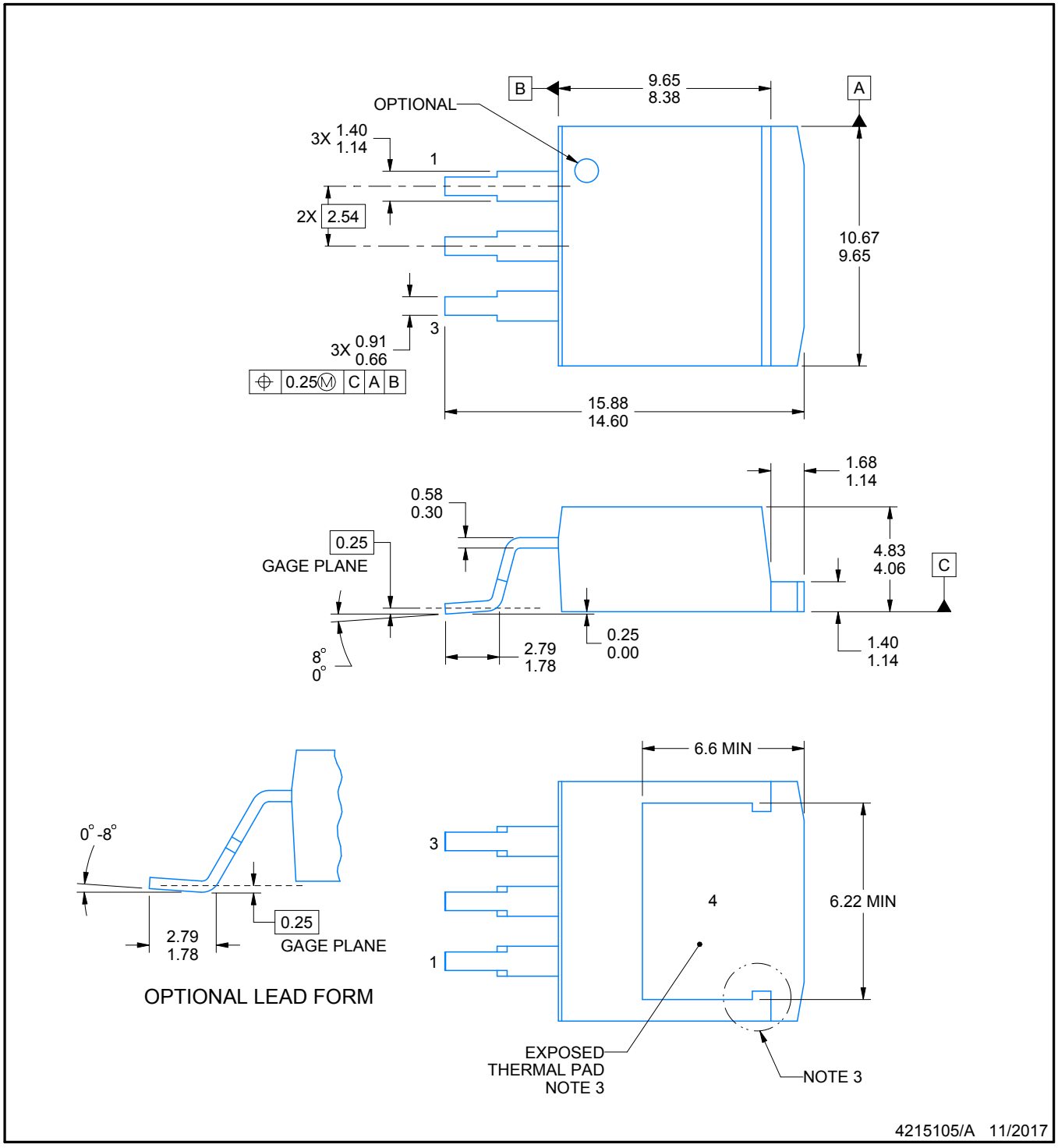
KTT0003B



PACKAGE OUTLINE

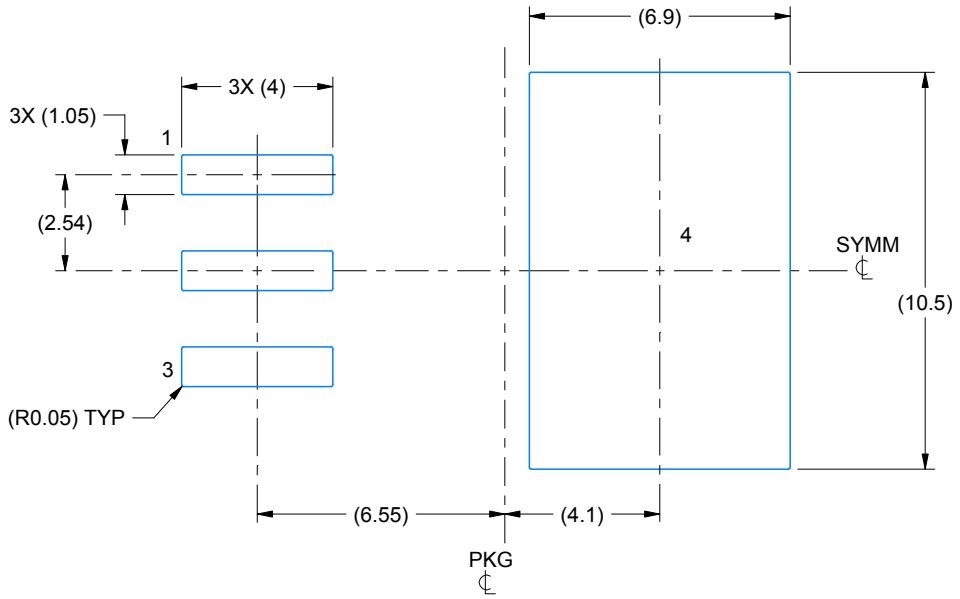
TO-263 - 4.83 mm max height

TO-263

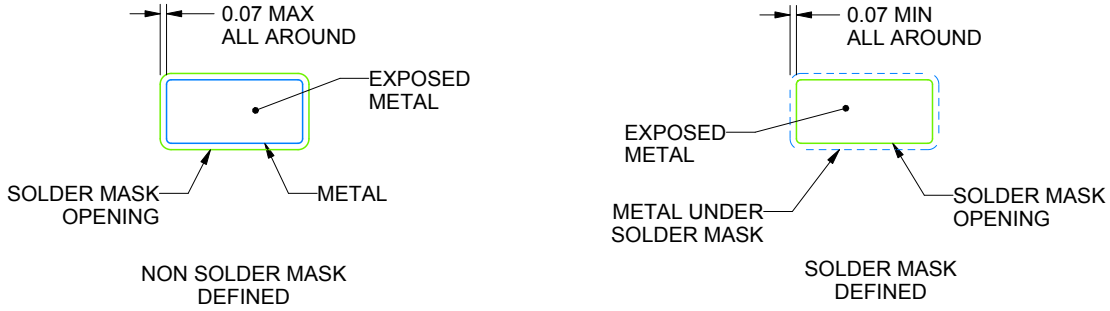


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263, except minimum lead thickness and minimum exposed pad length.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

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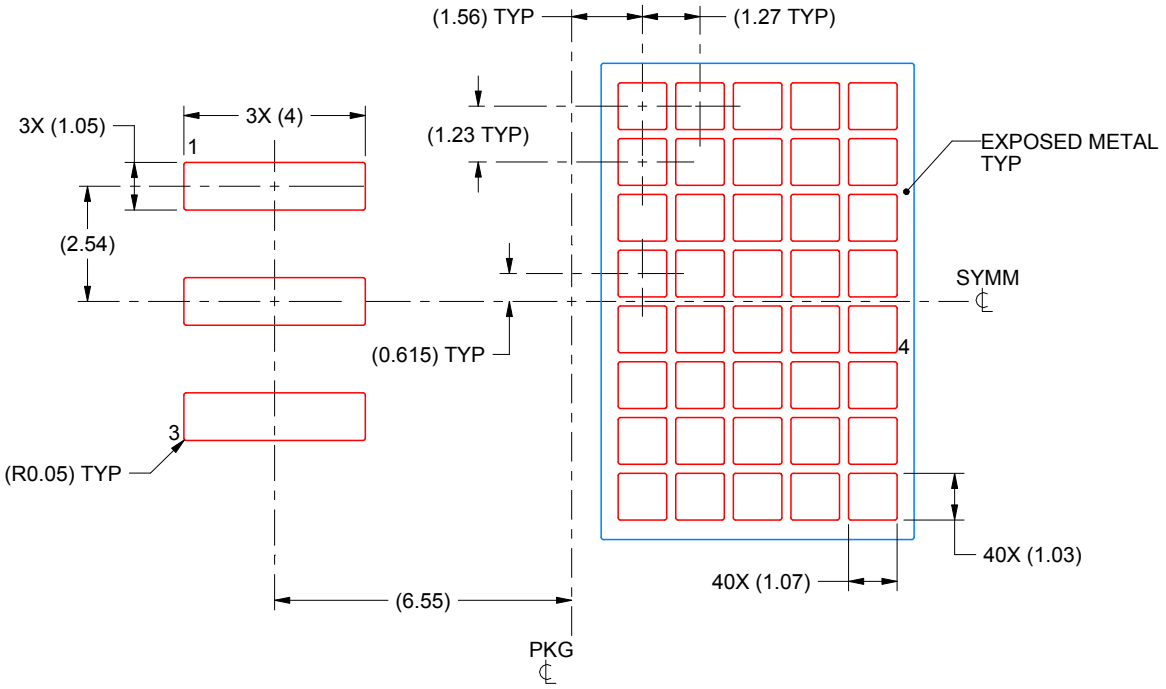
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2165743	11/09/2017	B. TAN / T. LEQUANG