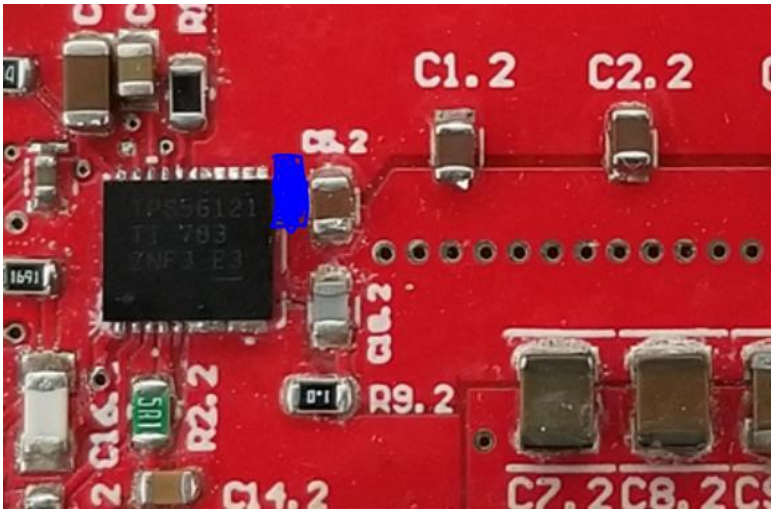
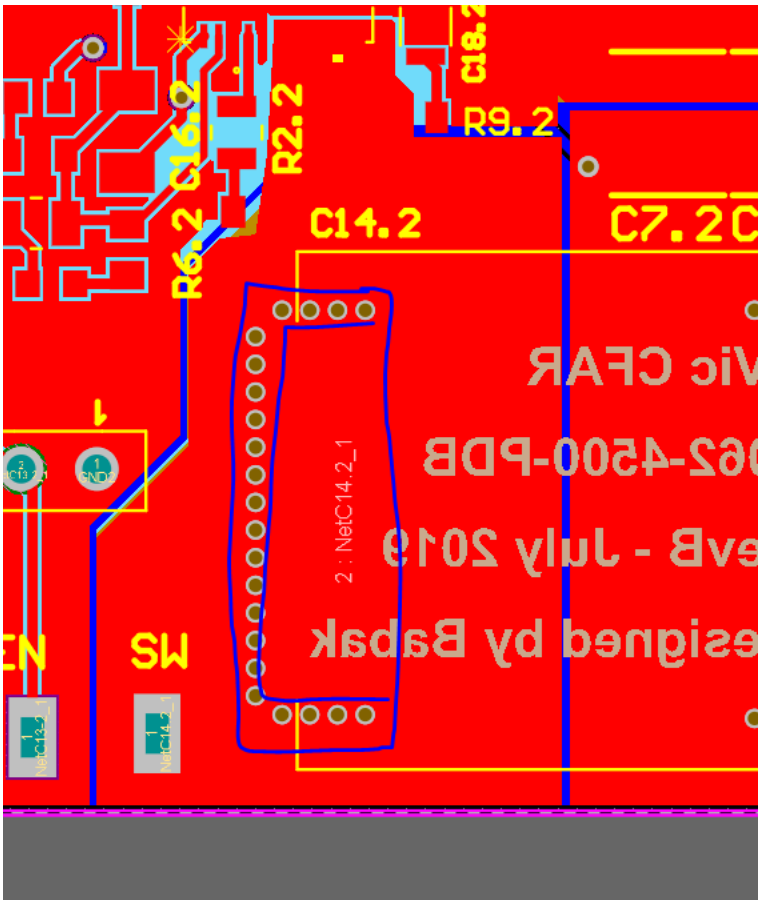
Place a 1uF ceramic where the blue mark is.



The SW node needs to be smaller.
There are vias connecting the SW node to two internal layers.
Cut the board so that the vias are not connecting to the internal nodes.
The clearance from the SW pour to other traces are as little as 3mils.
The clearance distance could be cause of the noise issue.



On the output. you are using 5x 100uF/16V capacitors.
The excel sheet is assuming 5x100uF. But the effective capacitance of a 16V caps used at 8V dc 50%.
Ceramics need to be derated based on the voltage.
Either double the capacitance to troubleshoot or recalc and change components.

PGOOD is connected incorrectly .