

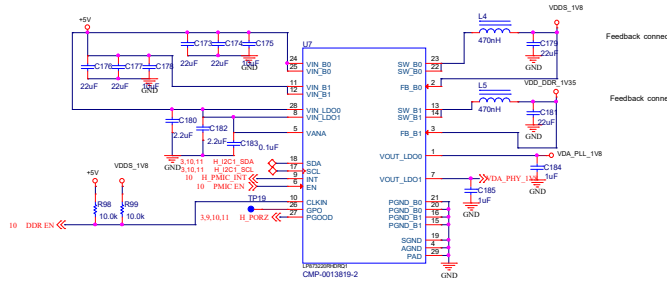
OTP Sequencing for LP8732:

1. VDDS_1V8 (SMPS0 LP87322 1.8V, 1.5 A max)
2. VDA_PLL_1V8 (LDO0 LP87322 1.8V, 300 mA max)
3. VDD_DDR_1V35 (SMPS1 LP87322 1.35V, 2 A max)
And: DDR EN (GPO2) CLKIN LP87322, Enables TPSS1200)
4. VDD_CORE_AVS (SMPO LP87322 1.15V, 3 A max)
5. VDD_DSP_AVS (SMPS1 LP87322 1.06V, 3 A max)
6. VDA_PHY_1V8 (LDO1 LP87322 1.8V, 300 mA max)
7. REGEN1 (GPO LP87322 Open Collector pulled-up to 3.3V)
Enables Switch U27 to switch 3.3V to Ethernet, J6Entry VDDSHVx rails)
8. VDA_USB_3V3 (LDO1 LP87322 3.3V, 300 mA)
9. VDDSHV6 (LDO0 LP87322 1.8V, not used)

CLIN is used as GPO2 for both devices.
All logic pins INT, EN, GPOs, and PGOODs are open Drain.

Both PGOODs and GPO LP87322 create the SMRT_PORz signal.

PMIC EN comes from first stage power supply PGOOD signal.



Feedback connect after C259

Feedback connect after C263

