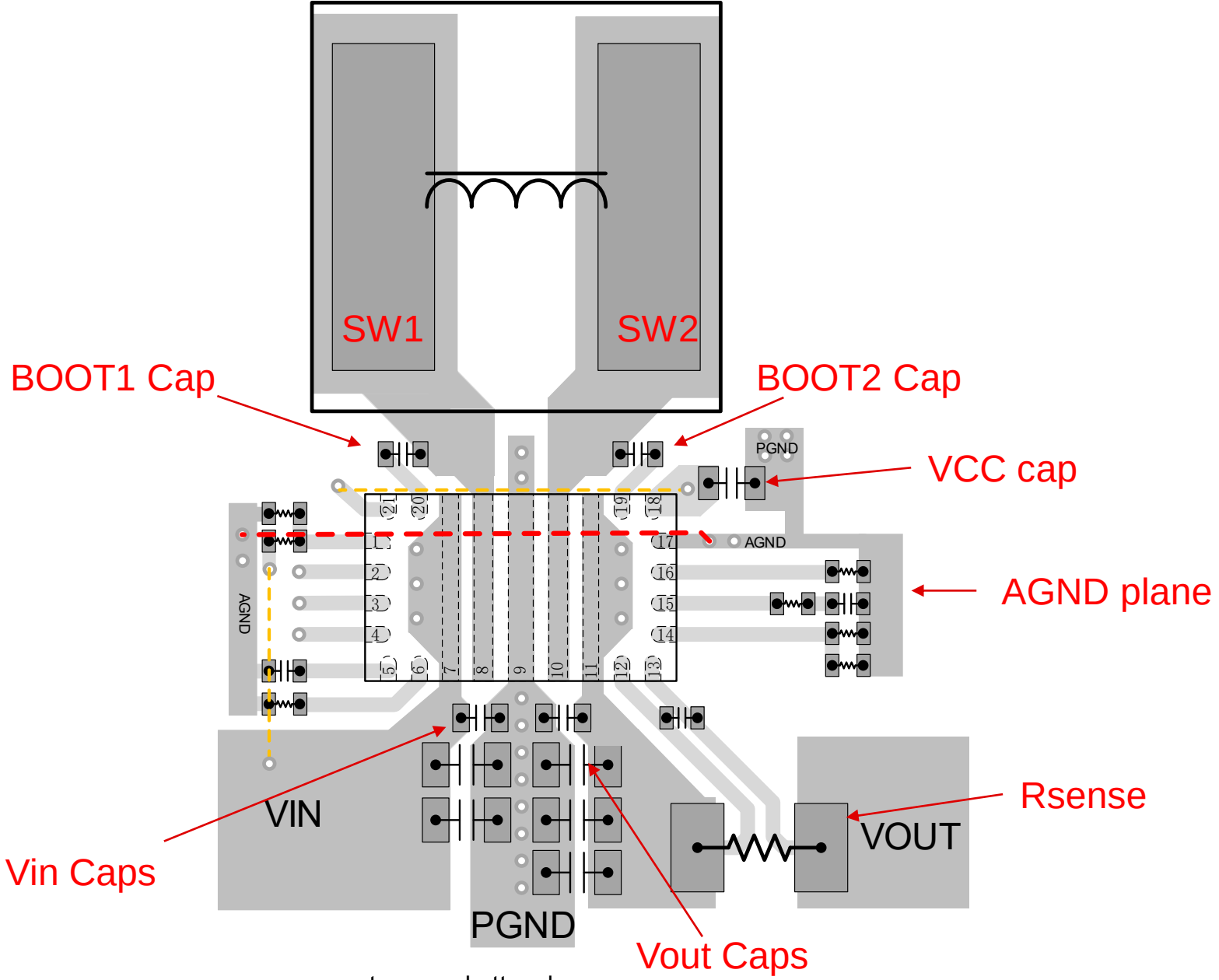
TPS55289 Layout Guideline

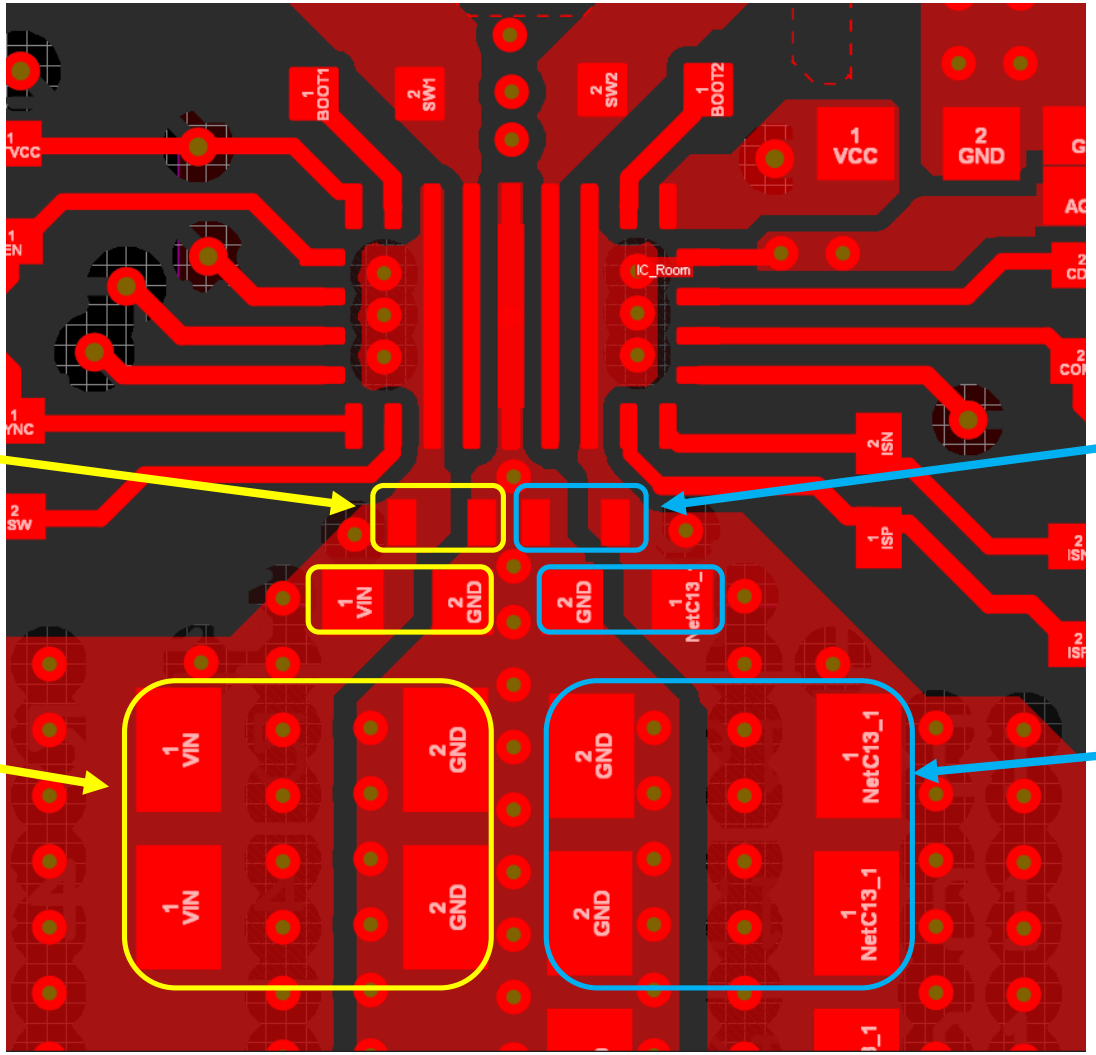


The first inner layer is the PGND plane

Step 1 Vin cap, Vout cap

Put 0.1uF/0402 package ceramic cap (CHF_IN) close to VIN pin and PGND pin with wide, short copper.

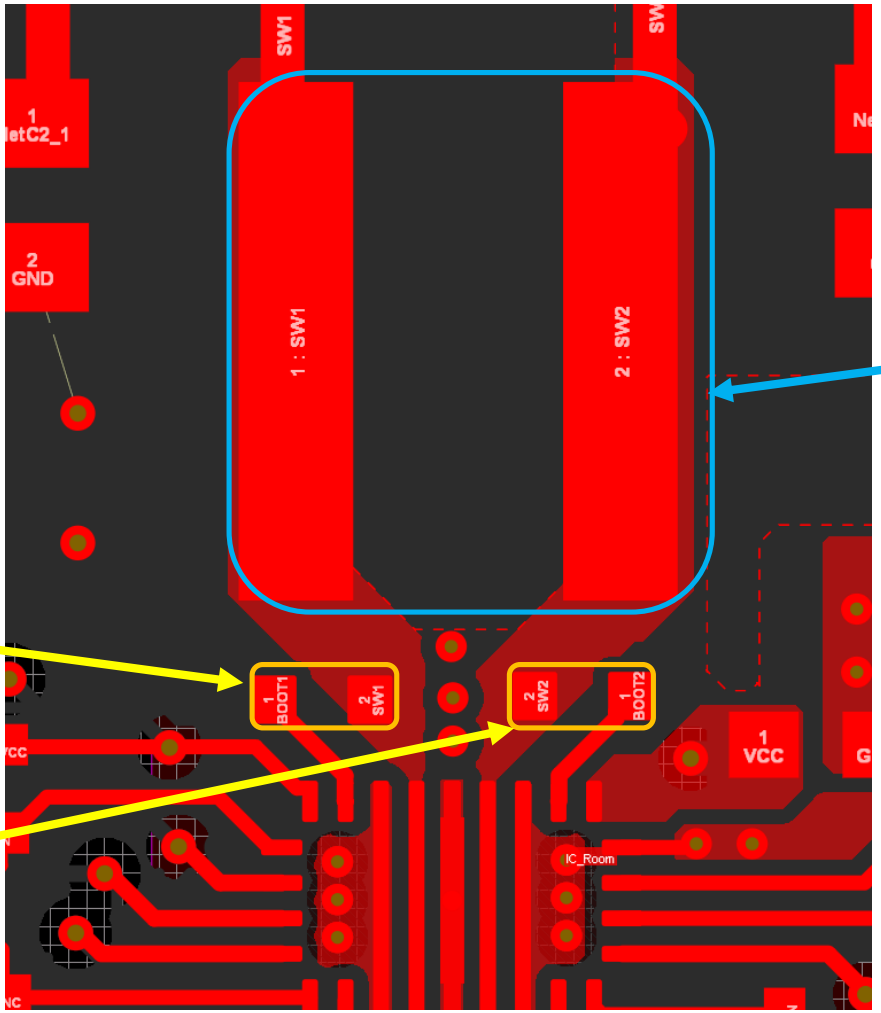
Put the rest input ceramic capacitors close to the CHF_IN cap.



Put 0.1uF/0402 package ceramic cap (CHF_OUT) close to Vout pin and PGND pin with wide, short copper.

Put the rest output ceramic capacitors close to the CHF_OUT cap.

Step 2 Inductor, Boot 1 & 2 capacitor

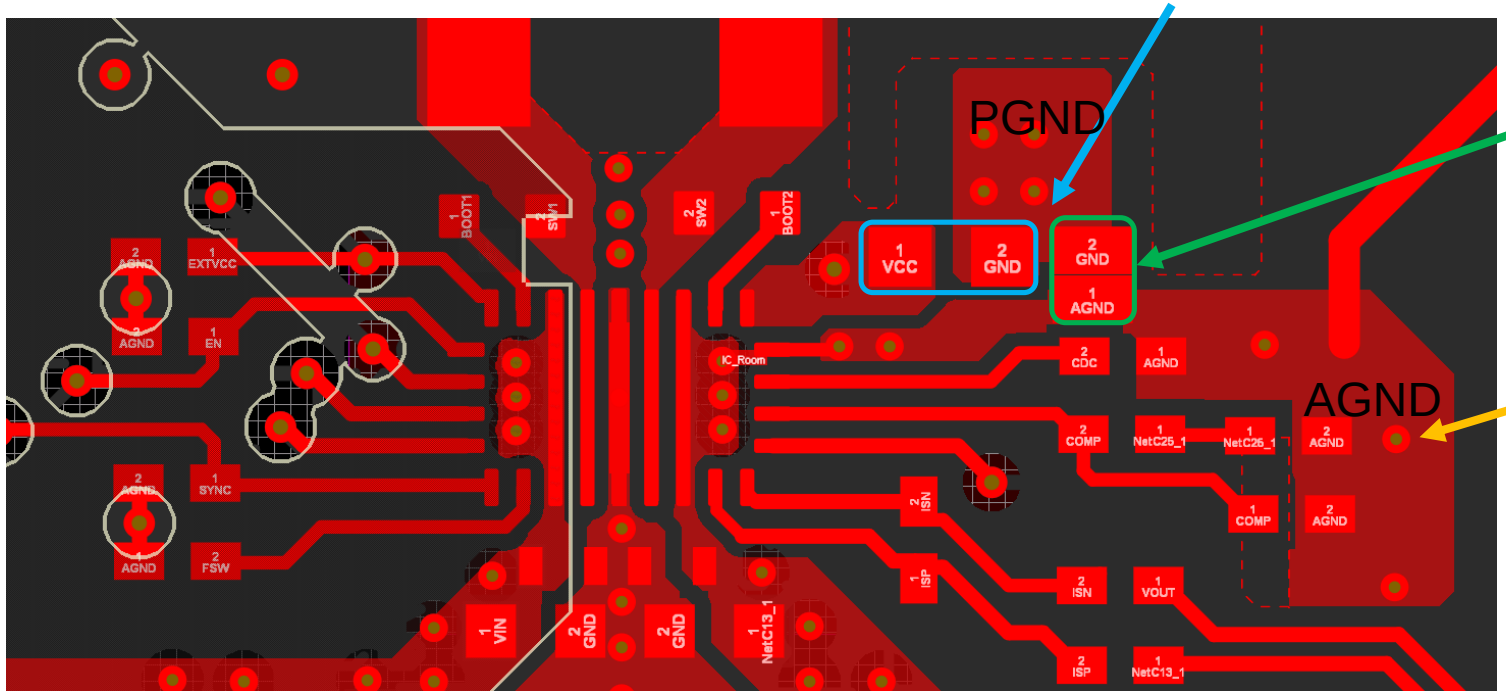


Connect the inductor with TPS55289 SW1, SW2 pin with short, wide copper.

Put the BOOT 1& 2 capacito close to IC. Connect with IC BOOT1 and BOOT2 pin with short trace.

Step 3 VCC capacitor, AGND plane

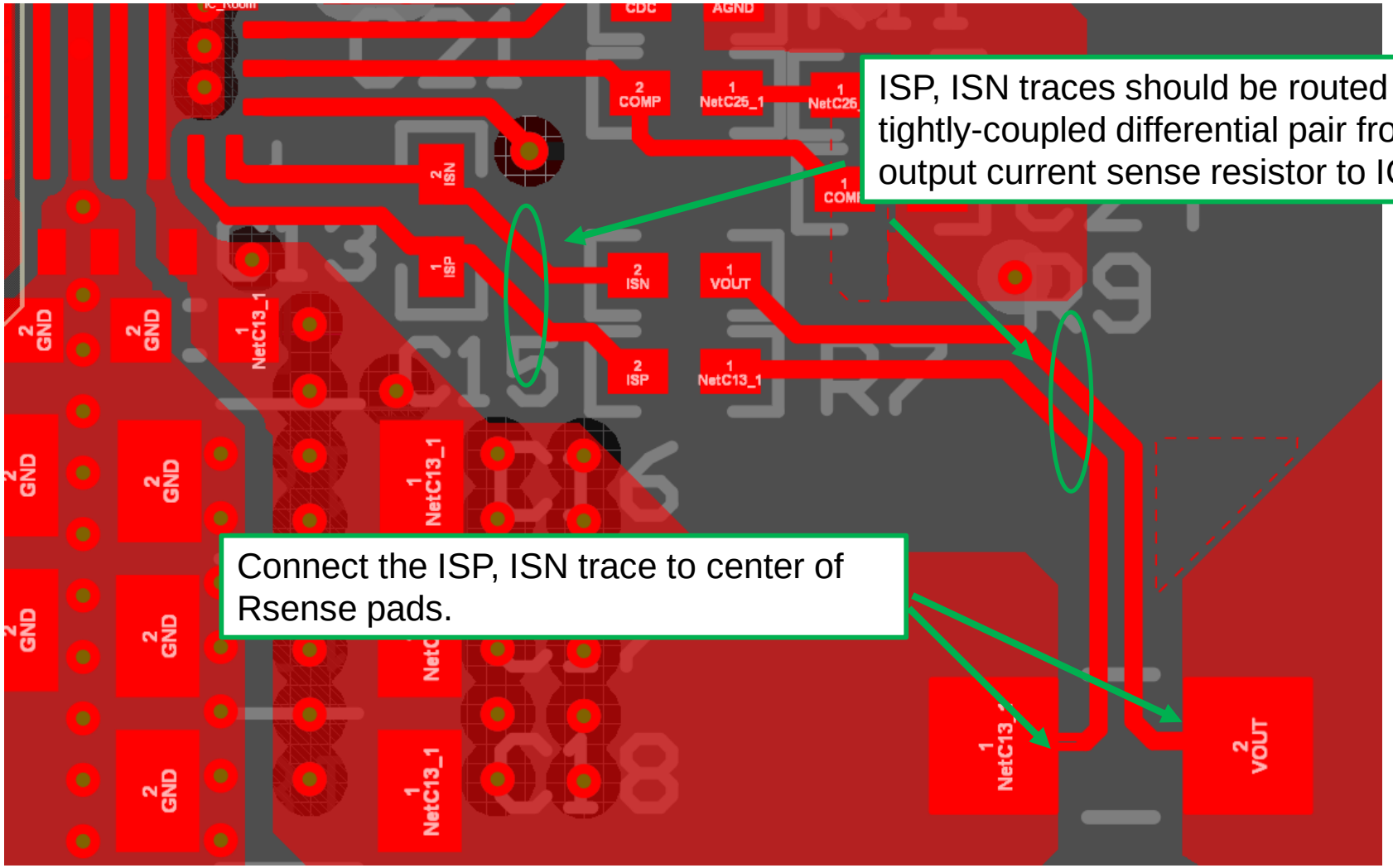
Put the VCC 4.7uF capacitor close to VCC pin. Connect the capacitor with VCC pin with short, Wide trace. Add 3-4 PGND vias close to 4.7uF cap.



Connect AGND plane and PGND plane at the terminal of the VCC capacitor.

Compensation network, CDC, Fsw, etc should connect to AGND plane.

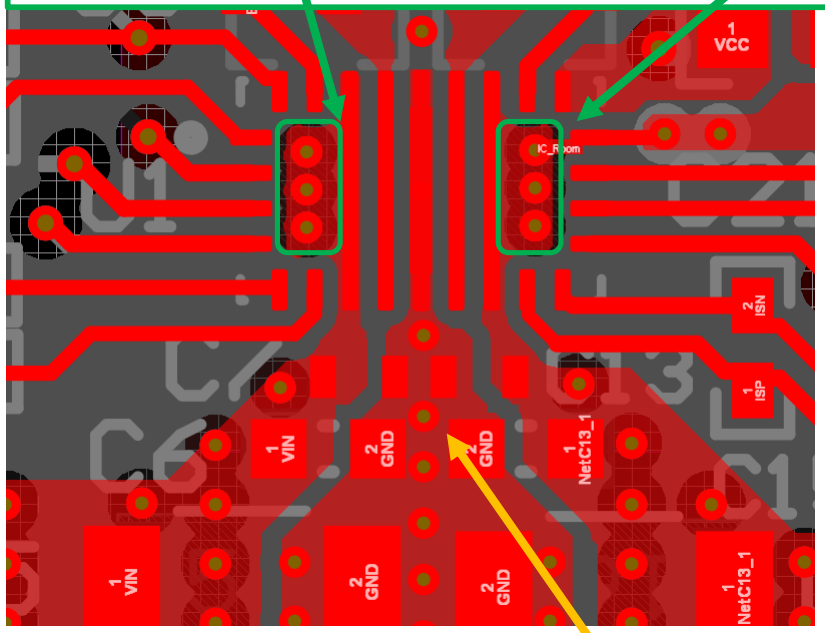
Step 4 Output Current Sense Trace, ISP & ISN



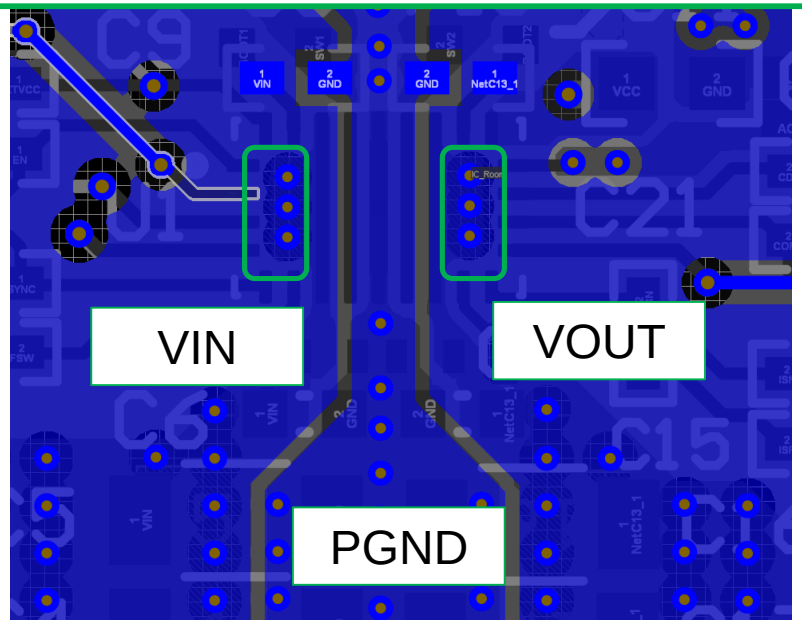
Step 5 Optimize Thermal Performance

Suggestion 1:

Add 3 thermal vias close to VIN pin and 3 thermal vias close to Vout pin to help improve thermal dissipation.
Connect the thermal vias to a large VIN area and Vout area on bottom layer separately.



Top layer



Bottom layer

Suggestion 2: Add enough GND thermal vias close to PGND plane, VIN & VOUT plane.

Step 6 Optimize the Switching spikes and EMI

Put two 0.1uF/0402 package ceramic caps (CHF_IN and CHF_OUT) close to VIN pin and PGND pin and Vout to PGND on bottom layer