Understanding, Measuring, and Reducing Output Voltage Ripple

Simple Switchers Wiki

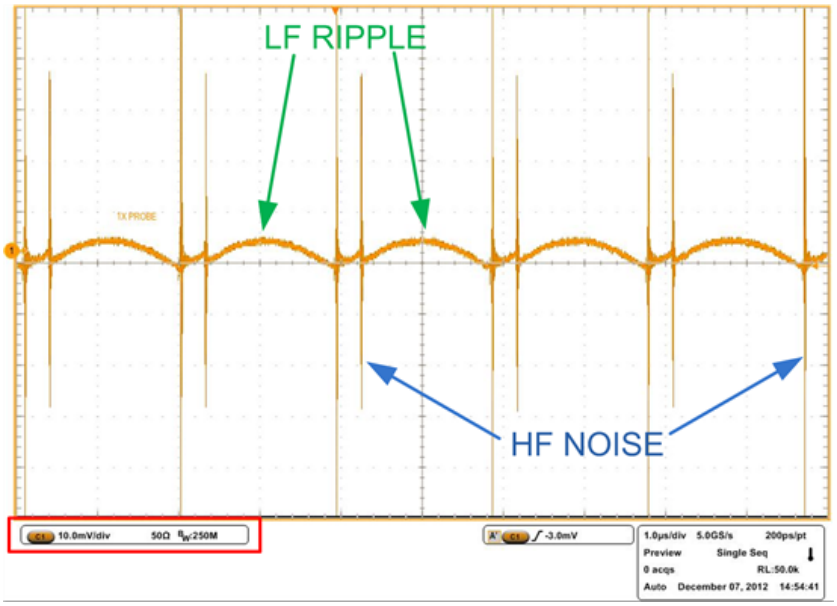
Overview

So you have designed and built your new buck regulator and now you would like to measure the output voltage ripple. You hook up your scope probe and see HUGE spikes on the output voltage. Are these real?! Or maybe you don't see HUGE spikes but there is still too much ripple? What can you do to fix this?

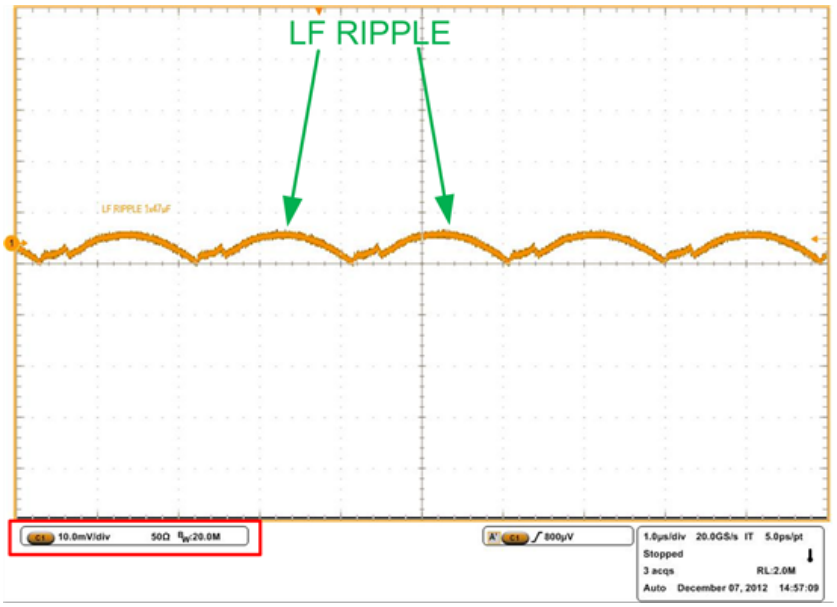
A lot of the problems you will encounter with DC-DC converters are due to parasitic elements that do not "officially" appear anywhere in your schematics. The following applications brief will attempt to explain where this output ripple comes from (think parasitics!), how to properly measure it, and what you can do to reduce it.

1. Ripple Origin

The output voltage ripple has two components: Low Frequency "ripple" and High Frequency "noise". Here is an example:



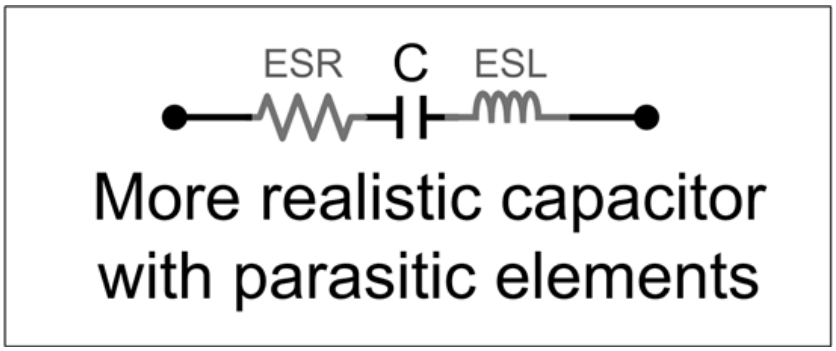
Depending on how you perform the measurement, e.g. using limited bandwidth on your oscilloscope, you may or may not capture the HF noise and could only see the LF ripple which appears at the regulator's switching frequency. Then, the waveform would look more like this:



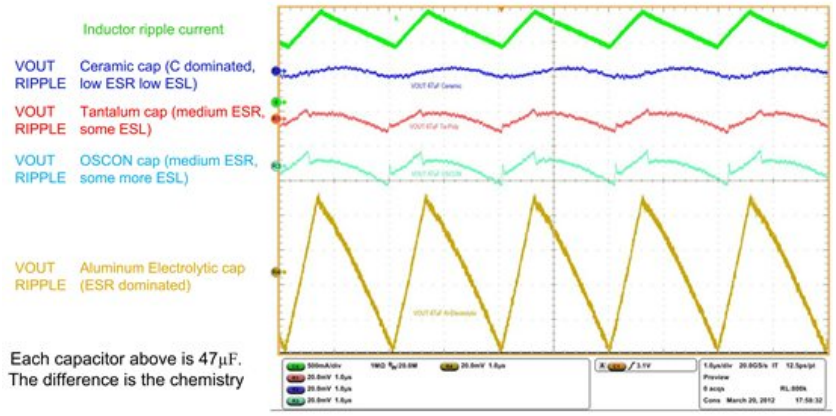
1.1. LF Ripple

Let's look at this LF ripple first.

The LF voltage ripple is a function of the inductor ripple current going through the output capacitor's impedance. This impedance is formed by the capacitance value along with the parasitic equivalent series resistance (ESR) and parasitic equivalent series inductance (ESL) that come "free of charge" with your capacitor.



Depending on the type of output capacitor, the values of its parasitic elements could be quite different and consequently the shape and amplitude of the output ripple voltage will vary. Here is one example using off-the-shelf capacitors with matching capacitance values but different chemistry types (e.g. ceramic, tantalum, OSCON, Aluminum Electrolytic):

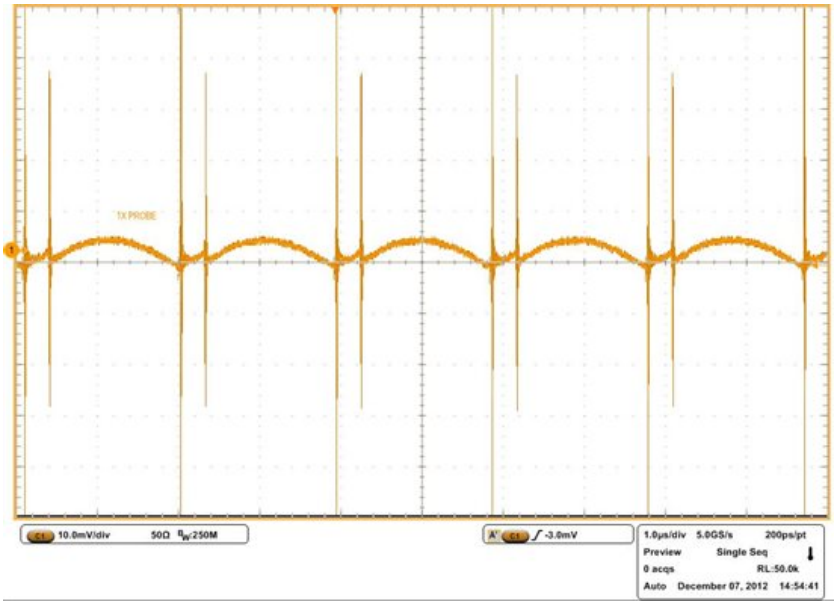


If the output capacitor has large ESR (typical for Aluminum Electrolytic), the ripple shape is more triangular (ESR dominated). If there is some ESL (see the OSCON type waveform) you will notice some voltage steps at the peak and valleys of the ripple waveform. If you use ceramic capacitor, the voltage ripple will be sinusoidal since the ESR and ESL terms are very small.

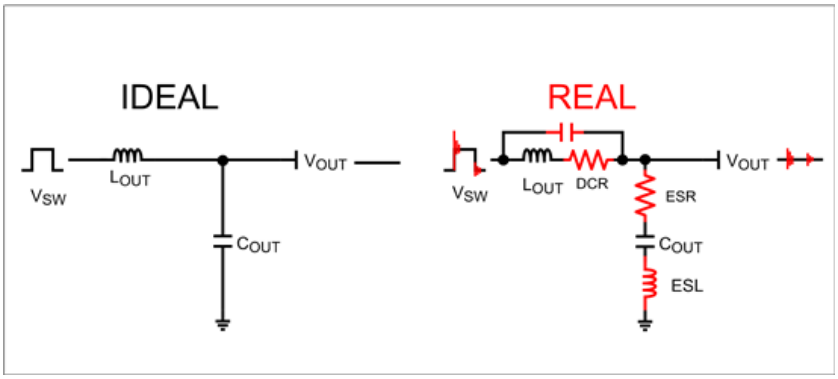
1.2. HF Noise

Let's look at the high frequency noise and determine where it's coming from.

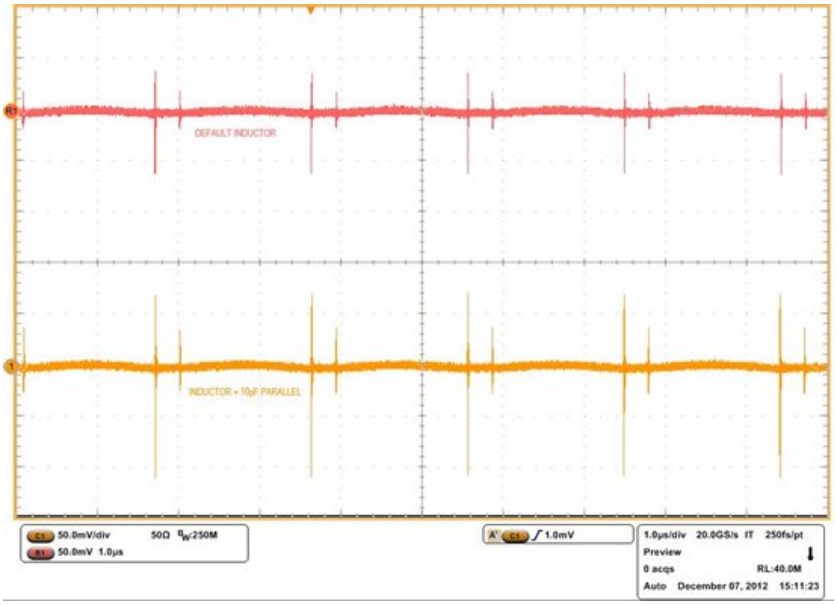
If you set your scope to higher than 20MHz bandwidth, you will most likely start observing high frequency voltage spikes on the output, as in this example:



These spikes appear on the output through the parasitic capacitance across the output inductor. The fast edge of the switch node voltage couples right through this parasitic capacitance. This issue gets worse with bad board layout where the switch voltage leading edge may already be ringing several volts above the input voltage and higher than normal spikes would be coupling through. We will talk about the switch node ringing problem in more detail later on. Here is an illustration of the parasitic elements in the "real" output filter.



The parasitic capacitance across the inductor could be 10s of pico-farads. The higher it is, the larger the spikes will be on the output. Here is a comparison of the HF output noise using a default inductor and the same inductor but with additional 10pF of capacitance in parallel:

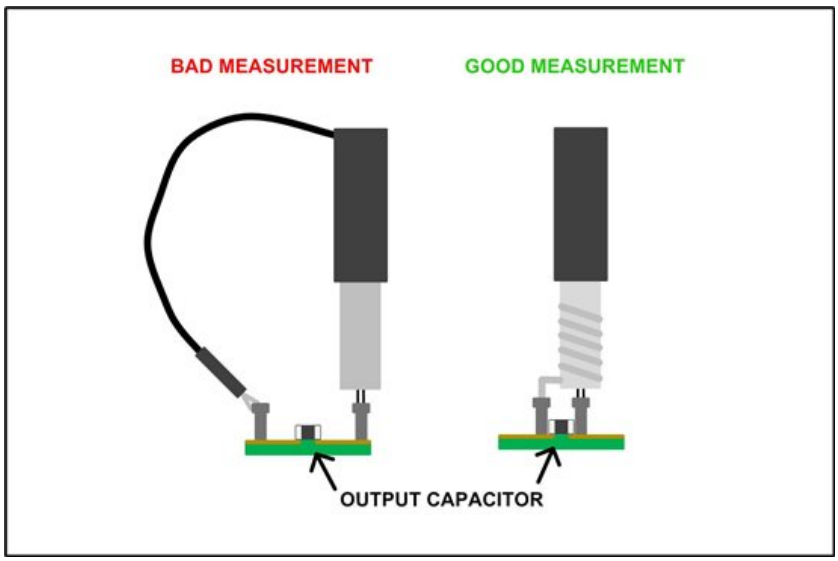


The spike ringing frequency can be in the 100's of MHz and will be modulated by the inductor's parasitic capacitance and the output cap impedance.

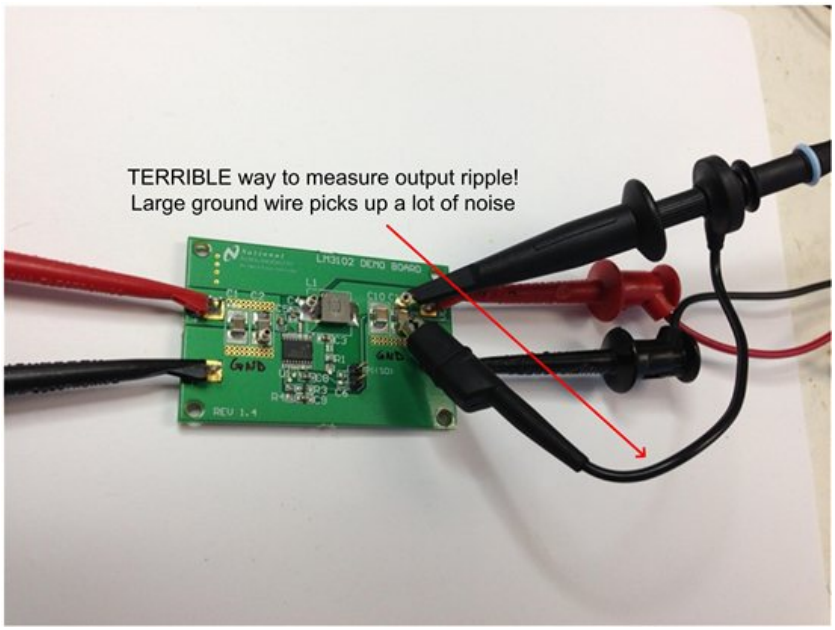
Before we go into a discussion on how to lower the LF ripple and the HF noise, let's make sure we are measuring it correctly. The ripple and noise may not be as bad as it seems.

2. Measuring Output Ripple

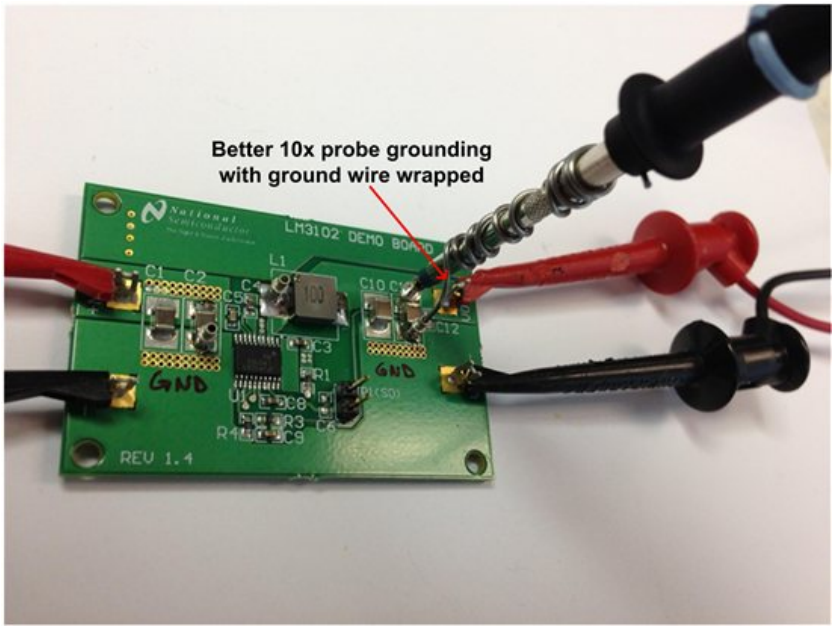
2.1. Probe grounding and noise pickup



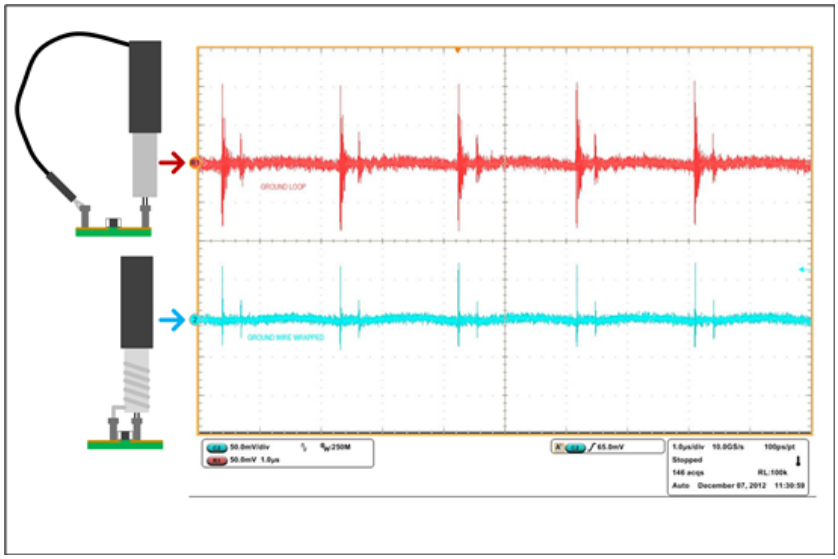
Here is a good example of a **bad way** to take output voltage measurement.



Using the alligator clip GND wire of your oscilloscope probe forms a nice loop antenna will pick up radiated noise. A better way to measure is to use a wrapped ground wire around the barrel of the scope probe. This will make the loop area of this antenna much smaller and will greatly reduce the noise pickup. Here is an example of this simple probe modification:



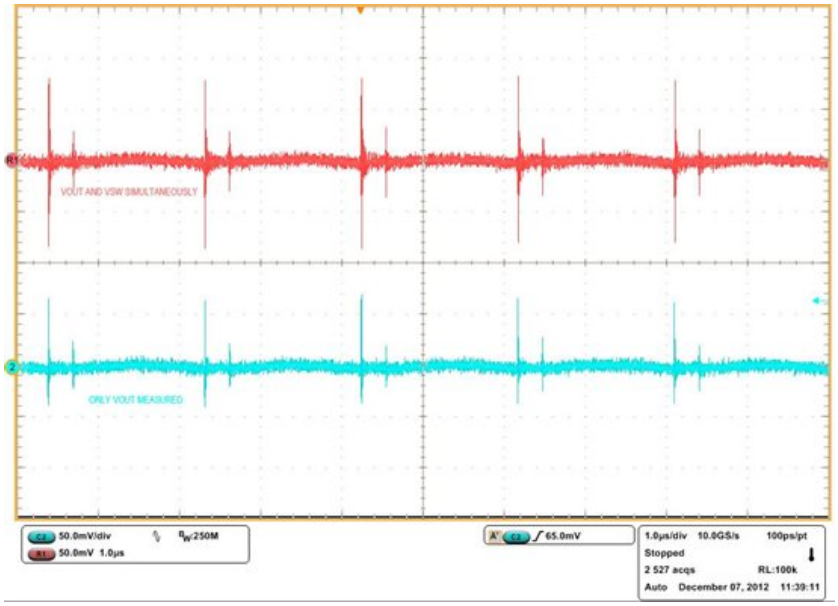
Let's compare the two probes. Here is a scope shot showing measurements taken with large ground loop probe vs the ground wire wrapped around the probe:



Another pitfall of measuring output noise is taking other measurements at the same time while measuring VOUT. For example, you may want to look at the switch waveform as you are also observing the output voltage ripple. But measuring the switch node at the same time as the output voltage will couple in additional noise and make your output voltage noise measurement worse. This is regardless of whether you use a ground wire wrapped around the probe. Here is an example:

The setup:

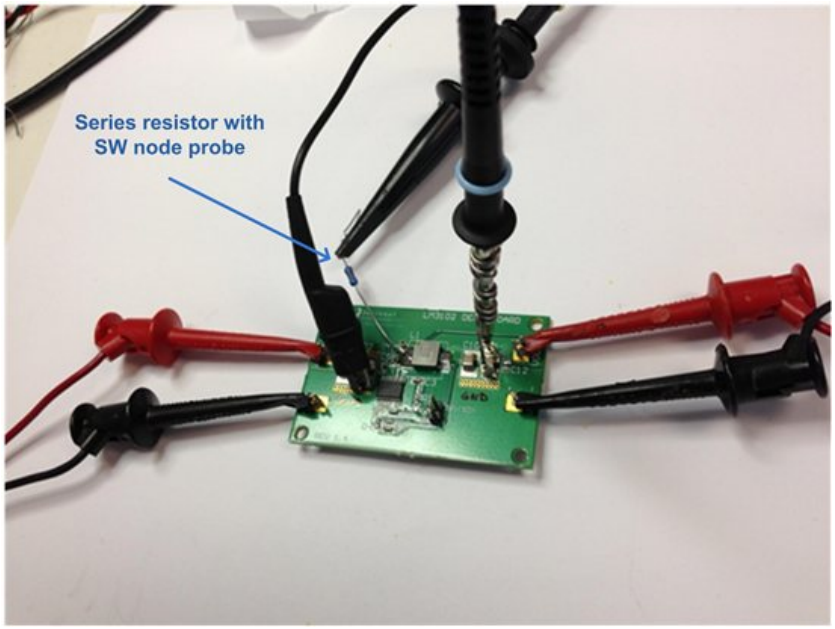
The measurement difference when SW node is measured with VOUT:



The red trace shows the output voltage measurement WHILE the switch node is measured at the same time. Channel 2 shows the output voltage measurement with only VOUT being measured. You can notice that the spikes are much larger if the switch node is measured simultaneously.

Now, if you must measure the switch voltage at the same time as VOUT and don't want to corrupt your output voltage measurement, **there is a trick** (credit to my colleague Alan Martin).

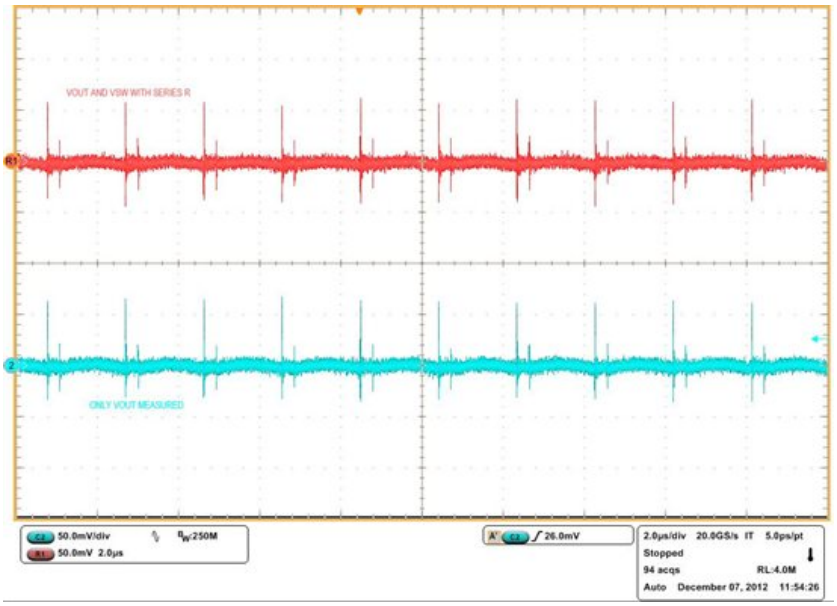
Use a (2k) resistor in series with your switch node probe as such:



Here is the measurement – no substantial difference whether or not the switch node is monitored at the same time as VOUT.

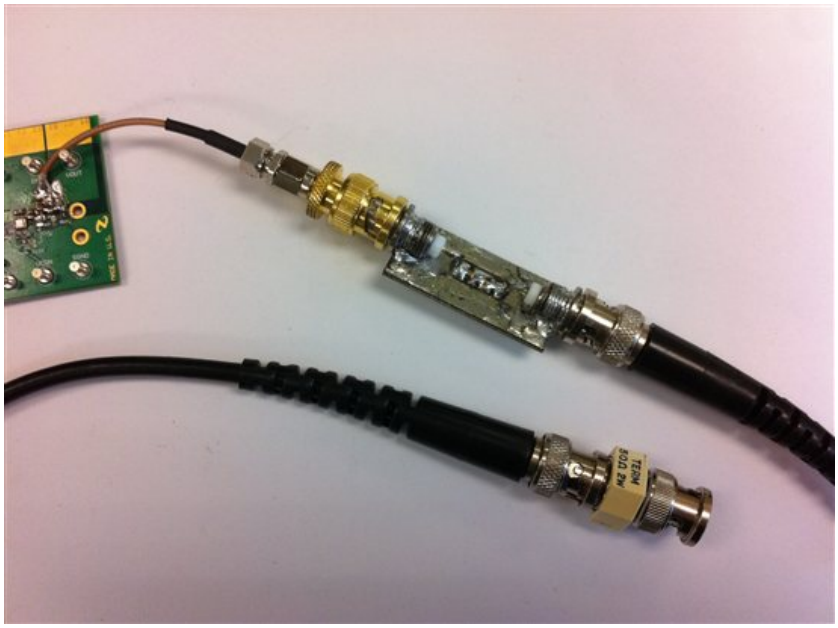
Red trace = SW (with series R) and VOUT measured

Blue(ish) trace = only VOUT measured

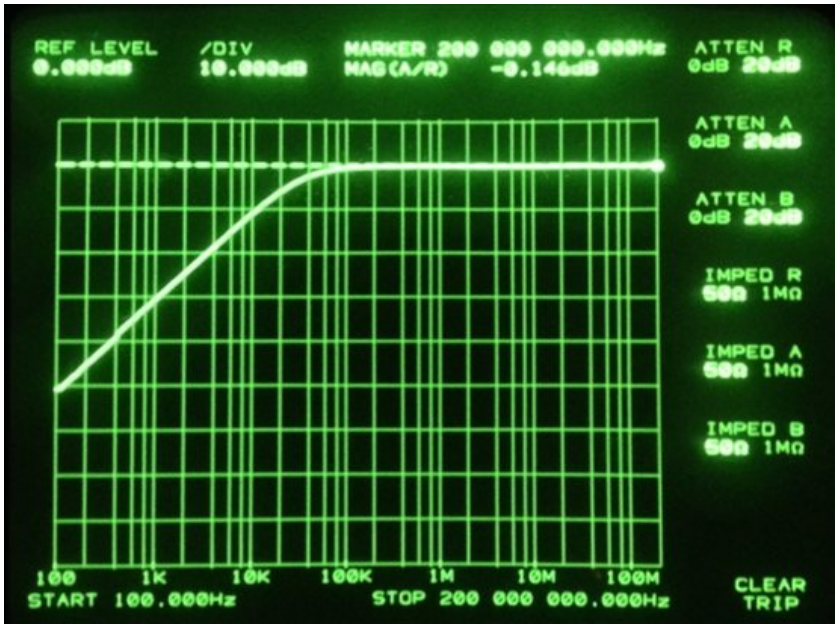


2.2. Probe Sensitivity – Using 10X vs 1X Probes

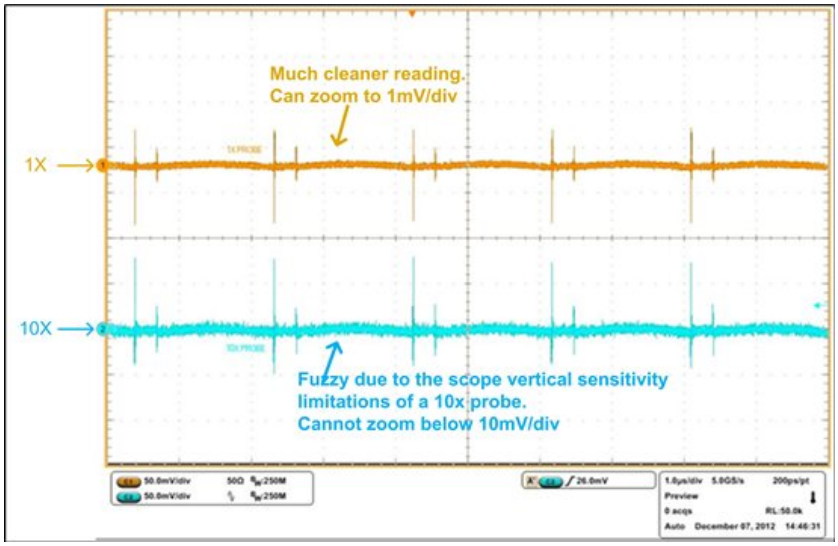
When trying to measure signals in the sub ~10mV range, using a 10x probe will not be appropriate. The sensitivity of the probe is not high enough to have a clean signal reading. A simple, custom made 1x probe can be used for measurements under 10mV. This probe is shown here:



A piece of coaxial cable is laid flat against the board and soldered directly to the output capacitor of the switching regulator. The coaxial cable then connects to a small board which has a series 0.01µF or 0.1 µF AC coupling (DC blocking) capacitor. The other end of the coupling capacitor board connects to a coaxial cable which connects to an external 50Ω termination on the scope channel. One can also use the internal 50Ω termination on the scope. Note that the AC coupling capacitor and the 50Ω termination form a high pass filter with a cutoff frequency at 1 / (2πRC). In this case the capacitor is 0.1µF which results in a cutoff frequency at 31.8kHz. This simple probe is suitable for use for up to 250MHz BW setting on the scope. Here is the frequency response of the probe measured with a network analyzer, showing a flat response up to 200MHz:



Here is a comparison of a Vout ripple measurement using 1x and 10x probes at 250MHz BW:



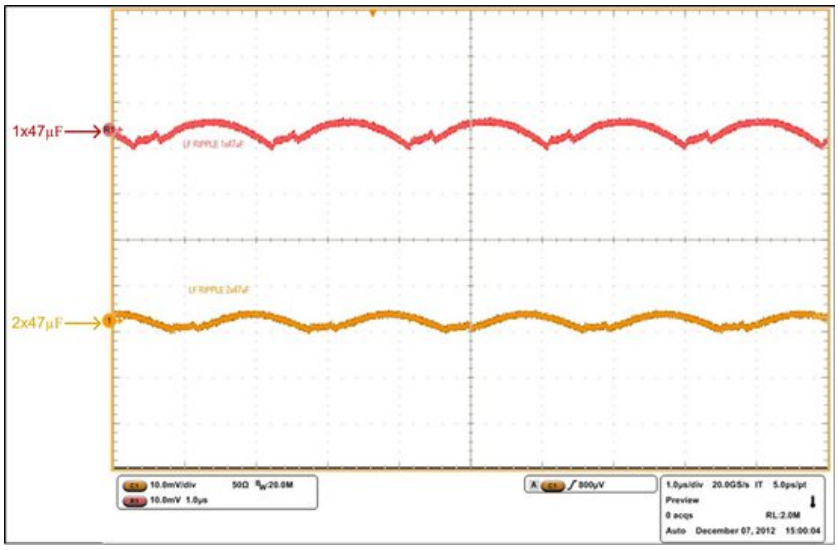
3. Reducing output ripple

3.1. Reducing LF Ripple

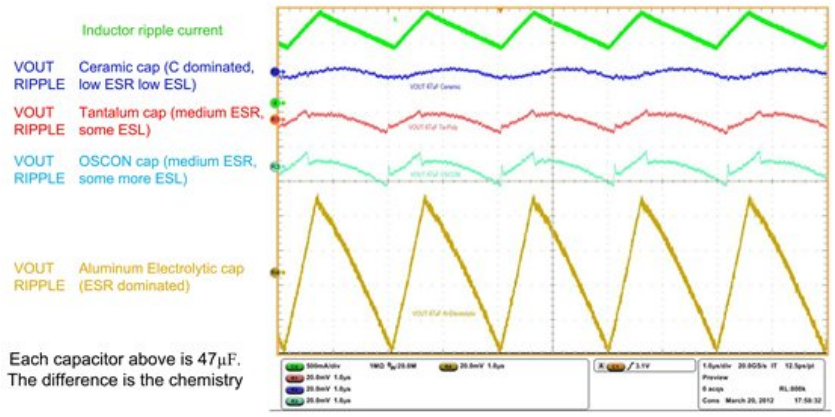
As discussed in section 1.1, the LF ripple voltage on the output of a buck converted is caused by the inductor's ripple current and the output capacitor's impedance at the switching frequency of the regulator. Then, there are two ways to reduce this ripple voltage.

- **Reduce the inductor ripple current.** This can be achieved by increasing the switching frequency (tradeoff is more switching losses, hotter solution and lower efficiency) or by increasing the inductance (tradeoff is larger physical size).
- **Use output capacitor(s) with lower impedance at the switching frequency.** This will be the focus of the discussion here.

Paralleling output capacitors is an effective way to achieve this. Here is an example of LF ripple reduction by using two parallel capacitors instead of one:



Also, you can choose a different capacitor type altogether. Here is an example of achieving different LF ripple by changing the capacitor type (same capacitance value of 47µF and same 20mV/div vertical scale on all voltage waveforms):



As you can see, reducing the LF ripple is fairly straight forward. Place another capacitor in parallel or pick one with lower parasitics.

Reducing the HF noise is the more challenging part.

3.2. Reducing HF Spikes

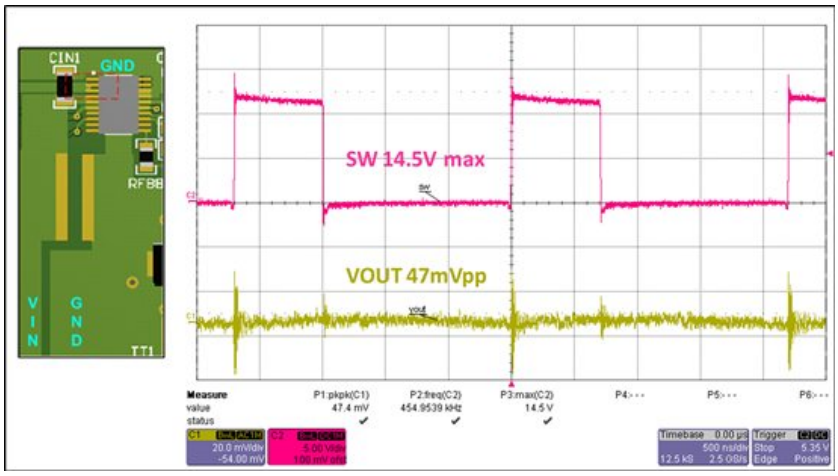
In section 1.2 we discussed the origin of the HF spikes – the edge of the switch node voltage coupling through the parasitic capacitance of the inductor and appearing at the output:

Switch node HF voltage spikes -> Parasitic capacitance of inductor -> Output voltage HF spikes

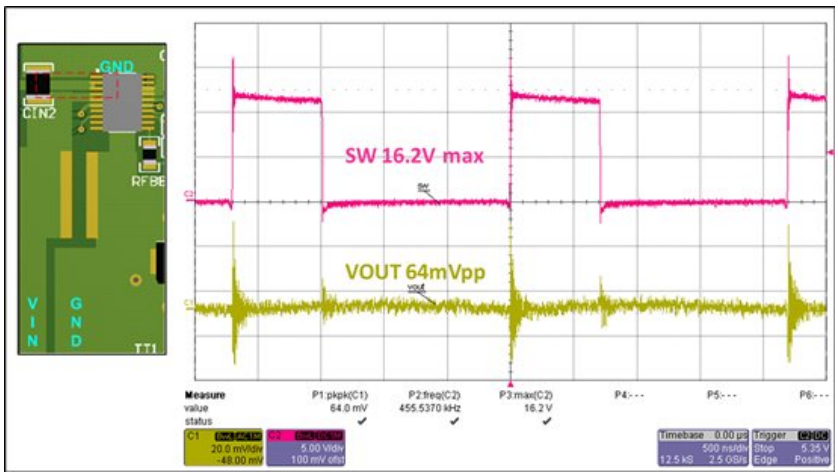
In a practical design, we always have the switch voltage spike above the input voltage because of parasitic inductance in the switching current loop. One approach to reduce the spikes the output is to reduce the spikes on the switch node. This can be done by more careful board layout of the power stage components. In particular, in a buck converter, the placement of the input capacitor terminals with respect to the low side switch GND terminal and VIN is critical. Why is it critical? If you look at the current flow in the buck converter power stage, you will notice that the loop formed by the input capacitor and the power switches has high di/dt switching current going through it each switching cycle. Any parasitic inductance in that path will result in voltage spikes. Making the area of this high di/dt loop as small as possible will result in parasitic inductance that is as small as possible. The benefit – lower switching spikes, lower EMI, and proper operation of the converter.

Here is an example.

This is a 12V input regulator with integrated power MOSFET switches. The input capacitor is placed as close as possible to the IC's input and GND terminals.

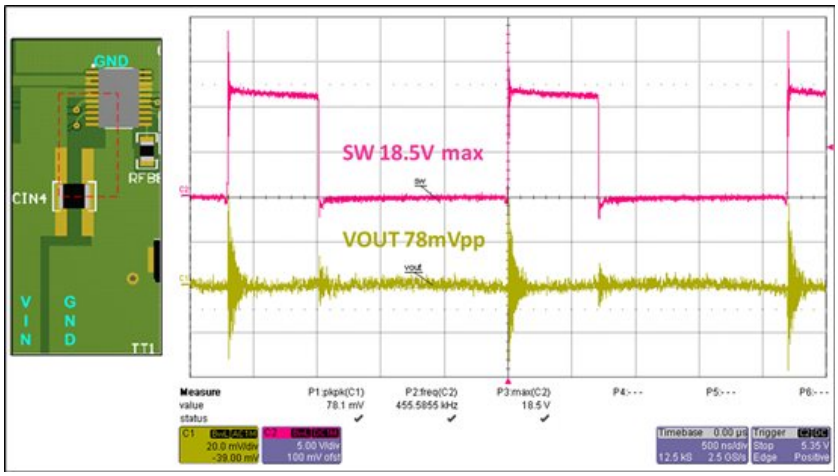


The resulting switch node spike goes to 14.5V and the HF spike on the output is 47mV peak to peak. In this case the input capacitor is very close to the IC. What happens if it is not? Here is an example:



The input cap is now further away from the IC. The high di/dt loop area (red rectangle) is larger. The switch node spike went up to 16.2V. The HF noise on the output also increased, now at 64mV peak to peak.

Let's move the input cap even further and see what happens to the output noise:



Now the switch node spike is at 18.5V and the HF noise on the input went up to 78mV peak to peak. Note that we are using the same board layout, same components, same supply and load conditions in all three cases. The only difference is the input capacitor placement! With the cap far away from the IC we are putting higher voltage stress on the semiconductor component and our output noise increased. In this case we were fortunate that the input voltage is far below the breakdown limits of this IC and the spikes were not able to reach the abs max voltage.

Proper board layout is the first step we should be taking in reducing output noise.

Other ways to reduce the switch node spiking is by using snubbers or slowing down the switch transition edge. Both of these methods come at the cost of converter efficiency. We are not going to discuss these methods here.

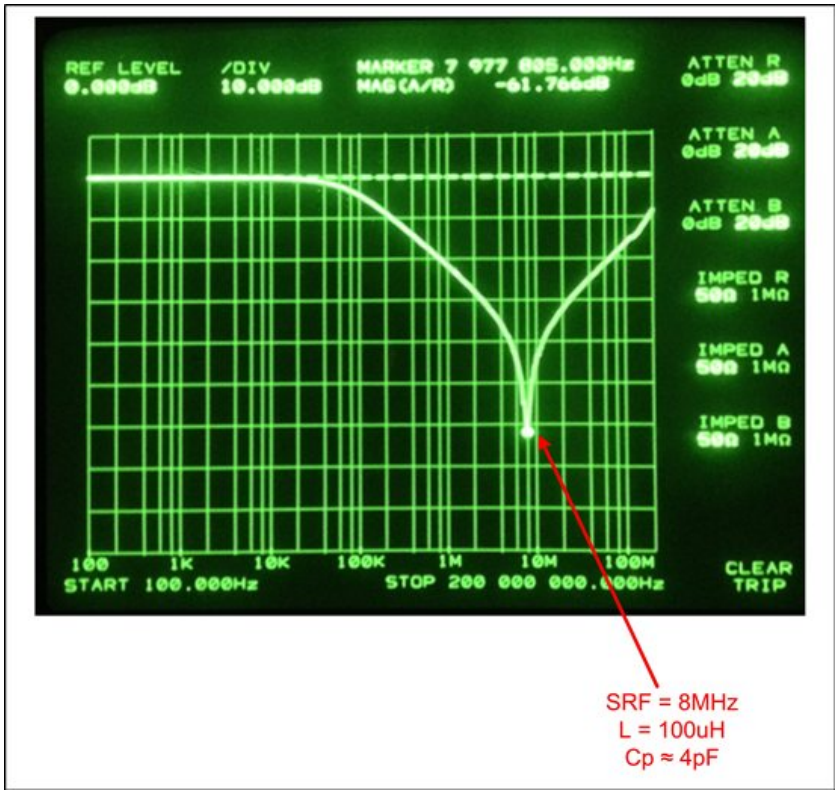
Once we have ensured that the board layout is optimized and the switch node spikes are as low as possible, we can look at reducing the noise coupling path.

Switch node HF voltage spikes -> **Parasitic capacitance of inductor** -> Output voltage HF spikes

As we showed in section 1.2, the coupling path for this HF noise is the parasitic capacitance of the inductor. Reducing HF noise at the output can be achieved by choosing an inductor with lower parasitic capacitance, if you have that choice available. The problem is that the data for the parasitic elements of the inductor may not be available in the manufacturer's datasheet.

If the manufacturer publishes data on self resonant frequency (SRF), you could calculate the parasitic capacitance from that. At the point of self resonance the impedance of the parasitic capacitance and the impedance of the inductance are equal. Then, the parasitic capacitance $Cp = 1 / [(2\pi SRF)^2 x L]$

You could also measure the parasitic capacitance with a network analyzer by looking at the SRF of your inductor. Here is an example:



Once we have ensured that the board layout is optimized and we have chosen an inductor, we can look at the HF spikes at the output and try to filter them out.

Switch node HF voltage spikes -> Parasitic capacitance of inductor -> **Output voltage HF spikes**

The idea is to add capacitance to the output so that the impedance of the output capacitor combination at the ring frequency is low enough. My colleague Alan Martin has done some work on how to filter out the output voltage HF spikes. Here is what he does.

Step 1. Measure the HF noise ringing frequency.

Step 2. Choose a ceramic capacitor that has an impedance null (self resonance) at the ring frequency or higher.

Step 3. Place this small ceramic cap in parallel with your output and measure the ringing again.

Step 4. Add additional small capacitance if necessary to reduce ringing even further.

Another advice Alan has is to plan ahead and reserve locations on the schematic and PCB for these small parallel capacitors. You will not know the capacitor values until after you test the running power supply for ringing noise.

In terms of the capacitor's self resonant frequency, you could get this data from the manufacturer or measure it with a network analyzer. Capacitor manufacturers often have software packages available that would plot different cap characteristics. Here is an example of one such tool with several capacitors' |Z| plotted: