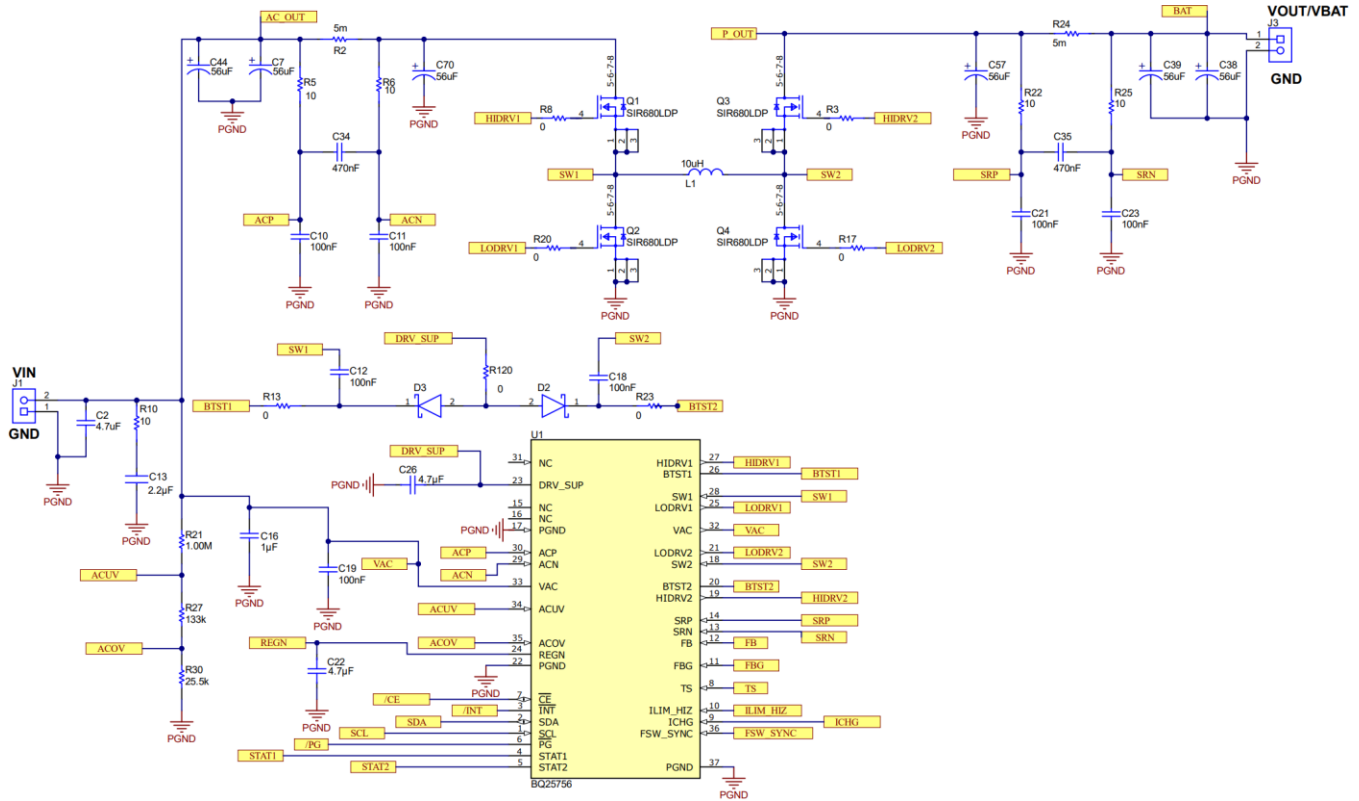
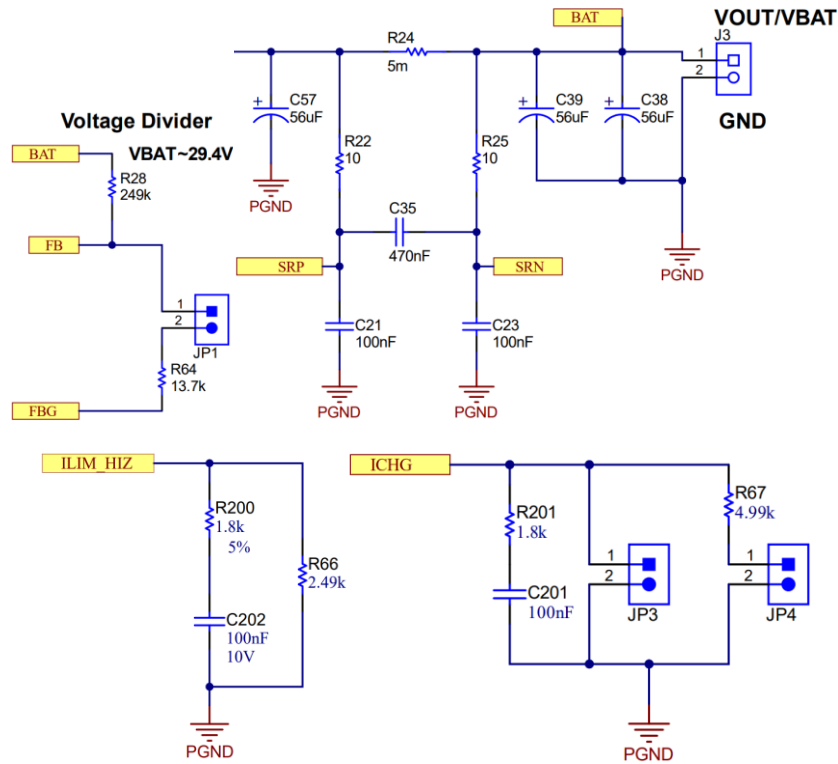


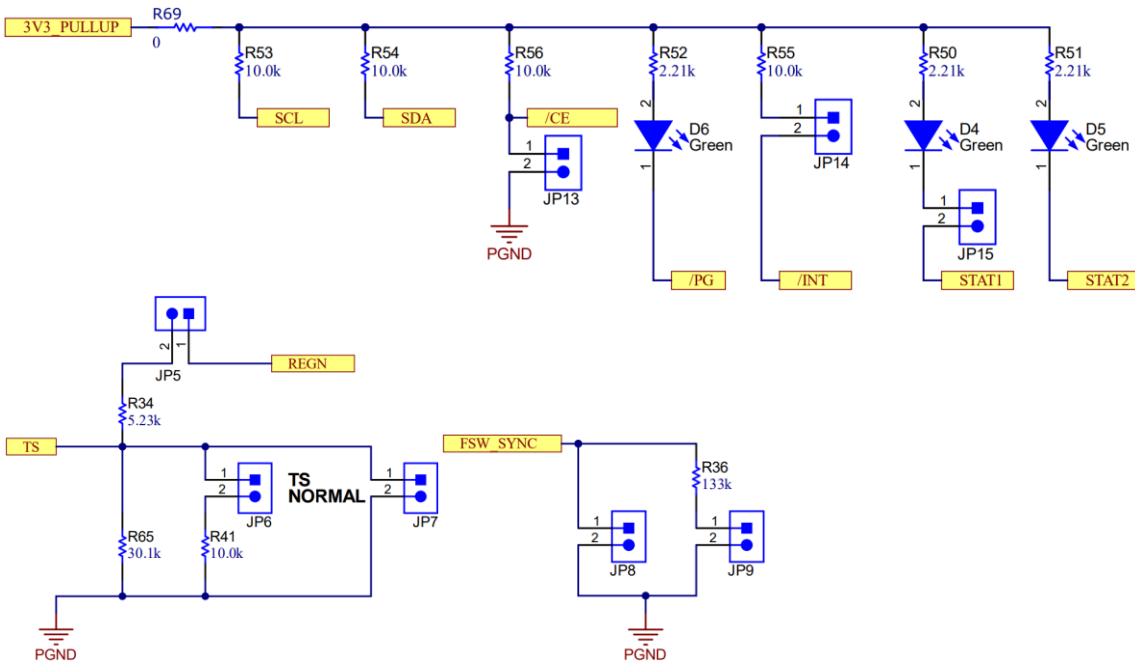
BQ25756 Schematic Checklist



PIN NAME		REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
INPUT POWER- DESIGN CHECKLIST								
Differential input current sensing and current limit setting								
ACP-ACN, ILM_HIZ	30,29,10	Optional	R2(RAC)	0mΩ		5mΩ	Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecture of the charger.	R2(RAC) is not required if input current limit functionality is not needed. Short ACV and ACN to VAC if R2(RAC) is not being used. Refer to section 8.2.2.7 Sense Resistor (RAC_SNS and RBAT_SNS) and Current Programming for choosing the correct resistor value if input current limit functionality is needed.
		Optional	R5,R6		10Ω		Input current sense switching noise and common mode and noise filtering	Can be removed if R2(RAC) is not going to be used.
		Optional	C10,C11		100nF			Can be removed if R2(RAC) is not going to be used.
			C34		470nF		Differential mode noise filtering	Can be removed if R2(RAC) is not going to be used.
REGN	24	Required	C22	4.7μF	4.7μF		Internal LDO output stabilizing capacitor	Placed close to the IC REGN pin.
Converter (Forward Buck Mode) High-Side N-Channel MOSFET gate driver								
HIDRV1	27	Required	Q1				Converter (forward buck mode) active High-Side N-Channel MOSFET	This is also the reverse boost mode High-Side MOSFET.
		Recommended	RHIDRV1	0Ω			Q1 High-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q1 turn-on and turn-off. Don't add a gate to source pull down resistor to Q1.
Converter (Forward Buck Mode) Low-Side N-Channel MOSFET gate driver								
LODRV1	25	Required	Q2				Converter (forward buck mode) active Low-Side N-Channel MOSFET	This is also the reverse boost mode Low-Side MOSFET.
		Recommended	RLODRV1	0Ω			Q2 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q2 turn-on and turn-off.
Buck-boost switching nodes and High-Side MOSFET bootstrap network								
SW1-SW2, BTST1, BTST2, DRV-SUP	28-18, 26,20, 23	Required	L1	2.2μH	10μH	15μH	Converter inductor	SW1 and SW2 should be connected to minimize the inductive path from the IC pin to the Inductor
		Required	D2,D3	-			BTST1/BTST2 Diode-OR	BTST diodes should use a Schottky diode to minimize reverse recovery loss
		Required	C26	4.7μF			Connected between DRV-SUP and PGND	
		Required	C12	100nF			Converter bootstrap capacitor for Q1 High-Side N Channel MOSFET gate driver	Capacitor needs to be placed close to the IC.
		Recommended	R13	0Ω			Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q1 turn-on.
		Required	C18	100nF			Converter bootstrap capacitor for Q4 High-Side N Channel MOSFET gate driver	Capacitor needs to be placed close to the IC.
		Recommended	R23	0Ω			Bootstrap capacitor discharge current limiting resistor F	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q4 turn-on.
Converter (Forward Boost Mode) High-Side N-Channel MOSFET gate driver								
HIDRV2	19	Required	Q3				Converter (forward boost mode) active High-Side N-Channel MOSFET	This is also the reverse buck mode High-Side MOSFET.
		Recommended	RHIDRV2	0Ω			Q3 High-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q3 turn-on and turn-off. Don't add a gate to source pull down resistor to Q3.
Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver								
LODRV2	25	Required	Q4				Converter (forward boost mode) active Low-Side N-Channel MOSFET	This is also the reverse buck mode Low-Side MOSFET.
		Recommended	RLODRV2	0Ω			Q4 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI constraints, add an experimentally derived resistance to slow down the Q4 turn-on and turn-off.
Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver								
ACUV, ACOV	34, 35	Optional	R21		*Ω		Resistor divider from VAC to PGND to program the undervoltage and overvoltage protection.	Refer to section 8.2.2.1 ACUV/ACOV Input Voltage Operating Window Programming of the datasheet for choosing the correct resistor values. Tie ACOV to GND and ACUV to VAC to set the widest operating window
		Optional	R27		*Ω			
		Optional	R30		*Ω			
Input Voltage Detection and Power								
VAC	33,32	Required	C16		1μF		Input voltage noise decoupling capacitor	Place close to the VAC Pin. Short pin 33 and 32 together.



OUTPUT POWER- DESIGN CHECKLIST								
PIN NAME	REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	
SRP,SRN	14, 13	Differential charge current sensing						
		Required	R24	-	5mΩ	-	Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecture of the charger.	The battery sense resistor between SRP and SRN is fixed at 5mΩ. Using a different value is not recommended.
		Required	R22,R25		10Ω		Input current sense switching noise and common mode and noise filtering	
		Required	C21,C23		100nF		Differential mode noise filtering	
ICHG	9	Charge Current Limit setting						
		Optional	R67	0kΩ	5kΩ	100kΩ	Resistor to PGND. This resistor sets the fast charge current	Refer to section 8.3.4.1.1 Charge Current Programming (ICHG pin and ICHG_REG) of the datasheet for choosing the correct resistor values. This pin can be tied to GND if not used.
		Optional	R201		1.8kΩ		RC filter for the ICHG pin	An RC filter is recommended if the ICHG resistor is greater than 5kΩ.
ILIM_HIZ	9	Charge Current Limit setting						
		Optional	R66	0kΩ	5kΩ	100kΩ	Resistor to PGND. This resistor sets the input current limit.	Refer to section 8.3.5.1.1.1 ILIM_HIZ Pin of the datasheet for choosing the correct resistor values. This pin can be tied to GND if not used.
		Optional	R200		1.8kΩ		RC filter for the ILIM_HIZ pin	An RC filter is recommended if the ILIM_HIZ resistor is greater than 5kΩ.
FB, FBG	12, 11	Charge voltage						
		Required	R28		249kΩ		Voltage divider used to adjust output battery regulation voltage. R28 is recommended to be 249kΩ.	$R64 = \frac{(R28 * VFB_REG)}{(Vout - VFB_REG)}$
Required	R64		*kΩ					



COMMUNICATION AND MISC INPUT/OUTPUT SIGNAL- DESIGN CHECKLIST							
PIN NAME	REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
SCL,SDA	1,2	Optional	R53,R54	10kΩ		I2C Open-drain communication input and output Pullup resistors for the open-drain I2C clock and data communication bus. The pull up voltage can be between 1.8V to 5V	The BQ25756 can operate in standalone by setting the charge current and voltage through external resistor on ICHG and FB, FBG pin. The 10kohm resistor is required if host control configuration is desired
STAT1	4	Optional	R50 D4	2.21KΩ -		Open Drain Charge Status 1 Output STAT1 pull up resistor to 3.3V STAT1 LED Indicator	This pin can be left floating if not used
STAT2	5	Optional	R51 D5	2.21KΩ -		Open Drain Charge Status 2 Output STAT2 pull up resistor to 3.3V STAT2 LED Indicator	This pin can be left floating if not used
/PG	6	Optional	R52 D6	2.21KΩ -		Open Drain Active Low Power Good Indicator /PG pull up resistor to 3.3V /PG LED Indicator	This pin can be left floating if not used
/CE	7	Required	R56	10kΩ		Charge Enable pin /CE pull up resistor to 3.3V	/CE must be pulled High or Low, do not leave floating.
TS	8	Optional	R34 R65 R41	*Ω *Ω 103AT-2.10 kΩ		Battery temperature qualification voltage input Resistor divider from REGN to TS to PGND	Refer to section 7.3.4.7.1 JEITA Guideline Compliance in Charge Mode in the datasheet for choosing the correct resistor values.
/INT	3	Optional	R55	10kΩ		Open Drain Interrupt Output /INT pull up resistor to 3.3V	This pin can be left floating if not used
FSW_SYNC	36	Required	R36	40kΩ	200kΩ	Switching Frequency and Synchronization Input Used to set the nominal switching frequency	A clock can be provided on this pin in the range of 200 – 600kHz for switching frequency synchronization. R36 can also be calculated with the following formula $R_{FSW} = \frac{1}{10 \times (f_{SW} \times 5 \times 10^{-12} - 500 \times 10^{-9})}$
PGND	17	Required	-	-	-	GND Tie this pin to PGND	Tie this pin to PGND
PGND	37&22	Required	-	-	-	Power Ground Return IC Ground Return	
NC PINS	31 15 16	Required	-	-	-	NC PINS Leave this pin NC, do not tie to ground Leave this pin NC, do not tie to ground Leave this pin NC, do not tie to ground	

BQ25756 Layout Guidelines

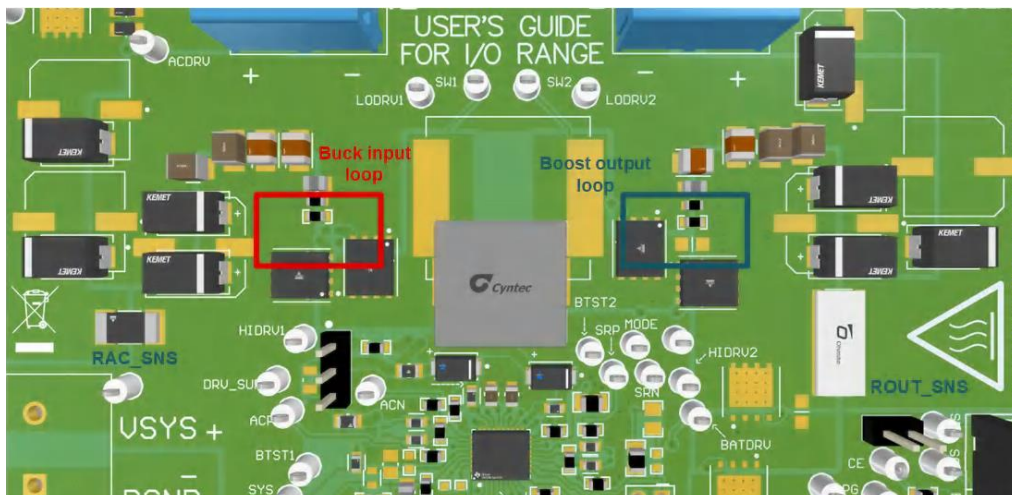
Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

Components	Function	Impact	Guidelines
Buck high side FET, Buck low side FET, input capacitors	Buck input loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the input of the buck. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place input ceramic capacitors close to the switching FETs.
Boost low side FET, boost high side FET, output capacitors	Boost output loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the output of the boost. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place output ceramic capacitors close to the switching FETs.
Sense resistors, Switching FETS, inductor	Current path	Efficiency	The current path from input to output through the power stage and sense resistors have low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2-A per via for a 10-mil via with 1oz. copper thickness.
Switching FETs, inductor	Power stage	Thermal, efficiency	The switching FETs and inductor are the components with highest power loss. Allow enough copper area for heat dissipation. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
DRV_SUP, BTST1, BTST2, capacitors	Switching FET gate drive	High frequency noise, parasitic ringing, gate drive integrity	The DRV_SUP capacitors are used to supply the power to drive the low side FETs. The BTST capacitors are used to drive the high side FETs. It is recommended to place the capacitors as close as possible to the IC.
LODRV1, LODRV2	Low side gate drive	High frequency noise, parasitic ringing, gate drive integrity	LODRV1 and LODRV2 supplies the gate drive current to turn on the low side FETs. The return of LODRV1 and LODRV2 is PGND. As current take the path of least impedance, a ground plane close to the low side gate drive traces is recommended. Minimize gate drive length and aim for at least 20 mil gate drive trace width. Routing HIDRV1/HIDRV2 next to LODRV1/LODRV2 is not recommended.

HIDRV1, HIDRV2, SW1 (pin trace), SW2 (pin trace)	High side gate drive	High frequency noise, parasitic ringing, gate drive integrity	HIDRV1 and HIDRV2 supplies the gate drive current to turn on the high side FETs. The return of HIDRV1 and HIDRV2 are SW1 and SW2, respectively. Route HIDRV1/SW1 and HIDRV2/SW2 pair next to each other to reduce gate drive parasitic inductance. Minimize gate drive length and aim for at least 20 mil gate drive trace width.
Current limit resistors, FSW_SYNC resistor	IC programmable settings	Regulation accuracy, Switching integrity	Pin voltage determines the setting for input current limit, output current limit and switching frequency. Ground noise on these could lead to inaccuracy. Minimize ground return from these resistors to the IC ground pin.
Input (ACP, CAN) and output (SRP, SRN) current sense	Current regulation	Regulation accuracy	Use Kelvin-sensing technique for input and output current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs, away from switching nodes.
Input (ACUV), and output (FB, VO_SNS) voltage sensing	Voltage sense and Regulation	Regulation accuracy	ACUV divider sets internal input voltage regulation in forward mode (V_{ACUV_DPM}). FB divider sets battery voltage regulation in forward mode (V_{FB_ACC}). Route the top of the divider point to the target regulation location. Avoid routing close to high power switching nodes.
Bypass capacitors	Noise filter	Noise immunity	Place lowest value cap+B7:D12acitors closest to the IC

Layout Example:

Based on the above layout guidelines, the buck-boost PCB layout example top view is shown below including all the key power components.



For both input and output current sensing resistors, differential sensing and routing method are suggested and highlighted in the Image below. Use wide trace for gate drive traces, minimum 20 mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad.

