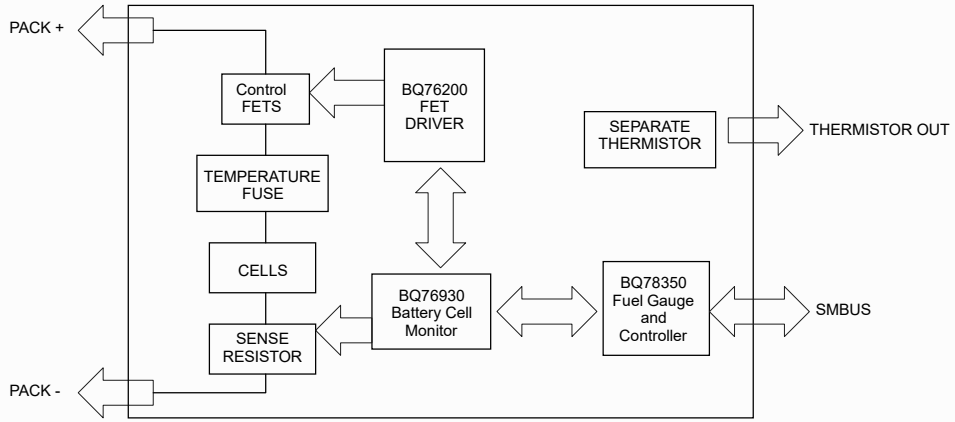
SCHEMATIC: FUEL GAUGE BOARD	
SHEET	**DESCRIPTION**
01	TITLE AND BLOCK DIAGRAM
02	BQ76930 MONITOR
03	BQ78350-R1A GAUGE AND BQ76200 DRIVER

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	X1	INITIAL RELEASE	15 Sept 23	C. STANFIELD

BLOCK DIAGRAM



DASH NO.	NEXT ASSY	USED ON	QTY NEXT ASSY	QTY FINAL ASSY
	BA110020	BA200010		

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND AFTER PLATING TOLERANCES ARE:

FRACTIONS	DECIMALS	ANGLES
± 1/32	0.XX ± .03 0.XXX ± .010	± 1/2

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

BREAK SHARP EDGES .010, INTERNAL RADIUS 0.015 MAX, UNLESS OTHERWISE SPECIFIED

125 MACHINED SURFACE TEXTURE UNLESS OTHERWISE NOTED

CONTRACT NO.

	APPROVED	DATE
DRAWN	Curt Stanfield	15 Sept 23
CHECKED		
ENVIRON		
MFG		
MATERIALS		
SECURITY		
QUALITY		
RELIABILITY		
STRESS		
DES ENGR		
PROJ ENGR		
EXPORT		

ENERGY SYSTEMS
HUNT VALLEY, MARYLAND USA

TITLE

BMS, 76930 Battery

SIZE	CAGE CODE	DWG NO.	REV
B	0RTN5	BA110020	-

SCALE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

BMS Design: BQ76930

Layout Guidelines for BQ76930:
1. Match traces going to sense resistor (0.01 Ohms)
2. VCx filters, Vdd, AVDD caps should be placed close to the device.
3. Separate the device ground planes from the high current paths. Filter Capacitors should reference the low current ground path or device Vss
4. In a stack configuration, Rctrd and Rctrc should be placed closer to the lower device CTRD and CTRC pins.
5. Charge and discharge FET gate resistors should be placed near the FET's.
6. D1 BAT diode should be placed near B+ tap

Power Supply to REGSRC

Design Considerations:
1. For High current discharge applications, Schottky diodes can be added to cell sense lines.
2. Is there a standby current (leakage current) consideration?
3. We have said that the 50mA (5mA) balancing current is enough for the Gavia Application. Would other applications or battery chemistries need higher balancing current? If yes, then balancing MOSFETS would be necessary.
4. Note: The Pinout on the PCB connector is not the same as previous Gavia on the PCB.
5. The output of the Gavia Charger is rated as 32v-35v. However, per the power manager document the minimum voltage applied to the V Charge port on the gavia sub that will allow the power manager to connect the packs to the charge source is 24v. So the most extreme low case for the rising edge would be 0v to 24v, but the much more normal case would be 0v to 32-35v. The process of charging a Gavia pack initial jump is 24 (vehicle low voltage cutoff) to 27.5v

Activate Boot Switch from Charger

Part Number Ordering: 2.5V LDO
BQ7693000DBT (No CRC)
BQ7693000DBTR (No CRC)

Boot Switch Connected to TS1

TS1 is used to boot the part from SHIP mode to NORMAL mode. A rising edge is required to boot above 1V. Max voltage is 3.6V after POR (Power on Reset) and 5V before. TS1 causes a temperature reading anomoly during boot.

Note: NTC1 Should be configured to measure the FETs and NTC2 Should be used for the cells.

Note: Load Detect will not work with external high-side FET controller because it uses the CHG pin for this function. If low standby current is required, the path from VBatt to GND through CHG needs to be addressed.

Note: Current Shunt, equivalent to 0.010mOhms. Would be better at 2 or 5mOhms.

Wires Soldered to PCB

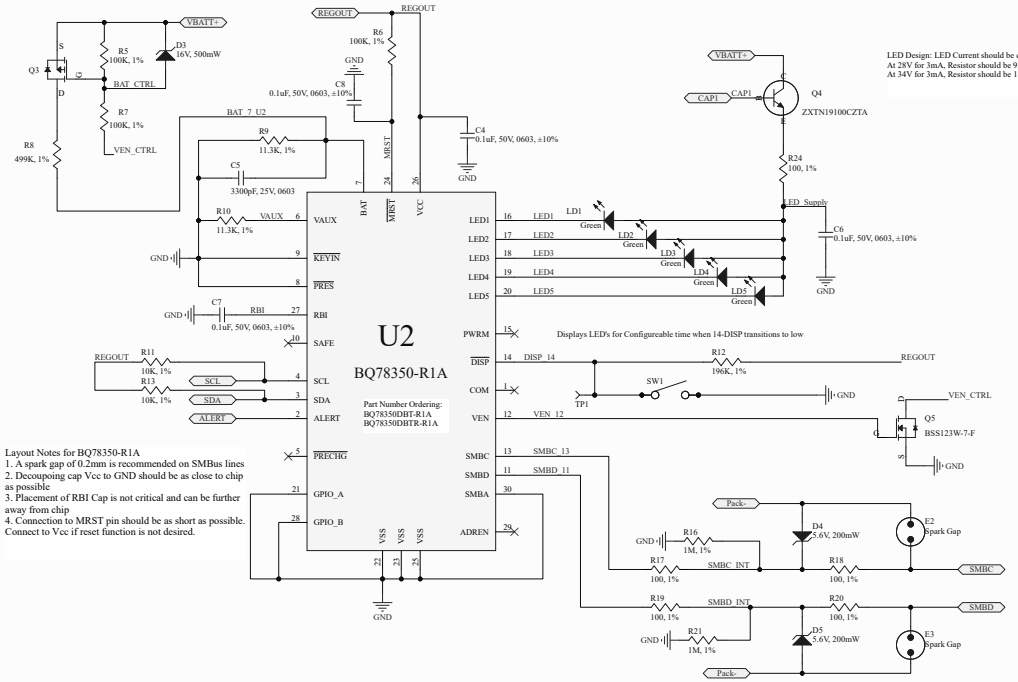
Note: The NTC should be placed near the negative terminal for heat conduction.

SIZE	CAGE CODE	DWG NO.	REV
C	0RTN5	BA110020	-
SCALE	BMS 76930 BATTERY	Sheet 2 of 3	

DWG NO BA110020
SHT 2
REV -

IRAD BMS Design: BQ78350 and BQ76200

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



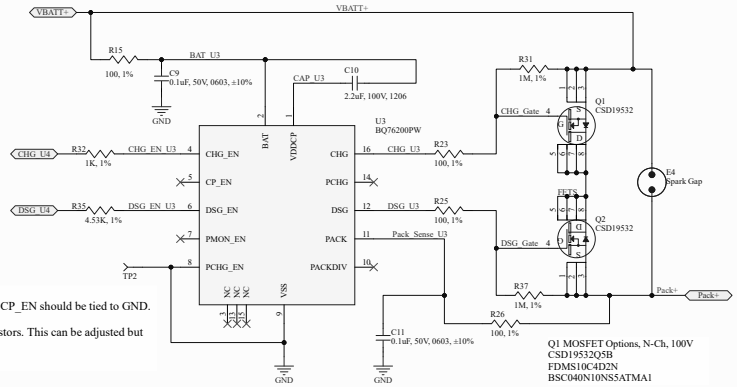
LED Design: LED Current should be designed for 3mA
At 28V for 3mA, Resistor should be 9.3k Ohms
At 34V for 3mA, Resistor should be 11.3k Ohms

Displays LED's for Configureable time when 14-DISP transitions to low

Future Design Note: When the pack is reconfigured/redesigned, the push-button switch for the battery status display should be placed near the connector so the button design can be integrated into the cover for the wires to allow for button pushes.
Possibly similar to R-667823 or EVQ-P7D01P

Layout Notes for BQ78350-R1A
1. A spark gap of 0.2mm is recommended on SMBus lines
2. Decoupoing cap Vcc to GND should be as close to chip as possible
3. Placement of RBI Cap is not critical and can be further away from chip
4. Connection to MRST pin should be as short as possible. Connect to Vcc if reset function is not desired.

Note: If the height of C10 is an issue, KGM31HR72A225KL from Kyocera is only 60 mils (1.52mm) tall. KAM21KR72A105KU from Kyocera is 55 mils (1.4mm) tall and can be doubled up to use at 1uF.



Layout Guidelines for BQ76200:
1. CPack, CBat and CVDDCP should all be close to the chip.
2. Chip should be on low power ground plane that connects at single point to high power ground plane.

Design Notes BQ76200:
1. If the charge pump does not need to be pre-activated, then CP_EN should be tied to GND.
2. Leave PACKDIV floating if not used
3. FET Turn-Off time is determined by the Gate-Source Resistors. This can be adjusted but will strain the chip the lower it gets.

Q1 MOSFET Options, N-Ch, 100V
CSD19532Q5B
FDMS10C4D2N
BSC040N10NS5ATMA1

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C	0RTN5	BA110020	-
SCALE	BMS, 76930 Battery	Sheet 3 of 3	

DWG NO BA110020
SHT 3
REV -