Application Report

PCB Thermal Design Tips for Automotive DC/DC Converters

ABSTRACT

Thermal management is one of the most important aspects of designing power supplies. This is especially true in the automotive environment where converters must operate in high ambient temperatures and enclosed spaces. This paper provides guidance to the designer that will make the task of thermal management proceed somewhat more smoothly.

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Trademarks

1 Introduction

Thermal management is one of the most important aspects of designing power supplies. This is especially true in the automotive environment where converters must operate in high ambient temperatures and enclosed spaces. This paper provides guidance to the designer that will make the task of thermal management proceed somewhat more smoothly.

2 The Goal of Thermal Management

The goal of thermal management is to keep the maximum junction temperature of the device at or below a safe value. This safe value is stated in the data sheet under the "Absolute Maximum" specification section as shown in the example of Figure 2-1.

7.1 Absolute Maximum Ratings

Over the recommended junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
	VIN to PGND	–0.3	40	V
	EN to AGND	–0.3	40	V
	SYNC/MODE to AGND	–0.3	6	V
	VOUT_SEL and RT to AGND	–0.3	5.5	V
	$\overline{\text{RESET}}$ to AGND	–0.3	16	V
	FB to AGND (Fixed VOUT mode)	–0.3	16	V
	FB to AGND (Adjustable VOUT mode)	–0.3	5.5	V
	AGND to PGND	–0.3	0.3	V
	SW to PGND for transients of less than 10ns	-6	40	V
	BOOT to SW	–0.3	5.5	V
	VCC to AGND	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 2-1. Maximum Junction Temperature Specification

This will usually be 125°C or 150°C for an automotive qualified device and is called $T_{J\text{-}max}$. A good thermal design will keep the converter temperature below this value under all operating conditions.

3 Junction Temperature Calculation

Equation 1 shows the key to calculating junction temperature. The next sections detail what each of the terms mean and how they are determined.

$$T_J = T_A + P_D \times \theta_{JA} \quad (1)$$

3.1 Regulator Junction Temperature (T_J)

T_J is the average temperature of the semiconductor die when the converter is operating. The power dissipated within the regulator will cause the junction temperature to rise above the ambient within which it is operating. The thermal design must keep this temperature below $T_{J\text{-max}}$. The maximum safe junction temperature is fixed at the time that the regulator is designed, and cannot be changed. Considerations of current density in the metallization on the IC die, place limitations on the maximum junction temperature. Higher temperatures require heftier metal interconnects and therefore a larger and more expensive regulator. Exceeding $T_{J\text{-max}}$ will usually not cause damage, since most regulators incorporate thermal shutdown protection to shut off the converter when the temperature exceeds $T_{J\text{-max}}$. The user must decide how far below the $T_{J\text{-max}}$ specification is reasonable for the application. Many companies have general guidelines for the maximum junction temperature they allow for a given circumstance; and of course these must be followed. The guideline is simple: the lower the junction temperature the higher the reliability of the device. Calculations of reliability versus time and temperature are possible, but beyond the scope of this discussion. Conversely, selecting too low a temperature will limit the maximum ambient temperature or the power dissipation that can be achieved in the application; see Equation 1.

3.2 Ambient Temperature (T_A)

The maximum ambient temperature is fixed by the application environment. With both T_A and $T_{J\text{-max}}$ set, the designer has only the power dissipation and thermal resistance to work with to meet the temperature specifications. The lower the maximum ambient temperature, the easier it is to satisfy $T_{J\text{-max}}$ for a given regulator. Higher ambient temperatures force the designer to use a regulator with higher efficiency, larger packages with better thermal resistance, or both. Lowering the ambient temperature by using forced air cooling is another option, but may not be practical. Both options result in a more expensive and larger overall solution.

3.3 Power Dissipation (P_D)

The power dissipation is calculated with Equation 2.

$$P_D = V_{OUT} \times I_{OUT} \times \frac{1 - \eta}{\eta} \quad (2)$$

The efficiency of the converter is represented by η. As previously mentioned, the efficiency is somewhat in the control of the designer. The maximum output power ($V_{OUT} \times I_{OUT}$) is set by the application, but there is some opportunity to select a device with good efficiency. Obviously, the higher the efficiency the lower the power dissipation. Lower input voltages tend to improve the efficiency of a regulator. As an example, if the output of a DC/DC converter is 3.3 V, then using a 5-V rail to power the converter (rather than something higher like 12 V) will help to improve efficiency. Switching frequency also has a big impact on the losses in the converter. Selecting a lower switching frequency will reduce the frequency dependent losses. The trade-off here is that a larger LC filter will be needed, increasing the solution size and possibly cost. Reducing the power loss has other benefits for the system as well. With less heat being generated, the other components will experience a cooler ambient, helping to improve overall reliability. The efficiency used in the equation is found in the data sheet or measured under actual operating conditions. In some cases the published efficiency includes the losses in the inductor. These can be approximately accounted for if the inductor resistance is known, using Equation 3.

$$P_{inductor} \approx I_{OUT}^2 \times R_{inductor} \quad (3)$$

Simply subtract Equation 3 from Equation 2 to get the approximate power loss in the regulator. Although the total inductor power dissipation consists of both AC and DC losses, for the purposes of this example only the DC

power loss is accounted for, as represented by the stated resistance of the inductor. If a more accurate loss model for the inductor is needed, the inductor manufacturer should be consulted.

Usually the efficiency found in most data sheets will be taken at an ambient temperature of 25°C. The efficiency at higher temperatures will be somewhat lower. Many times the regulator manufacturer can provide efficiency data at elevated temperatures to aid the user in making power dissipation calculations. In any case the published curves can be used to estimate the efficiency under the specific user conditions and this number can be reduced by a point or two, to account for higher temperature operation. Table 3-1 gives a guide as to how regulator operating conditions affect efficiency and can be used to aid in estimating efficiency under conditions not given in the data sheet.

Table 3-1. Variation of Efficiency With System Parameters

Condition	Effect on Efficiency
Input Voltage	Decreases with increasing voltage
Output Voltage	Increases with increasing voltage
Switching Frequency	Decreases with increasing frequency
Ambient Temperature	Decreases with increasing temperature

3.4 Thermal Resistance (θ_{JA})

This metric is the total thermal resistance from the junction of the device to the ambient air. It has dimensions of °C/Watt, and you can think of it as electrical resistance. In this case the power dissipation acts like the *current* and the temperature drop as the *voltage*. Multiplying the power dissipation by θ_{JA} gives the temperature change from ambient to the junction. That is basically what Equation 1 demonstrates. The lower the thermal resistance, the lower will be your junction temperature for a given power dissipation and ambient temperature. The real goal of thermal management is to get the lowest possible θ_{JA} for a given set of application restraints.

The metric, θ_{JA} is the most important parameter in Equation 1 and the most difficult to calculate, estimate, or measure.

The remainder of this discussion looks at many of the factors that affect thermal resistance to estimate this important parameter.

3.4.1 Thermal Metrics

Most data sheets include a value for θ_{JA}, along with other information, in the thermal characteristics table. Figure 3-1 shows an example from the automotive qualified *LM636x5-Q1 3.5-V to 36-V, 1.5-A, and 2.5-A Automotive Step-down Voltage Converter Data Sheet*.

THERMAL METRIC (1)		LM636x5 DRR0012 (WSON) 12 PINS	LM636X5 HTSSOP (PWP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	47.4	43.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	35.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	18.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	18.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the ***Maximum Ambient Temperature*** section.

Figure 3-1. Typical Thermal Metrics From Device Data Sheet

The value of θ_{JA} (or $R_{\theta JA}$) given in this table is taken under very specific conditions, that do not necessarily apply to the real application. Typically, the value of θ_{JA} will be quite a bit larger than what can be achieved with proper

PCB layout. Therefore the table value cannot be used for design purposes; its main use is in comparing between different regulators and different packages. As will be shown, the other metrics in the table can be very helpful. For packages with a Die Attach Paddle (DAP) the value of θ_{JC} (or $R_{\theta JC(bott)}$) for the bottom of the device is also important. Equation 4 shows how to use this parameter.

$$\theta_{JA} = \theta_{JC} + \theta_{SA} \tag{4}$$

In this equation, θ_{SA} is the thermal resistance from the heat sink to the ambient air. Usually, the value of θ_{SA} is not known and θ_{JA} is the true value of interest (Equation 1). However, some calculator tools require θ_{JC} when estimating the overall thermal performance. Also, a smaller value of θ_{JC}, will help to reduce the overall θ_{JA}.

You will notice in the table that there are those metrics termed as "thermal resistance" and those termed as "thermal parameters". The thermal *resistance* values are defined and measured assuming that all of the power flows in the path indicated by the metric name. As an example, with θ_{JC} (or $R_{\theta JC(bott)}$) it is assumed that all the power is flowing from the junction to the bottom DAP. These metrics are most important when designing the thermal management of the overall system from the junction to the ambient environment. Thermal *parameters* are defined and measured assuming that only some of the power is flowing in the path indicated by the metric name. As an example, the parameter Ψ_{JT} is used to calculate the junction temperature by measuring the top case temperature with a thermocouple or thermal camera. This calculation is discussed in Section 8.1. Essentially the "Ψ" parameters are used when evaluating and testing the system based on measurements. The "θ" resistances are used when designing or calculating the thermal performance of the system. Suppose a heatsink is used on the top of the package, rather than using the PCB through the bottom DAP connection. A safe assumption would be that most, if not all, of the heat is going through the top heatsink. In this case use the resistance, $R_{\theta JC(top)}$, rather than the Ψ_{JT} parameter to calculate the overall performance. Even though both the metrics indicate heat flow from "junction" to "top", the correct value to use would be the $R_{\theta JC(top)}$. The parameter Ψ_{JB} can also be useful. A measurement of the board temperature, T_B, could be used to estimate T_J using Equation 6. See *Semiconductor and IC Package Thermal Metrics* to get a much more detailed explanation of thermal metrics and how they are measured and used.

4 Package Type

The type of package has a major impact on the thermal performance. In this discussion packages are divided into two major groups: those that have a Die Attach Paddle (DAP) on the bottom of the package and those that do not. Of course there are many more distinctions between packages and many other important features, but this difference is the most important from a thermal perspective. As an example, the LMR33630 is available in both an HSOIC and *flip-chip* (or HotRod™) QFN package, as Figure 4-1 shows.

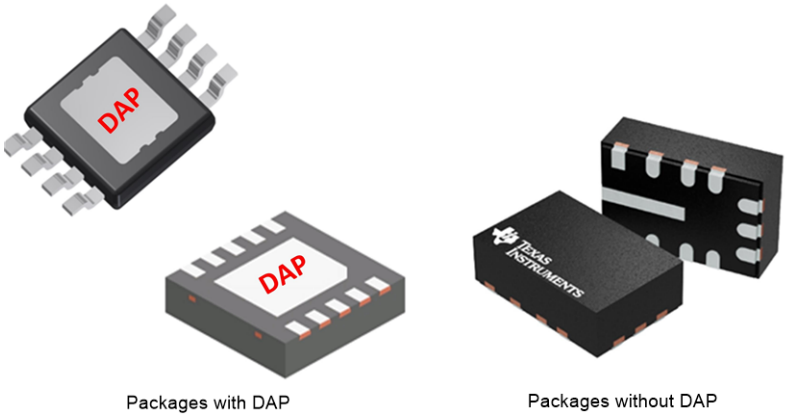

Figure 4-1. LMR33630-Q1 Package Variants

For this family of devices, Figure 4-2 shows the difference in θ_{JA} between the two packages. The values are based on a JEDEC standard board, and it is easy to see that the HSOIC package has a much lower thermal resistance. The tradeoff is also obvious; the HSOIC package is over three times the area of the flip-chip QFN in this example. A QFN package also requires more care in assembly to the PCB than a larger package with completely exposed pins. Figure 4-3 and Figure 4-4 help to explain the difference in thermal resistance between these two example packages. The HSOIC has a large metallic "slug", the DAP, attached directly to the regulator die. The DAP, in turn, is soldered to the PCB copper heat sink. This provides a very low resistance path from the die (heat generator) to the heat sink and outside ambient. As a result, about 80% of the heat flows through the DAP, 20% through the leads, and very little through the plastic. This makes the copper under the DAP (usually electrical ground) very effective in removing the heat from the package.

With the flip-chip package the back-side of the die (or substrate) is facing up, away from the PCB. The only metallic connection to the PCB is through the package pins. This forces the heat to flow through a very restricted path and increases the effective thermal resistance. It also indicates that the copper paths to the pins should be as substantial as possible to help act as a heat sink. For a DC/DC converter the VIN, GND, and SW pins are the most effective in removing the heat, and should be made wide.

Of course these are only two examples of the types of power packages available to the designer. TI offers many package types that provide the advantages of both good thermal performance and small size. An example is the automotive qualified LM63635-Q1. This device is offered in a small 3.00-mm by 3.00-mm WSON package with a DAP; giving comparable performance to a much larger package.

Remember that the JEDEC standard board overemphasizes the difference between the flip-chip QFN and the HSOIC. In many real applications, values of overall θ_{JA} can be made comparable between these two packages.

For the flip-chip QFN, more PCB copper area will be required, than for a package with a DAP. In any case, as previously stated, the values of θ_{JA} given in the table would not be used for design purposes.

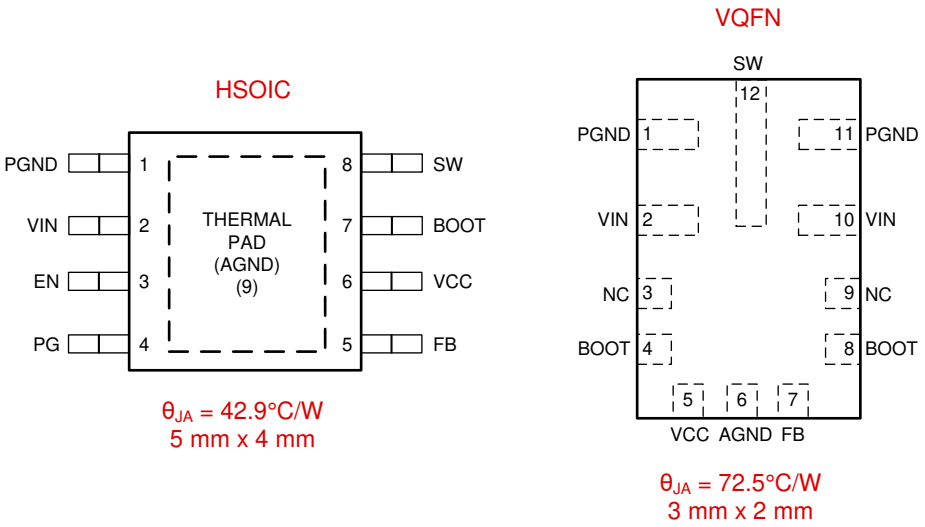

Figure 4-2. Comparison of HSOIC and VQFN Performance

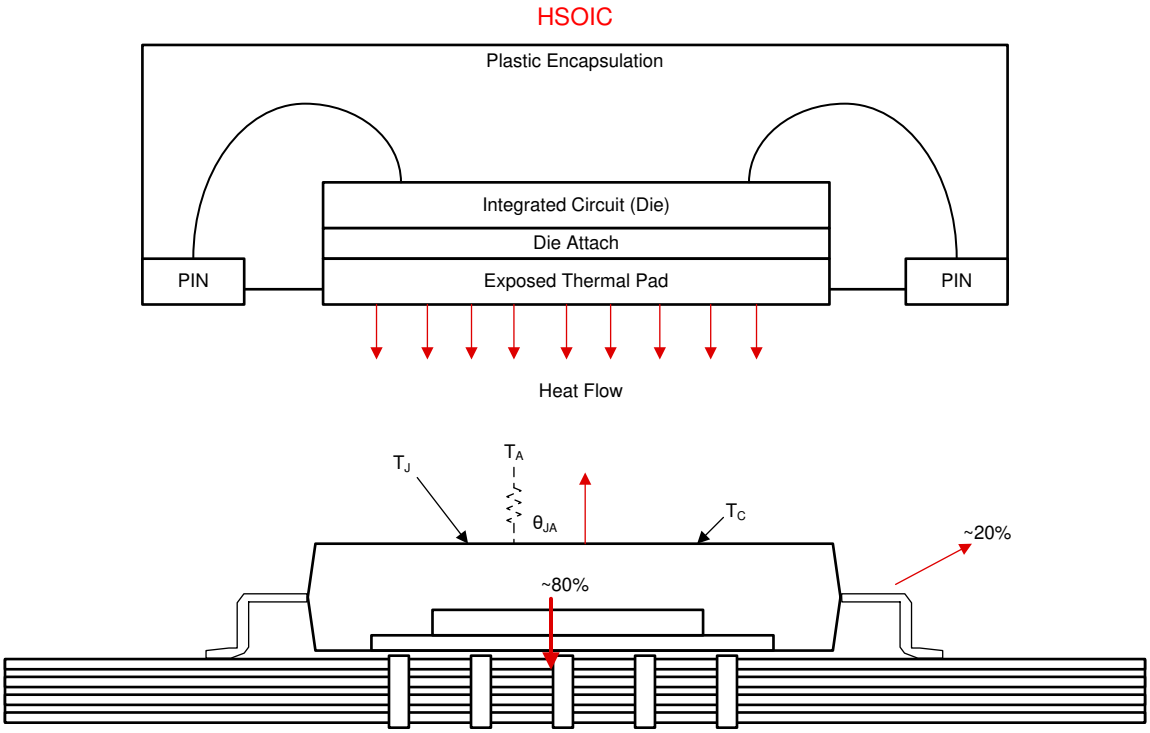

Figure 4-3. Typical Heat Flow in HSOIC Package

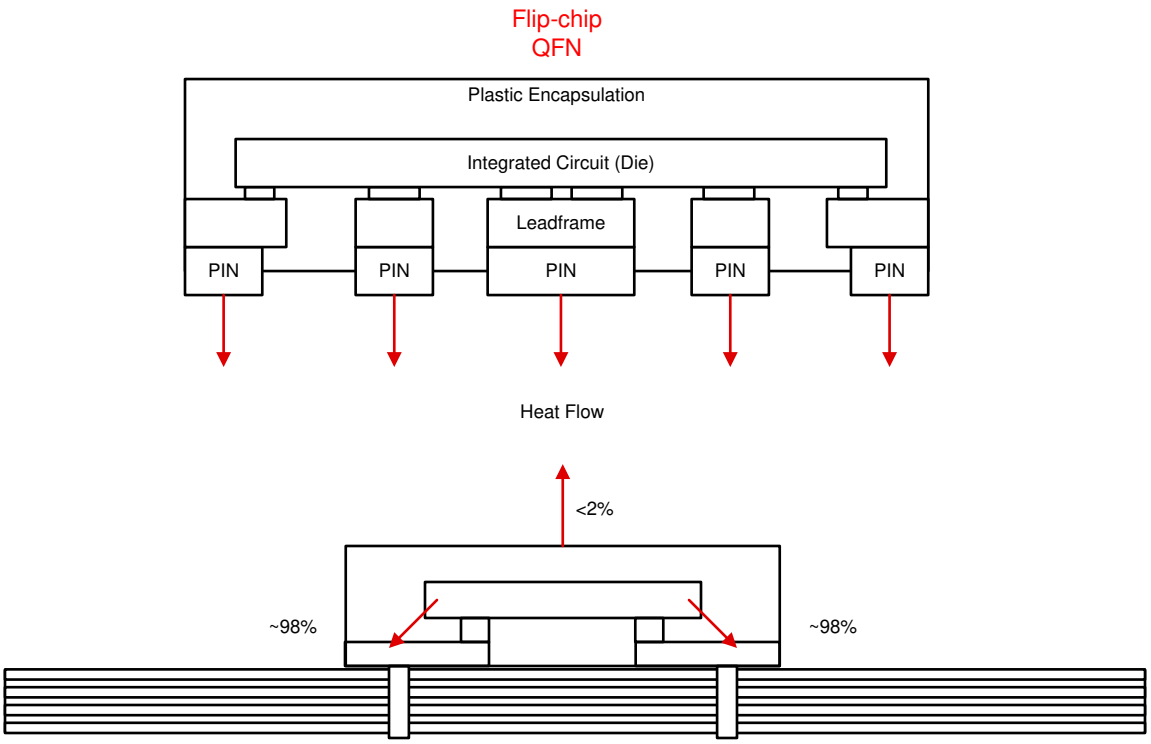

Figure 4-4. Typical Heat Flow in VQFN Package

5 PCB Copper Heat Sink

As mentioned, the PCB copper planes act as heat sinks for the regulator. The area and thickness (weight) of the copper is important. Most of the heat will be dissipated to ambient through the layer that is on the same side as the converter. The DAP must be firmly soldered directly to this plane providing both a good thermal and electrical connection. Most data sheets provide curves of overall thermal resistance (θ_{JA}) versus copper area, for a very specific set of conditions. Figure 5-1 shows an example for the LM63635-Q1 in the WSON package. The important point brought out by these curves is that more area translates into smaller thermal resistance and better thermal performance. Also, it is evident that a point-of-diminishing-return is reached at large values of copper area.

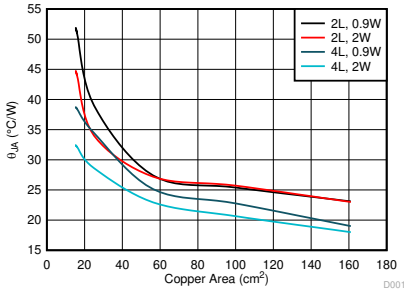

Figure 5-1. θ_{JA} vs Copper Area for LM63635-Q1 WSON

There are a number of underlying assumptions for the data provided in this graph, in addition to those shown in the legend. First, using more layers helps to reduce the thermal resistance. The outside layers are the most effective in moving heat from the regulator to the outside ambient. Note that in Figure 5-1 "2L" refers to a two layer board, while "4L" refers to a four layer board. With proper thermal vias under the DAP, the heat can move through the board and to the opposite layer most effectively. The internal layers are not as effective in removing the heat, since they are somewhat shielded by the PCB material, but they do help. Next is thickness or weight of the copper. Thicker copper will give lower thermal resistance. TI recommends at least 1 oz/ft^2 for top and bottom layers; and 2 oz/ft^2 for power dissipation of 2 W or more. The size and number of vias is also important. The thermal resistance of each via is in parallel with its neighbor, so the overall resistance will decrease with an

increasing number of vias; up to some limiting point. Thermal vias of 12-mil with 0.5 oz/ft^2 copper plating is recommended. As mentioned, the most effective place for the thermal vias is under the DAP. However, placing vias around and near the regulator will also help to reduce the thermal resistance of the board. Finally, notice in Figure 5-1 that reference is made to the power dissipation in the legend. This seems strange since Equation 1 assumes that θ_{JA} remains constant with power dissipation. In fact θ_{JA} does depend somewhat on power dissipation, thus complicating the entire process of estimating, calculating, and measuring θ_{JA}. With more power dissipation you get a larger temperature drop and therefore a somewhat more efficient heat sink due to both radiation and convection. However; throughout this discussion, assume that θ_{JA} is independent of power dissipation and state what power level was assumed when estimating or measuring the thermal performance.

All of the previously-discussed considerations also apply to packages without a DAP. As stated in Section 4, it is a little more difficult to get the heat out of these types of packages. In this case the heat must flow through the relatively narrow paths through the device pins and then to the PCB. As a result, the copper leading to the VIN, SWITCH, and GND pins should be as wide as practical.

6 PCB Layout Tips

In addition to the considerations given in the previous section, there are a few more details that should be kept in mind. The regulator can be considered as a "point" source of heat, when compared to the surrounding PCB. As shown in Figure 6-1, the heat will propagate radially from this source. You can think of the heat flow as a "pizza" slice, as shown in the figure. In our case the heat is flowing along the copper plane of the PCB. It is important not to obstruct this radial path to achieve good thermal performance.

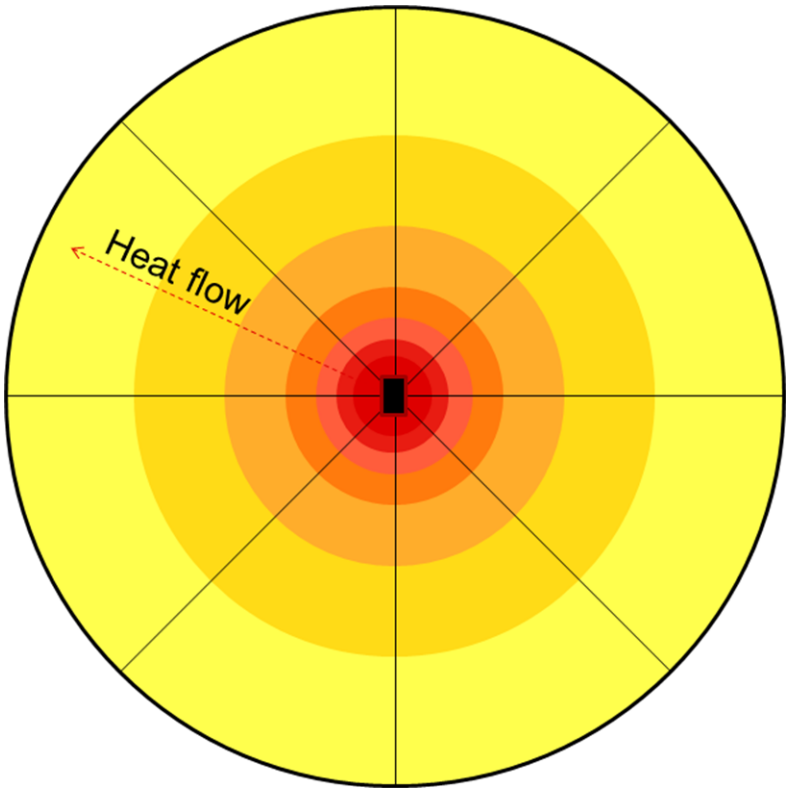

Figure 6-1. Heat Flow in "Pizza" Slice

Two important points can be learned from this model. First, the "tip" of the slice should be well connected to the heat source so that the entire slice is effective in providing a heat sink. That means avoiding cuts in the thermal plane near the device. It also means trying to put non-critical components on the side opposite the heat generating source. Secondly, it is not possible to completely avoid breaking up the thermal plane, since connections must be made to the regulator, along with critical external components. This model shows that the cuts should be made as radially as possible. Figure 6-2 shows an example of both good and bad practices.

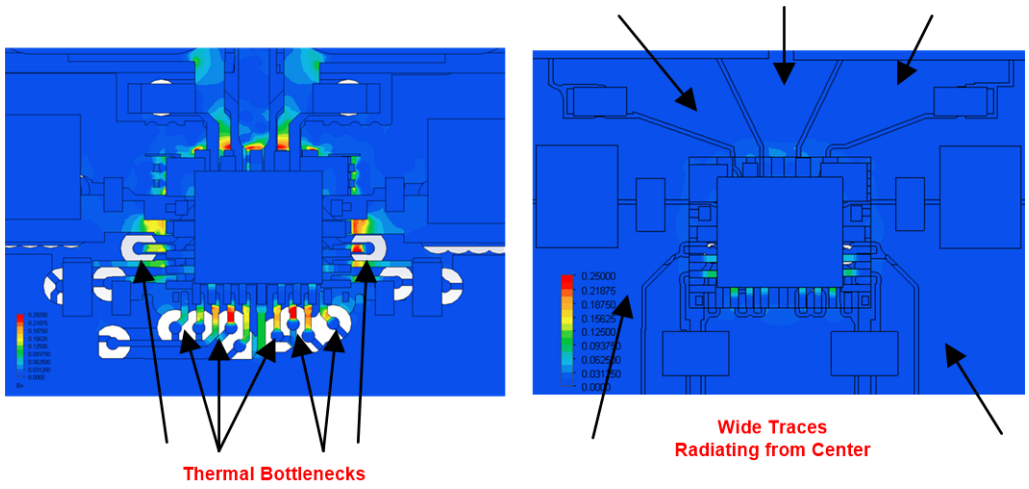

Figure 6-2. Comparison of Heat Flow Between Two PCB Layouts

This theme is continued in the example layout for the LMR33630-Q1, in the flip-chip package, shown in Figure 6-3. This shows a similar strategy of fat, wide traces radiating from the center.

Another aspect of good thermal design is how to deal with more than one heat generating source. For a switching regulator both the converter and the inductor will be dissipating power. Good electrical design usually dictates that these components are placed in close proximity to each other. It turns out that placing heat producing components too close together can have a larger effect on thermal performance than one would think. A heat generating component will have a "thermal footprint" that is about 18 times the area of the component package, as shown in Figure 6-4. A thermal footprint is the area of the PCB that participates strongly in the radiation and convection of the package. If these footprints are allowed to overlap, there will be a drastic increase in component temperature. The effect is most significant when the packages get closer than about twice the package dimension. Figure 6-5 shows measured data demonstrating this non-linear effect.

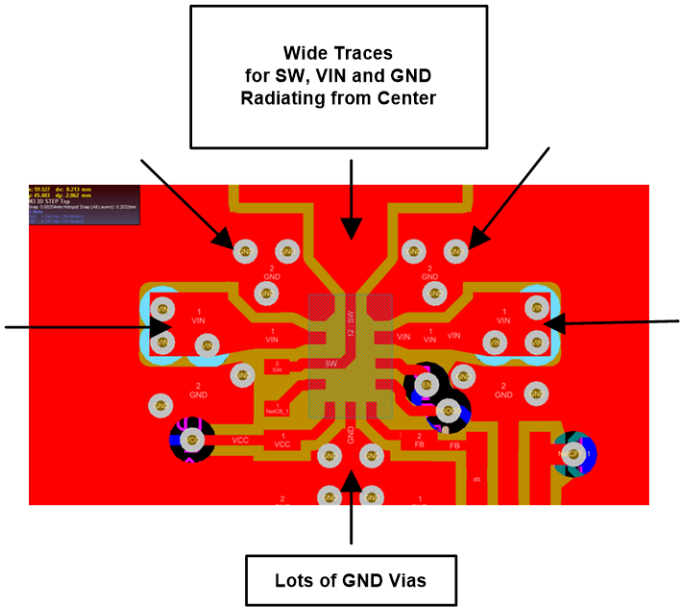

Figure 6-3. LMR3363-Q1 RNX PCB Layout Example for Good Thermal Performance

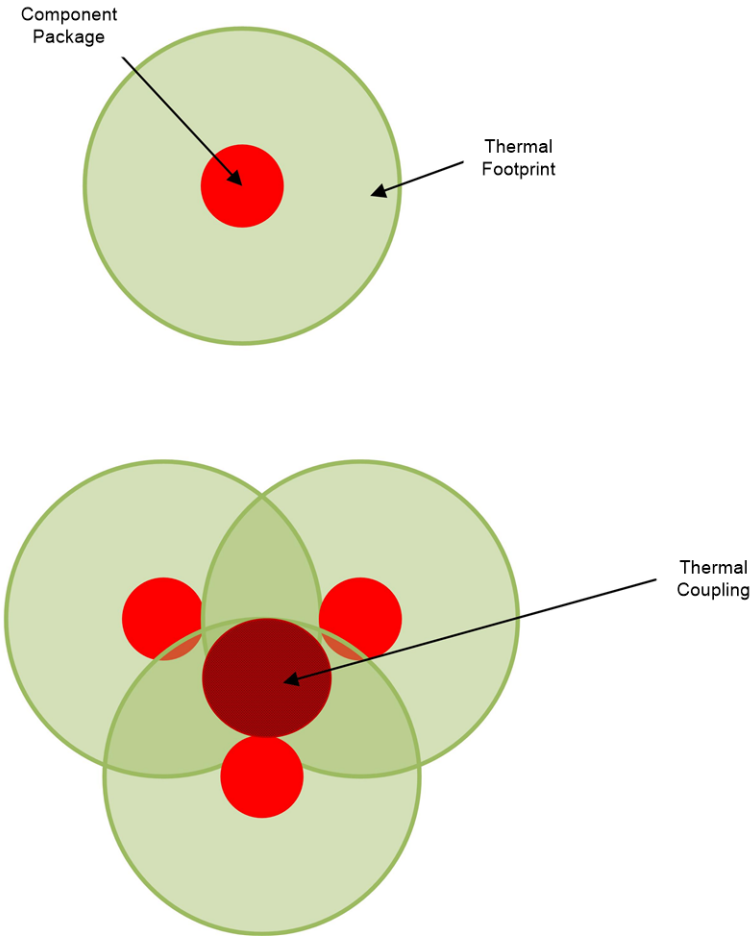

Figure 6-4. Example of Thermal Footprint Concept

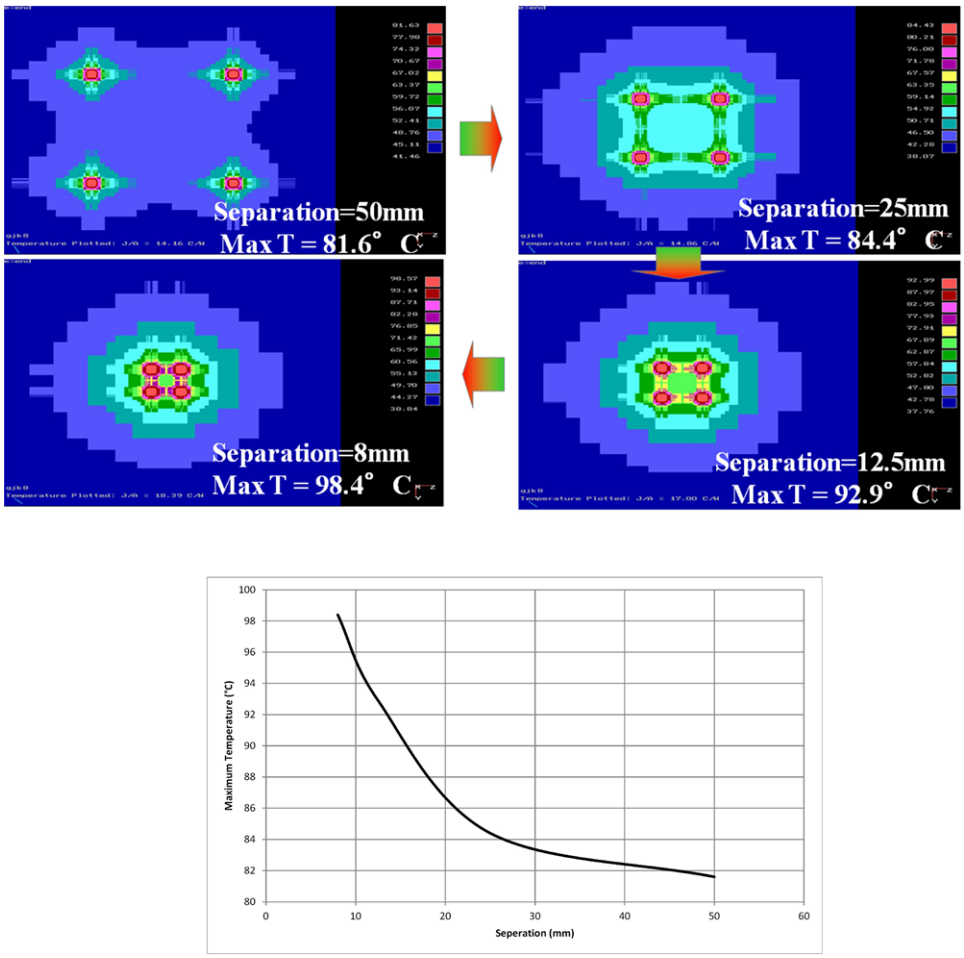

Figure 6-5. Measurement Showing the Effect of Component Crowding

Keep in mind that thermal considerations are not the only ones that enter into a good PCB layout for a DC/DC converter. Certain critical components need to be close to and on the same side as the converter. Also, wide traces on the switch node may aggravate EMI issues. The converter inductor also dissipates substantial power. However, it usually will need to be close to the device to minimize switch node area. In other words a compromise must be found; just as with any good engineering design. The best resource for good overall PCB design can be found in the regulator data sheet, and the recommendations found there should always be followed. Table 6-1 gives a summary of some best practices for good thermal PCB layout.

Table 6-1. PCB Layout Best Practices

Use a package with a DAP	If this option is available, it makes it easier to reduce the overall θ_{JA} and achieve the target thermal performance.
Maximize the copper layer on the same side as the device.	This layer will usually be ground and acts as the most effective heat sink for the device.
Use the thickest copper allowable.	Thick copper affords lower thermal resistance.
Widen PCB traces near the device.	Wide traces afford lower thermal resistance.
Avoid breaks in heat flow	Use the "pizza" slice concept when routing copper layers.
Judicial use of thermal vias	Use enough vias to connect the copper planes together to help reduce thermal resistance. Especially true under the DAP.
Avoid crowding together heat producing sources	Keep in mind the thermal footprint of heat generating sources such as the inductor when planning the PCB layout.

7 Estimating and Measuring θ_{JA}

As mentioned the goal of thermal management is to ensure that the device junction temperature stays within the desired limits. The key to estimating the junction temperature is generating a good estimate of θ_{JA}. There are several ways to arrive at an estimate depending on what resources are available. The best way to get a good estimate is to use sophisticated thermal modeling programs. This can be time consuming and expensive. The methods outlined below are not as accurate, but are much faster than conducting a complete thermal analysis and give a good idea whether the PCB/package combination will perform as desired. One common consideration with any method of thermal calculation is determining the "effective" copper area acting as the heatsink. On a crowded PCB, the regulator is only one small piece of the entire system, and it is obvious that the entire PCB copper area is not effective in acting as a heatsink for the power supply. The question becomes: "how much of the copper area surrounding the converter/inductor is effective in removing heat". The answer is related to the thermal footprint mentioned above and requires some prior experience and judgment. As a first estimate the effective copper area can be approximated as about 18 times the area of the heat producing components. However, components such as connecters, and so forth, that break the copper plane will tend to block the heat flow and reduce the effective heatsink area. On the other hand, large surface mount components, such as aluminum electrolytic capacitors, may tend to improve the thermal performance by acting as additional heatsink elements. The example given later may help to clarify some of these considerations.

7.1 Simple Guideline

If no other method is available, Equation 5 can be used to estimate the thermal resistance for a package with a DAP. Alternatively, the equation can be re-arranged to give the PCB copper area for a given required thermal resistance. This equation assumes an unbroken plane, using 1-oz copper, a perfect connection between top and bottom layers, and 1 W of power dissipation.

$$\theta_{JA} \approx \frac{500}{\text{Copper Area}\left(\text{cm}^2\right)} + \theta_{JC} \tag{5}$$

Here the copper heatsink area is in square centimeters and θ_{JC} can be found in the regulator data sheet. Let us use the LMR33630 in the HSOIC package as an example. Assuming a copper area of 20 cm^2, and θ_{JC} = 4.3°C/W, yields $\theta_{JA} \approx$ 29°C/W. This compares favorably with the value in the data sheet curve. It is also close to the data shown in Figure 5-1 for a similar package. Keep in mind that this equation is only a very rough estimate and should not be relied upon for values closer than ±50% or so.

7.2 Data Sheet Curves

Many modern converter products include curves in the data sheet of θ_{JA} versus copper area. These curves represent actual data measured on dedicated PCBs constructed for this purpose. Devices such as the LMR336x0 and LM636x5-Q1 families provide this data for the packages available for these devices. An example is shown in Figure 5-1. For the assumptions and conditions under which these curves were taken, they give a fairly good estimate of the thermal performance that can be expected. Many times curves of maximum output current vs ambient temperature, called "de-rating" curves, are also included in the data sheet. These curves are taken with an assumed value of θ_{JA} and can be used to estimate the maximum output current for a given ambient under the stated conditions.

7.3 Simplified Heat Flow Spreadsheet

The basic heat flow equations can be solved using a spreadsheet and some simplifying assumptions. *AN-2020 Thermal Design By Insight, Not Hindsight Application Report* and the accompanying spread sheet provide a

simple way to calculate thermal resistance for different PCB designs. A snap shot of the calculator output is shown in Figure 7-1.

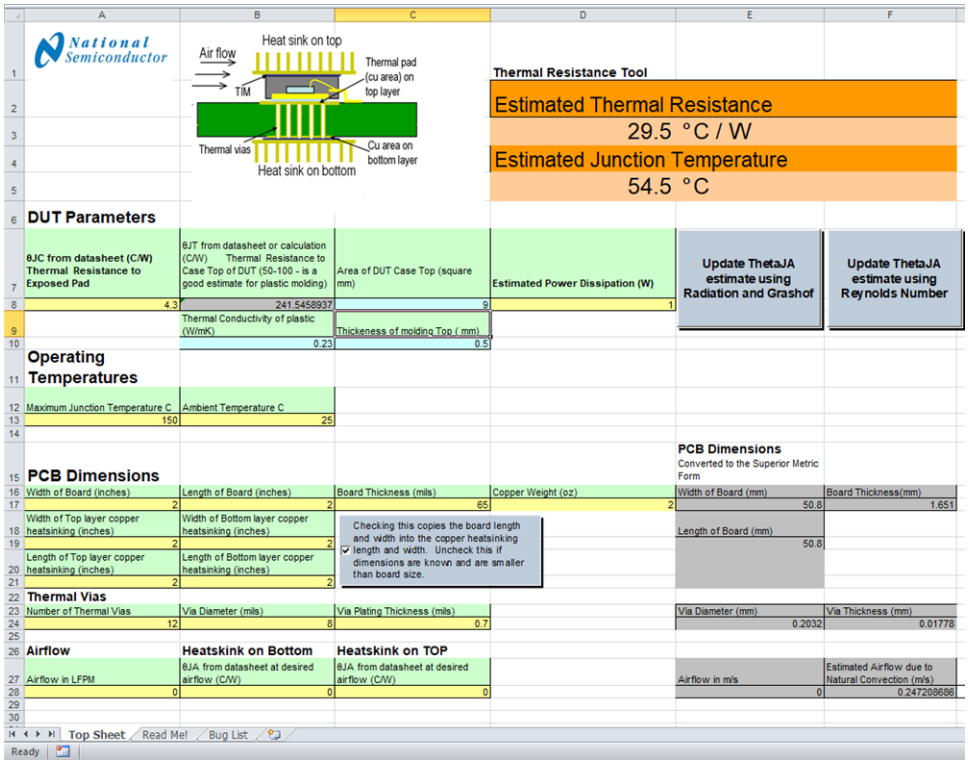

Figure 7-1. Screenshot of PCB Thermal Calculator

For a board of four square inches (about 26 cm^2) the calculator gives a θ_{JA} of about 29°C/W. This compares favorably with the data in Figure 5-1 and the simple guideline estimate. This spreadsheet also takes into account the number and size of thermal vias used in the design. It can be used to quickly and easily examine the effects of different PCB designs on the thermal performance of the application. For more information see *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*.

7.4 Online Database

TI provides an online calculator for many of our products. This tool can be used to estimate the junction temperature for a given device and power dissipation. See PCB thermal calculator for more information.

7.5 Thermal Simulators

The most accurate way to determine thermal performance is with one of the many finite-element type simulators designed for thermal analysis. These tools are rather complicated to use correctly and require detailed information about the PCB and the device package. However, many large companies will have these tools, and perhaps an entire group that is dedicated to performing this type of analysis. This method should be taken advantage of, if it is available.

8 Measuring Thermal Performance

To "close-the-loop" between calculation and actual performance, the regulator junction temperature should be measured. This section discusses three methods of measuring temperature. Remember that there are other ways to determine the actual junction temperature that may be more or less applicable in any given situation.

8.1 Thermal Camera

Probably the most convenient and reliable way to measure junction temperature is to use a thermal camera. These devices can be expensive, but they give a wide view of the temperature on the PCB, not just of the regulator. This can be helpful when evaluating a new design for "hot-spot" regions on the PCB. The simple IR-type thermal probes can also be useful, but they only give one temperature and are not as accurate as the cameras. It should be remembered that these instruments display the surface temperature of a device. The surface temperature is converted to junction temperature using Equation 6.

$$T_J = P_D \times \Psi_{JT} + T_{camera} \tag{6}$$

These cameras usually assume a certain thermal emissivity for the object they are measuring. Some components (or exposed copper) can be somewhat reflective and may give a misleading temperature reading. Since IC packages exhibit a dull black color, the camera can take an accurate temperature reading without any modification of the device.

8.2 Thermocouple

A thermocouple (TC) can be used to measure the regulator case temperature as well. This method is more complicated and time consuming than using a camera. The TC must be much smaller than the package you are probing and needs to make good thermal contact. If the TC is too large it will act as a heatsink and lower the actual temperature of the package. You also need to position the probe as close as possible to the die within the package. Equation 6 is then used to estimate the junction temperature, with the TC measurement in place of T_{camera}. The TC can also be placed on the PCB to estimate its temperature. The Ψ_{JB} parameter can then be used to estimate junction temperature from the board temperature, but this method is not as accurate as using the top case temperature. See *Semiconductor and IC Package Thermal Metrics Application Report*, for more details.

8.3 Internal Diode

The last method is the most involved and is usually only available to the IC manufacturer. Here one of the parasitic diodes appearing between the pins of the regulator and ground as a temperature sensor is used. The control pins of the device will always have an ESD protection diode connected from the pin to GND, and sometimes to VIN. Biasing this pin so that the diode is turned on provides a voltage that is temperature dependent. The first step is to calibrate the diode voltage vs. temperature in an environmental chamber. Typically the diode voltage temperature coefficient is about -2mV/°C. Then, with the same current in the diode, the voltage is measured when the device is running in the actual application. The calibration curve is then used to estimate the junction temperature from the diode voltage. There are many pitfalls with this method, such as selecting the proper pin, noise from the converter corrupting the measurement, and the time consuming calibration procedure. This method can be employed when the use of a thermal camera would be very difficult, such as when the test hardware is inside an environmental chamber.

9 Thermal Design Example

An example helps to clarify some of the ideas discussed in this paper. The LMR33630 in the HSOIC package is used. Table 9-1 summarizes the details of the design, while Figure 9-1 indicates the information needed from the data sheet.

Table 9-1. Design Example Parameters

Device	LMR33630ADDA
Input Voltage	24 V
Output Voltage	3.3 V
Output Current	3 A
Switching Frequency	400 kHz
Package	HSOIC
Ambient Temperature	85°C
T_{Jmax}	125°C

First, find the efficiency for the conditions in the application. If the efficiency for the exact conditions cannot be found, then look for data that is close and interpolate using the rules in Table 3-1. An efficiency of about 87% is found at an ambient of 25°C, and this includes the inductor loss. Reduce this to 85% to take into account the 85°C ambient in the example. The power dissipation is calculated to be about 1.7 W using Equation 2. From Equation 3 and the inductor resistance found in the data sheet, correct this power down to about 1.57 W. Next, rearrange Equation 1 to determine the maximum θ_{JA} that can be tolerated for our example conditions. This gives about 25°C/W; use 24°C/W to be conservative. Using the spreadsheet shown in Section 7.2, with the example values, adjust the size of the PCB until a value of about 24°C/W is reached. This gives a board size of about 4.84 in^2, or about 30 cm^2. To compare, the guideline in Equation 5 gives an area of about 25 cm^2; or about 20% less. Table 9-2 summarizes the results. Figure 9-2 shows the results of thermal measurements on the LMR33630ADDA EVM, using a thermal camera and Table 9-3 tabulates the results. The comparison with the calculations will be made on the basis of θ_{JA}, since the measurements were taken at 25°C. The camera gives a top case temperature of about 56°C; using Equation 6, a T_J of about 63°C is calculated. Rearranging Equation 1, and using 25°C as the ambient when the measurement was made, $\theta_{JA} \approx 24$°C/W.

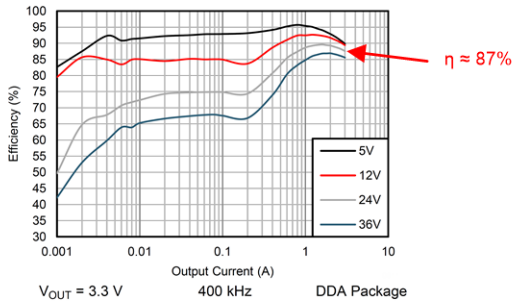

Figure 27. Efficiency

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

THERMAL METRIC[1] [2]		LMR336x0 DDA (HSOIC) 8 PINS	LMR336x0 RNX (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9[2]	72.5[2]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

Ψ_{JT} = 4.3°C/W

θ_{JC} = 4.3°C/W

$R_{inductor} \approx 0.014\Omega$

Table 3. BOM for Typical Application Curves DDA Package[1]

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	$C_{IN} + C_{HF}$	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 14 mΩ	LMR33630ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.2 µH, 16 mΩ	LMR33630CDDA
5 V	400 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	8 µH, 14 mΩ	LMR33630ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.5 µH, 8.2 mΩ	LMR33630CDDA

Figure 9-1. Design Example Information From Data Sheet

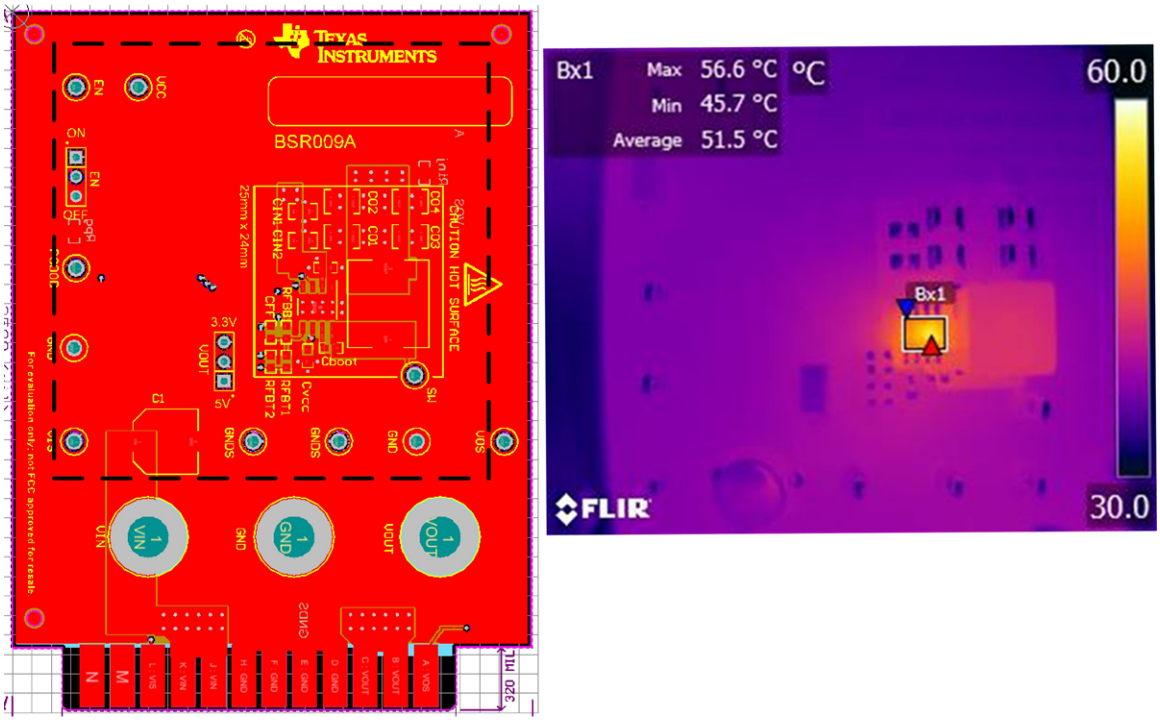

Figure 9-2. PCB Measurements for Design Example

Table 9-2. Summary of Example Design Calculations

Efficiency	0.87
Total Power Loss	1.7 W
Inductor Loss	≈ 0.13 W
Converter Loss	1.57 W
Max. θ_{JA} (for T_J = 125°C and T_A = 85°C)	≈ 25°C/W → 24°C/W
Effective Copper Area from Spreadsheet	≈ 30 cm^2
Effective Copper Area from Equation 5	≈ 25 cm^2

Table 9-3. Summary of Example Design Results

Case Top Temperature	56°C
Estimated Junction Temperature	63°C
Calculated θ_{JA}	24°C/W
Total EVM PCB Area	≈ 59 cm^2
Approx. Area of Inductor and IC Package	≈ 1.44 cm^2 + 0.2 cm^2 = 1.64 cm^2
Approx. Thermal Footprint of Heat sources	≈ 18 · 1.64 cm^2 = 29 cm^2

Notice that the total EVM area is almost 60 cm^2, or nearly double that required to get a θ_{JA} of 24°C/W. This is one of those situations where some judgment and the concept of thermal foot print come in, as mentioned in Section 7. The inductor on the EVM is about 1.2 cm by 1.2 cm, while the HSOIC package is about 0.5 cm by 0.4 cm. This gives a total area of about 1.64 cm^2. If this is multiplied by 18 (see Section 6) the product is about 29 cm^2. This is close to the calculated value and represents the effective copper area of this PCB design. The dotted line in Figure 9-2 highlights this area. A quick glance of Figure 9-2 shows that the area within the black lines is mostly clear of any thermal bottlenecks, and seems "about right" as the effective thermal area.

The previous process can be worked from many different directions. For example you may wish to determine the maximum acceptable power loss or ambient temperature based on a given PCB area. Hopefully, the previous example will provide guidance to help the designer estimate thermal performance in any given situation.

10 Conclusion

By using the thermal metrics found in the converter data sheet and a few simple equations, the thermal performance of a given application can usually be estimated well enough for engineering purposes. The considerations given here can provide sufficient information about the thermal performance for comparison purposes or may even provide a good estimate for a final design. Of course, as with any engineering endeavor, testing of a prototype application will provide the best possible measure of performance in the final product; however using the guidance in this paper, your first design is more likely to be your final design.

11 References

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*
- Texas Instruments, PCB thermal calculator

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265