LDO Thermal Performance

Kyle Van Renterghem

Applications Manager

Topics

- JEDEC Standard
- Using θja
- Guidelines For Maximum Thermal Relief

JEDEC Thermals

- Because an IC's thermal dissipation is subject to many variables we use the JEDEC standard (JESD51) for all thermal modeling.
- The JEDEC standard is used so that devices can be easily compared on a similar basis.
  - if a competitor is not reporting the JEDEC standard the customer should consider why they don't want to be directly compared to other devices.
- Common thermal metrics: θ_{JA}, θ_{JB}, $\theta_{JC(top)}$, $\theta_{JC(bot)}$

TI Datasheet

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS732[3] DRB [SON] 8 PINS	TPS732[3] DCQ [SOT223] 6 PINS	TPS732[3] DBV [SOT23] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.

Competitor Datasheet

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5-PIN PACKAGE			
	Min Pad Board (Note 3)	**1" Pad Board** (Note 4)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	4.2	4.7	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	100.9	46.8	C/W
D²PAK 5-PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	**1.2 sq. in. Spreader Board** (Note 6)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	3.8	4.0	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	74.8	41.6	C/W

3. 1 oz. copper, 0.26 inch² (168 mm²) copper area, 0.062" thick FR4.
4. 1 oz. copper, 1.14 inch² (736 mm²) copper area, 0.062" thick FR4.
5. 1 oz. copper, 0.373 inch² (241 mm²) copper area, 0.062" thick FR4.
6. 1 oz. copper, 1.222 inch² (788 mm²) copper area, 0.062" thick FR4.

28mm x 28mm area on the top side dedicated to only thermal dissipation?

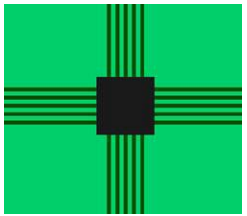
θ_{JA}: Understanding Usage and Limitations

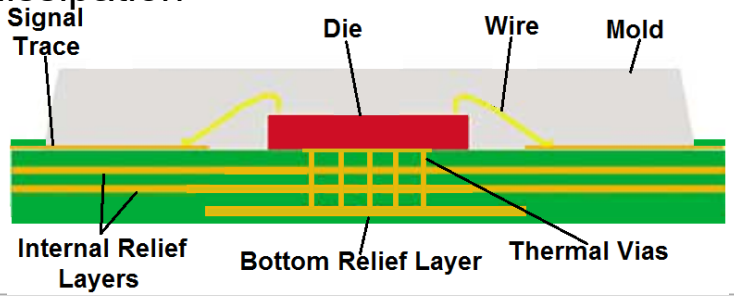
- The junction-to-ambient thermal resistance, θ_{JA}, is the most commonly used thermal metric.
  - θ_{JA} is a measure of the thermal performance of an IC mounted on a PCB.
- θ_{JA} is used since the ambient temperature is one of the few temperatures that designers have accurate data on. $T_J = T_A + (\theta_{JA} * P_D)$
  - The board acts as the main heat sink for any IC attached to it
  - If the actual application board is significantly different from the JEDEC High-K board this can result in an estimate that is unrealistic

Factors Affecting θja	Strength of Influence (rule of thumb)	Relation to θja
PCB design	Very Strong	The more metal connected to the IC the lower θja due to larger thermal mass
Chip or pad size	Strong	The larger the chip and thermal pad the lower θja due to heat spreading
Altitude	Medum	The lower the altitude the lower θja due to increased cooling efficiency of air
External ambient temperature	Weak	The higher the ambient temp the lower θja due to increased radiative heat transfer
Power dissipation	Very Weak	The higher the junction temp the lower θja due to increased heat transfer

JEDEC High-K Board

- TI LDO thermal metrics are modeled using the JEDEC High-K Board (2s2p)
- The JEDEC High-K board has:
  - Two internal planes which have ~5500mm^2 of 1oz copper (1 GND & 1 PWR plane)
  - Bottom layer (opposite the IC) thermal relief layer which has ~1100mm^2 of 2oz copper
  - One internal GND plane and bottom GND plane are connected to the thermal pad using as many thermal vias as can be fit within the power pad dimensions.
  - The top layer only has traces running straight to the pins.
- The JEDEC high-k board is good but not 100% optimized for maximum thermal dissipation





TEST BOARD DESIGN	JEDEC HIGH-K 2s2p	JEDEC LOW-K 1s0p
Trace thickness	0.0028 in	
Trace length	0.98 in	
PCB thickness	0.062 in	
PCB width	4 in	
PCB length	4.5 in	
Power/ground plane thickness	0.0014in (2 planes)	No internal copper planes

Guidelines For Maximum Thermal Relief

- ✓ Have as much metal as possible in the areas around the device (on both the same layer and the layers below the IC)
  - 2oz copper is better than 1oz copper simply because there is extra metal
  - The more thermal vias the better spreading the heat between the different layers
    - Vias should be as small as possible to decrease the amount of open space in the via hole (maximizing the amount of metal)
    - Ideally these thermal vias are all within the power pad landing pattern, but if the power pad is too small then placing extra vias as close as possible to the power pad is still helpful
- ✓ If there is a lot of metal, and the thermal vias are maximized then it is possible to reduce the θja by 35%-55%.

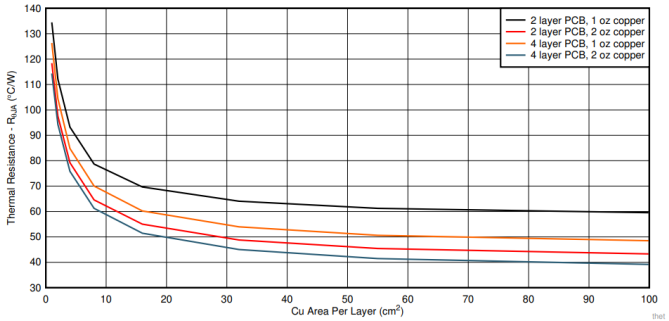
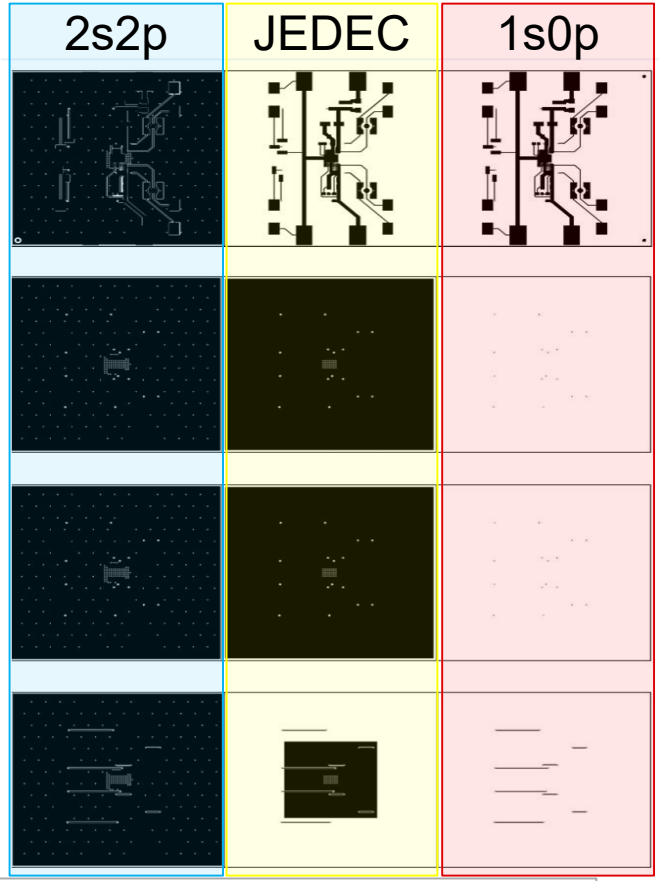


Figure 58. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package



Improving Thermal Dissipation with PCB Layout thermals

- We compared actual thermal performance of 3 package types with 5 different PCB layouts
- We learned that with an optimized PCB layout the JEDEC θja listed in our datasheets can be reduced by 35%-55%.

https://www.ti.com/lit/an/slvae85/slvae85.pdf

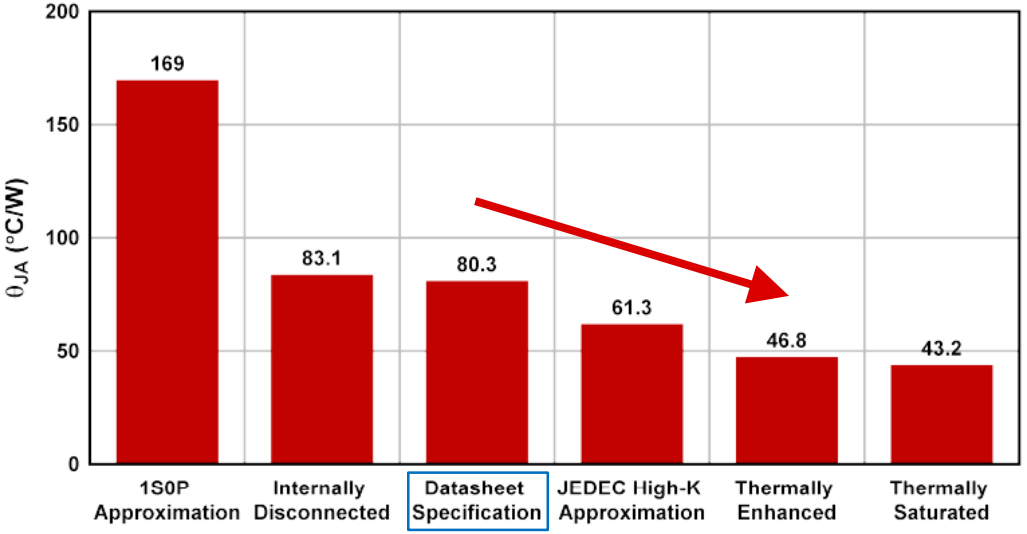


Figure 7. TPS745 (WSON) θ_{JA} vs. Board Layout

6.4 Thermal Information

THERMAL METRIC[1]		TPS745-Q1 DRV (WSON) 6 PINS	TPS745-Q1 DRB (WSON)[2] 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	62.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	73.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	35.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	35.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.8	18.2	°C/W

Other Thermal Considerations

- Nearby heat sources on the PCB can reduce the ability of the LDO to shed heat to the board
  - This is because those other heat sources increase the local board temperature decreasing the temperature differential between the board to the LDO in question
- Load pulses can still heat the die significantly if the duty cycle isn't low
  - A step increase in power dissipation will cause the die temp to stabilize on the order of hundreds of milliseconds to 1 second
    - For ~1 second pulses the LDO should reach a similar internal temp as if the load was on constantly
  - Pulses of tens of milliseconds don't heat the die nearly as much
- Forced convection and board level heatsinks can help significantly, though they are rarely a consideration for many applications which have to rely on passive cooling only
  - The thermal models in our datasheets assume natural convection (no forced air).
  - Some customer applications have a metal enclosure and it is punched so that the metal enclosure makes contact with ICs which are dissipating large amounts of power. This conduction of heat is much more affective than standard natural convection cooling.

2 methods for testing effective θ_{JA} of a PCB

1. For applications which can force ambient temp >165C
   a. Set a very light load on the output (ideally less 1mA or less)
   b. Increase the ambient temp until the device enters thermal shutdown (~165C). Note this temp as Tsd
   c. Decrease the ambient temperature at least until the devices turns back on (we usually use ~85C but in general lower is better). Note this temp as Ta.
   d. Increase the power dissipation until the LDO turns off. Note this temp as Pd
   e. You can now calculate θ_{JA} =(Tsd-Ta)/Pd
2. For applications with limited ability to change ambient temp
   a. Assume the Tsd is equal to value listed in the EC table of the datasheet.
      a. Sims indicate it can vary +-5C, but we've not seen that much variation with actual units on the bench
   b. Set the ambient temperature so that the device is on (we usually use ~85C but in general lower is better). Note this temp as Ta.
   c. Increase the power dissipation until the LDO turns off. Note this temp as Pd
   d. You can now calculate θ_{JA} =(Tsd-Ta)/Pd