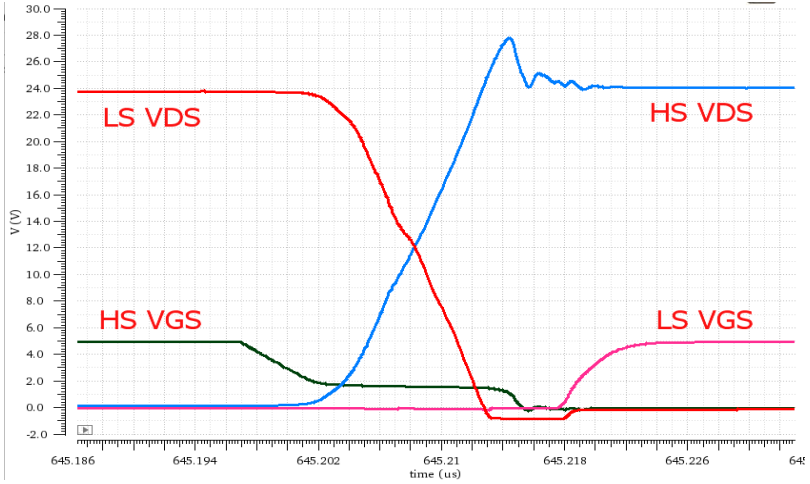
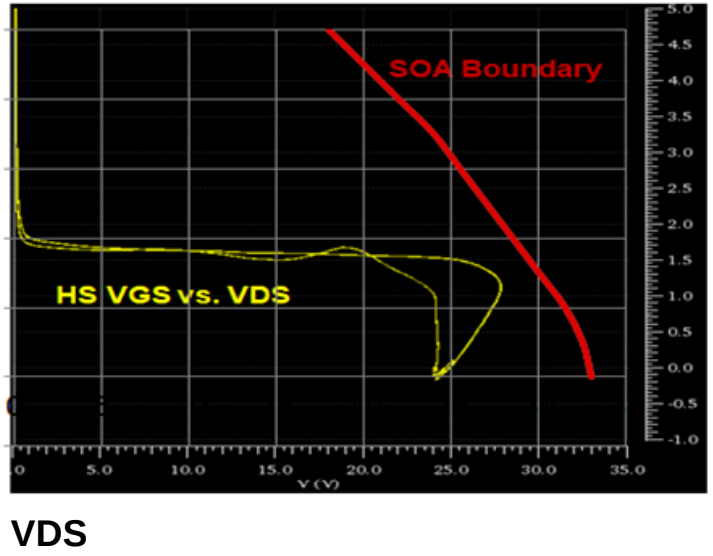
Typical MOS Stress in Operating

- Safe Operating Area (SOA) defines the boundary for reliable operation (measured at die)

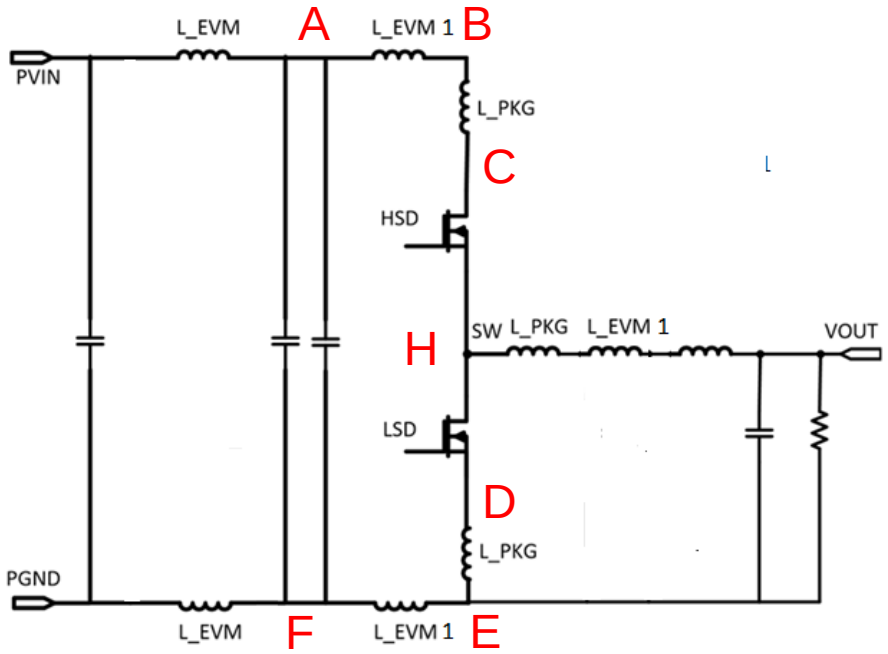


High side off and low side on, monitor high side Vds



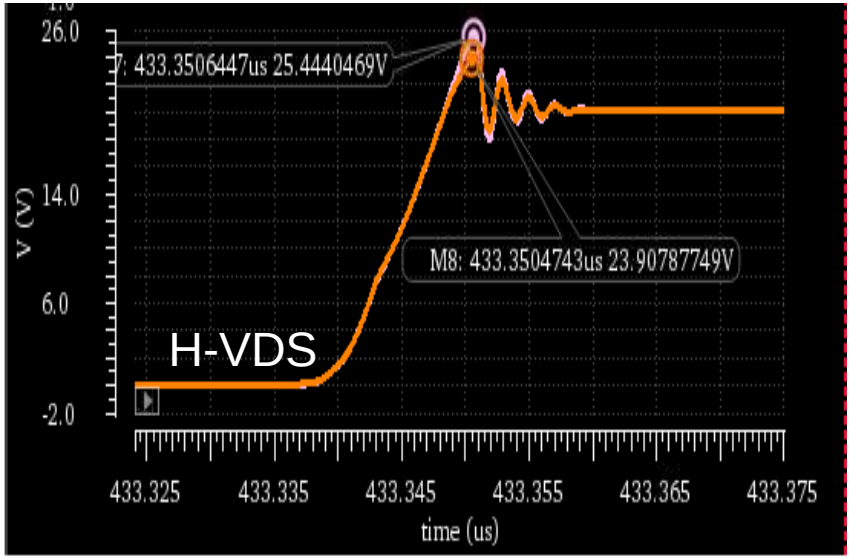
Power LDMOS Simulation Bench

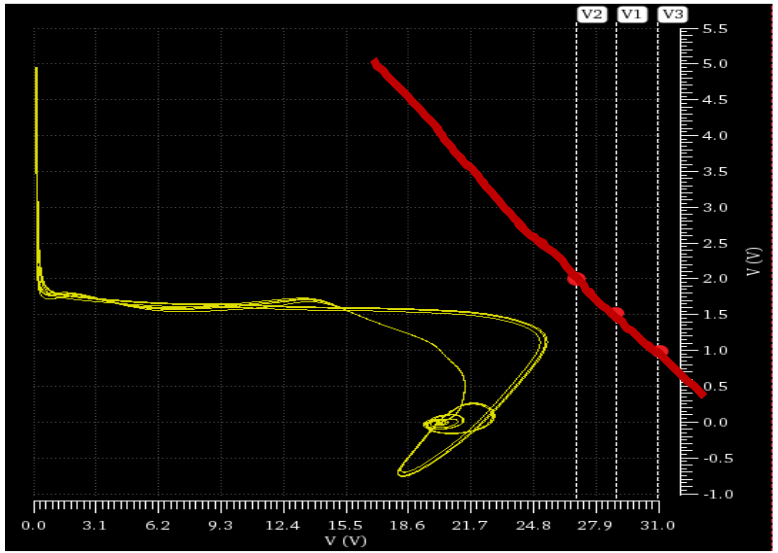
- L_EVM is PCB parasitic inductance and L_PKG is package parasitic inductance
- Bench test is always test AF node ring voltage, Simulation can get really CH/HD node ring voltage



Ring Voltage Simulation Result

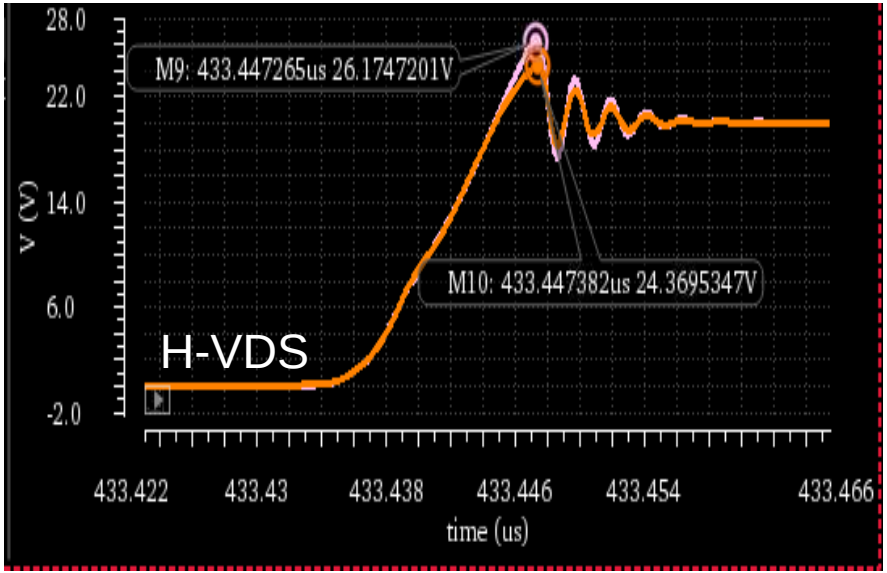
	Ring voltage on High side Vds (internal IC, VC-H)	Ring voltage on High side Vds (External IC, VA-H)	Parasitic inductance (L_EVM1+L_PKG)
20V EVM	25.44V	23.9V	350pH

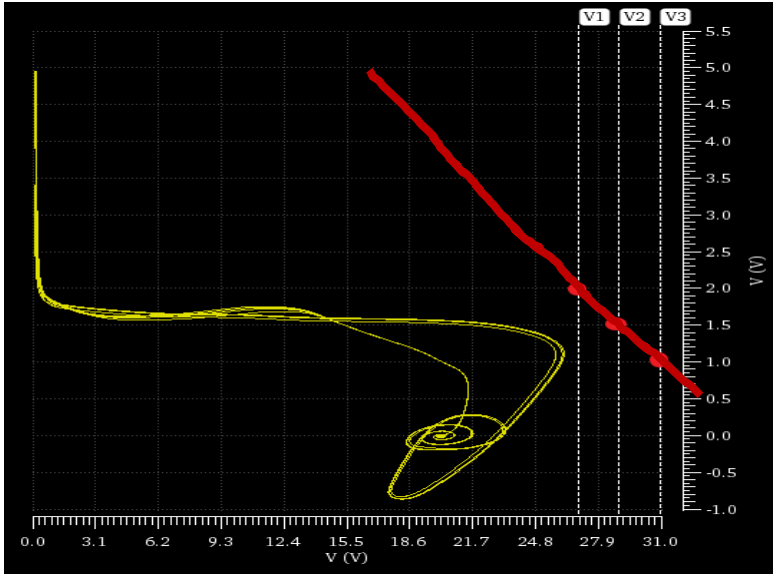




Ring Voltage Simulation Result

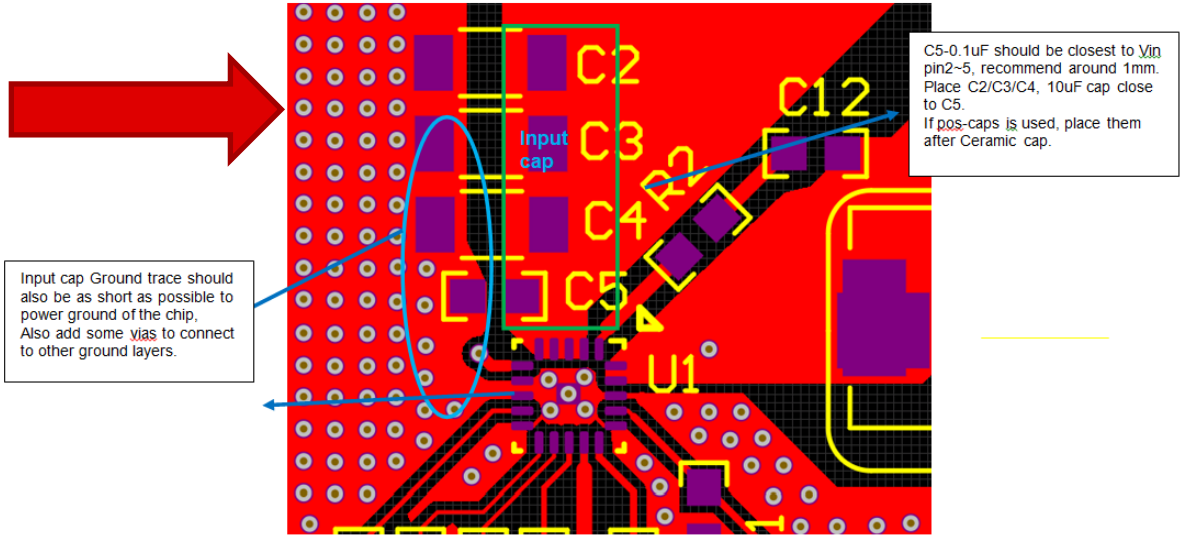
	Ring voltage on High side Vds (Internal IC, VC-H)	Ring voltage on High side Vds (External IC, VA-H)	Parasitic inductance (L_EVM1+L_PKG)
20V EVM	26.17V	24.37V	450pH





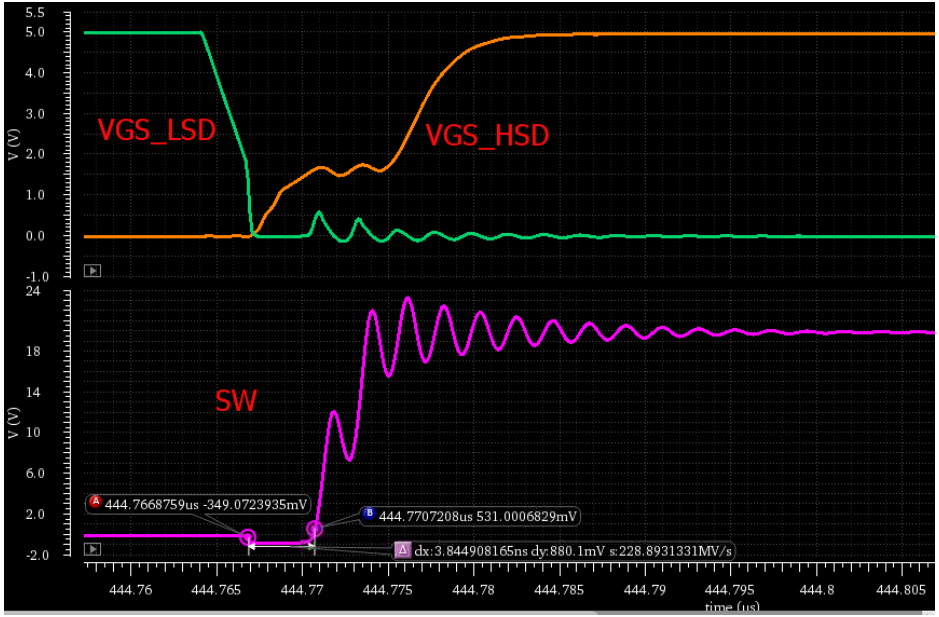
Layout Recommendation for input caps

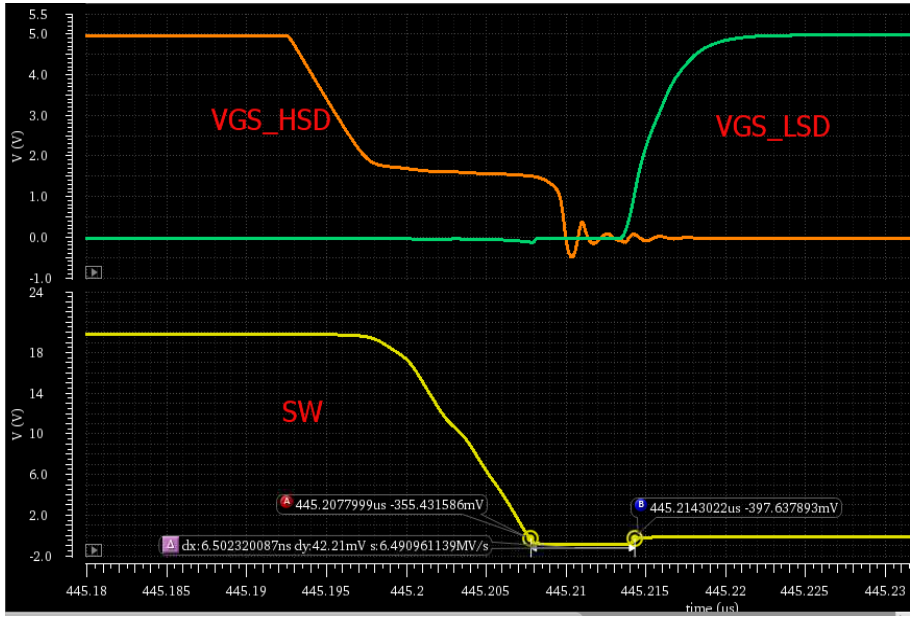
The placement and connection of input capacitor is critical. The goal is to reduce parasitic inductance between input capacitor and Vin pins. Also, the input capacitor ground should be directly connected to power ground through multiple areas to reduce ground connection inductance. High parasitic inductances increase spike voltage on internal FETs during switching rise and fall time due to L di/dt rule. Ultimately reducing these parasitic inductances is essential to prevent EOS events. Parasitic inductance can be reduced by making the path from input capacitor to IC Vin pin as short and wide as possible. 0.1uF cap, which has lower ESL and used for higher Frequency response, need to be added and placed closest to PVIN pins and PGND pins with short loop, and the goal is to make the connection around 0.05 inches (1 to 1.5 mm), the closer, the better, like in below picture C5 to Pin2~5.



Dead-time simulation

Dead time	HS-on to LS-off	HS-off to LS-on	Simulation condition
	3.8ns	6.5ns	Vin=20V, Iout=8A, Vout=5V





RPPM Result

PN	Shipment	Failure rate
TPS51396/A	>30M	< 0.5ppm
TPS51393	>10M	<0.5ppm

TPS51396/A and TPS51393 have been shipping in volume production for several years and got minimal return.

The RPPM (returned parts per million) for these devices are quite low over the last several years

There is high voltage applications, up to 19.5V, the RPPM is similar as other applications, no significant difference was observed.