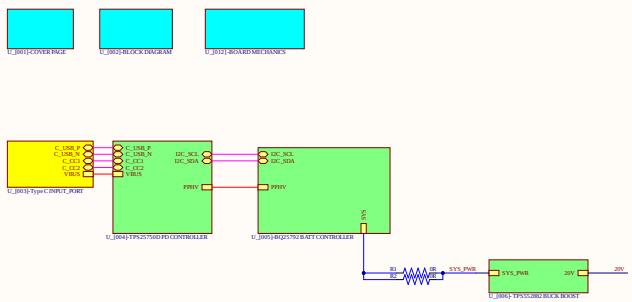

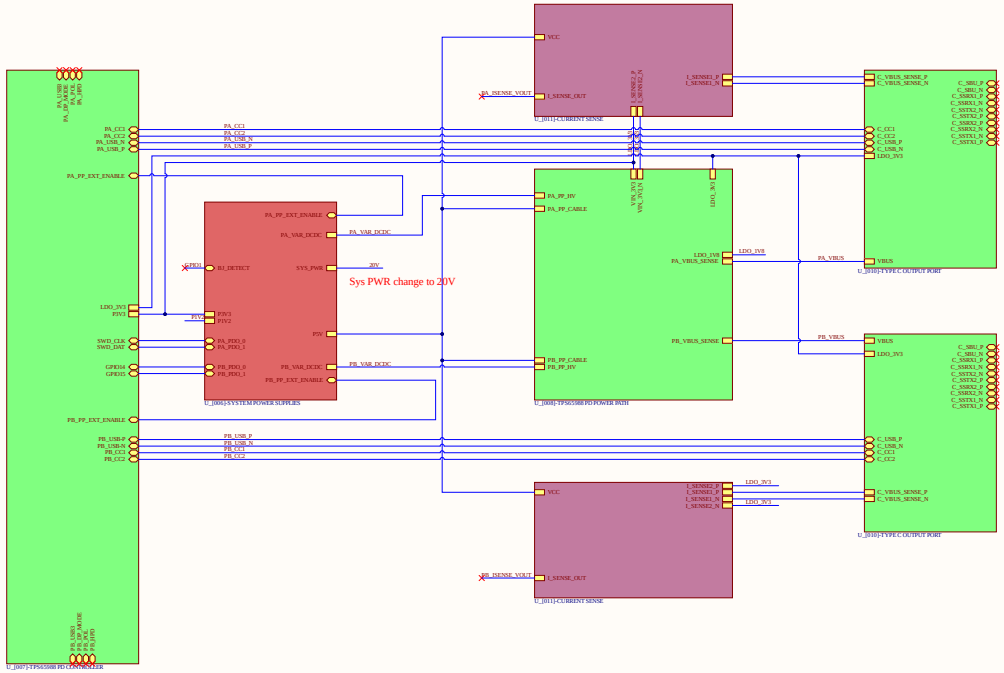

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
DNP

Net Class Example

Net Class
ClassName PCIE

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Title:			**Designer:**
Size: A1	Number: 1	Revision:	
Date: 9/5/2022	Time: 1:22:29 AM		
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9/5/2022

Variant:

Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	11	.....	21	.....	31	.....
2	BLOCK DIAGRAM	12	.....	22	.....	32	.....
3	.....	13	.....	23	.....	33	.....
4	.....	14	.....	24	.....	34	.....
5	.....	15	.....	25	.....	35	.....
6	.....	16	.....	26	.....	36	.....
7	.....	17	.....	27	.....	37	.....
8	.....	18	.....	28	.....	38	.....
9	.....	19	.....	29	.....	39	.....
10	.....	20	.....	30	.....	40	.....

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title:			***Designer:***
Size: A3	Number: 2.	Revision:	
Date: 9/5/2022	Time: 1:22:29 AM		
Sheet 2 of 15			
Company: ***Address:***			

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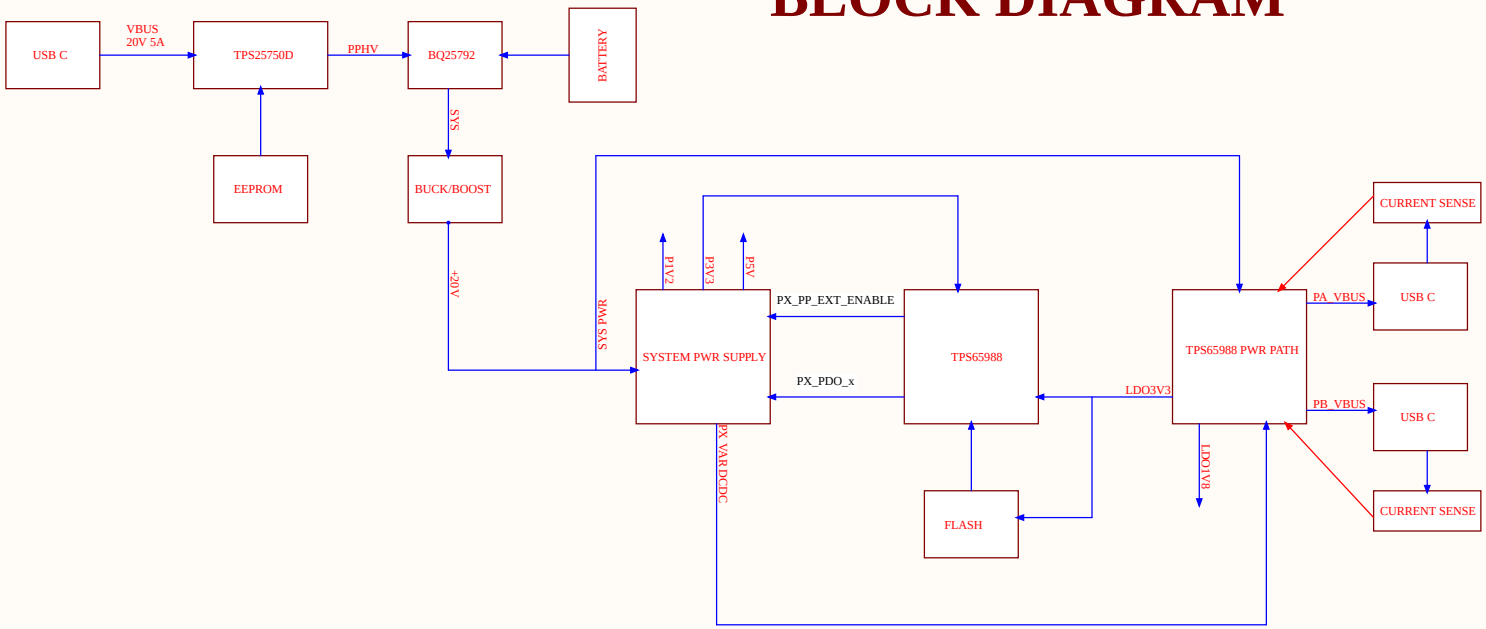
BLOCK DIAGRAM



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Date: 9/5/2022	Time: 1:22:30 AM		
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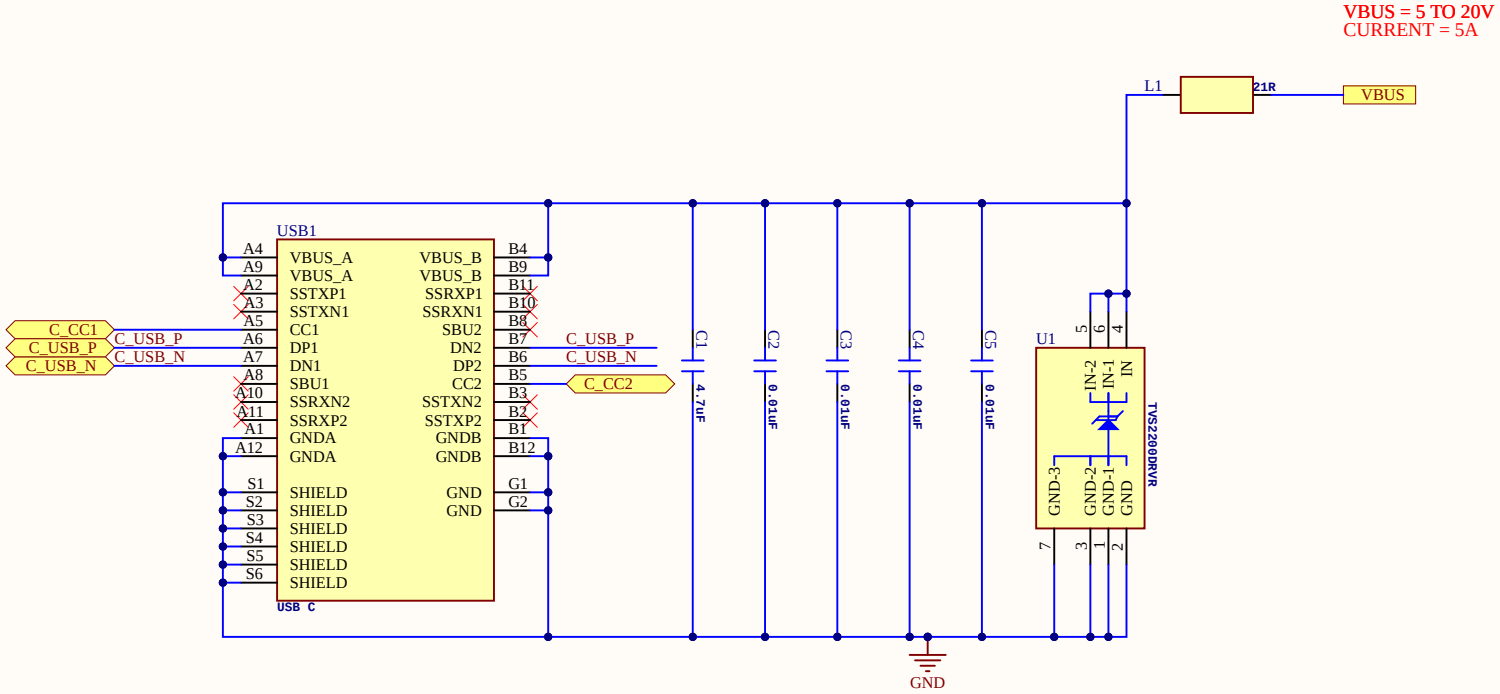

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Sheet 4 of 15			
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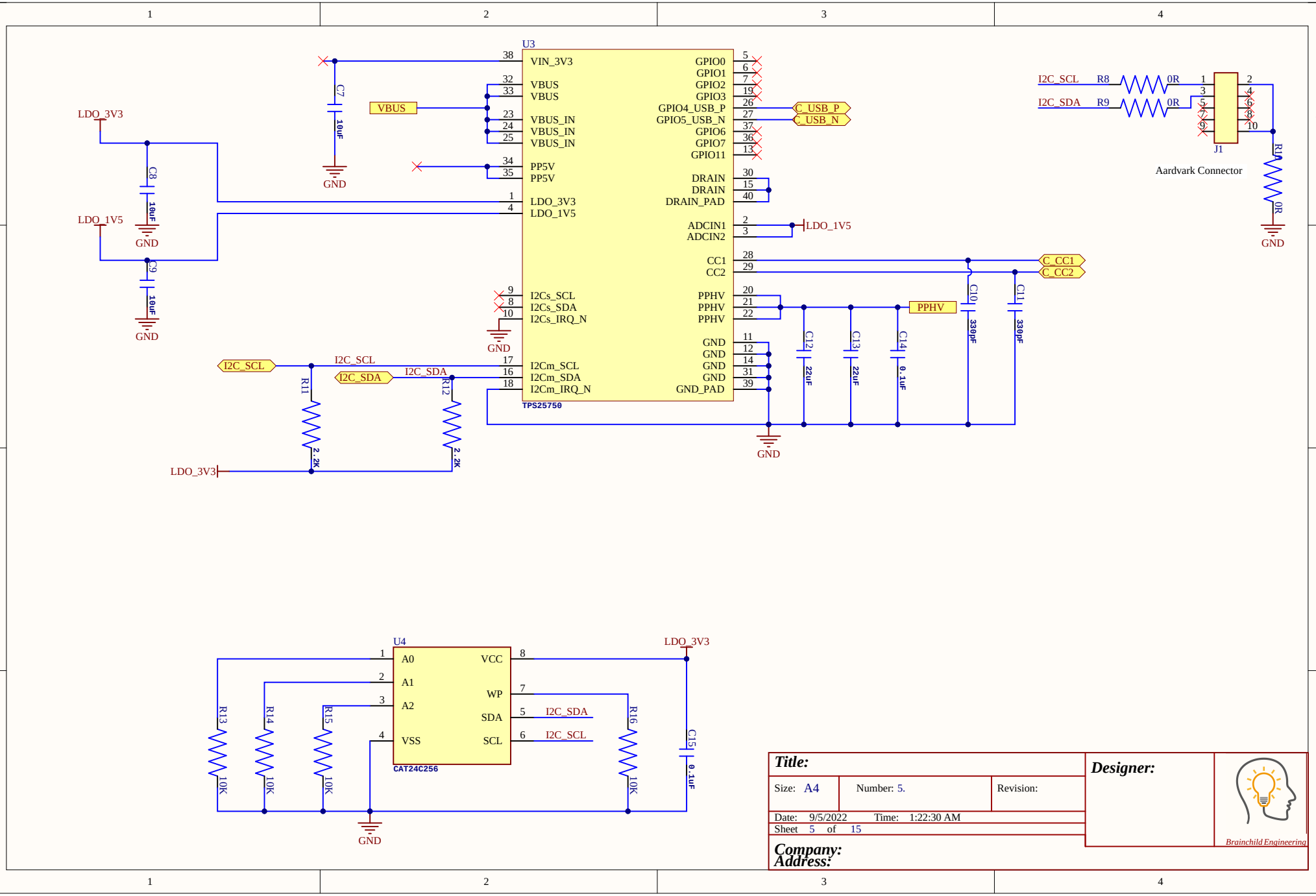

Title:

Size: A4 | Number: 5. | Revision:

Date: 9/5/2022 Time: 1:22:30 AM

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Company:
Address:

Designer:

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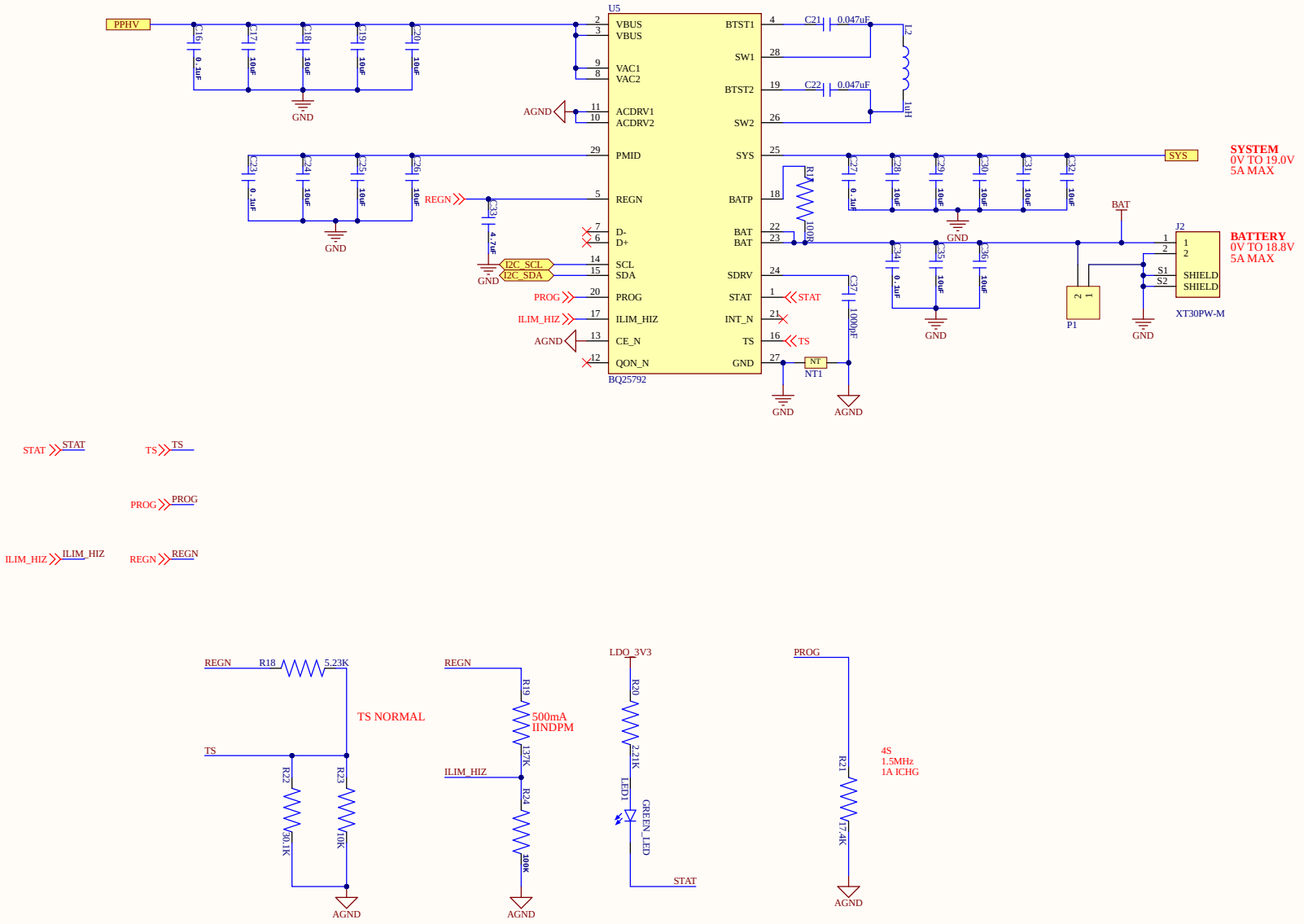

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Date: 9/5/2022	Time: 1:22:31 AM		
Sheet 6 of 15			
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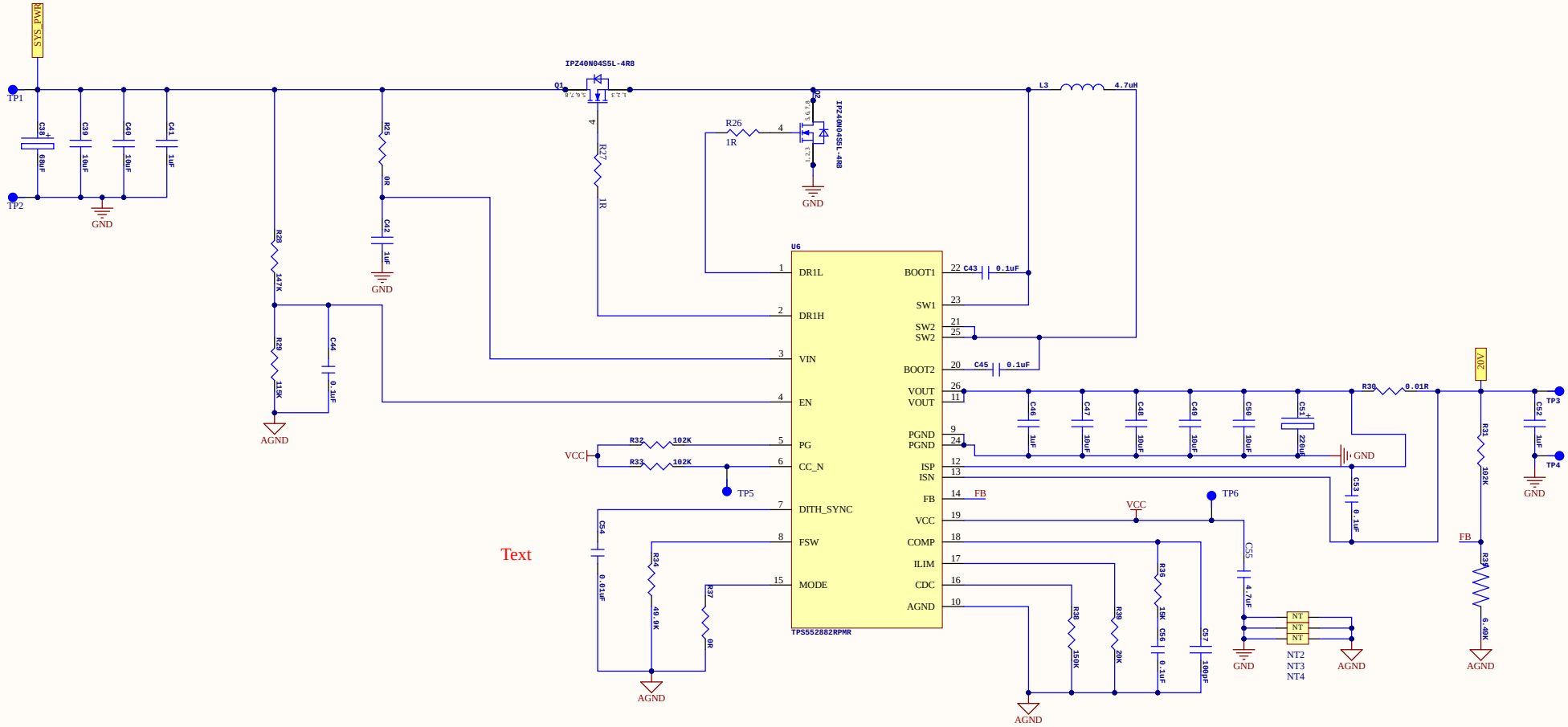

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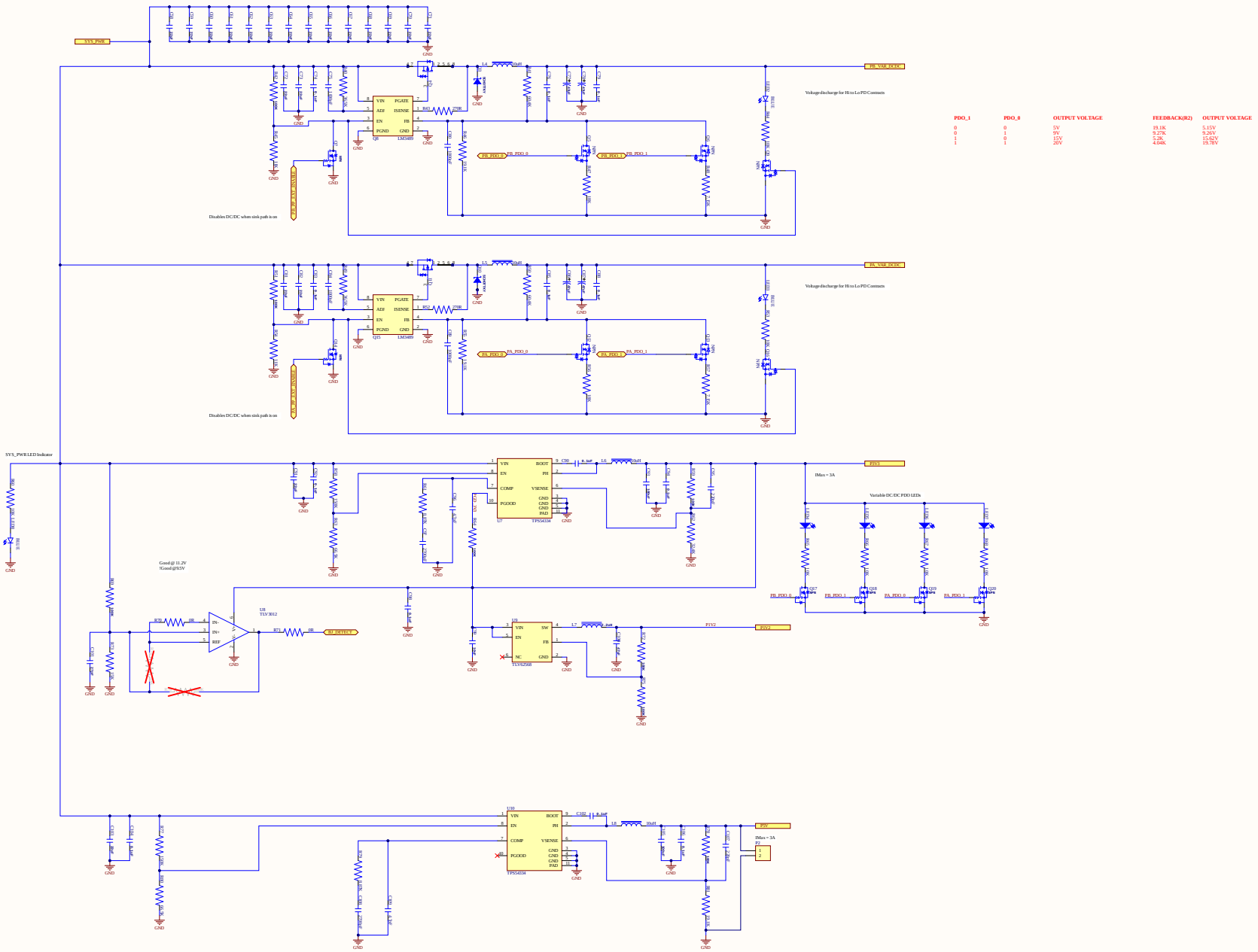

PDO_1	PDO_0	OUTPUT VOLTAGE	FEEDBACK(R2)	OUTPUT VOLTAGE
0	0	5V	19.1K	5.15V
0	1	9V	9.27K	9.26V
1	0	15V	5.2K	15.62V
1	1	20V	4.04K	19.78V

Title:
Size: A1 Number: 8 Revision:
Date: 9/5/2022 Time: 1:22:32 AM
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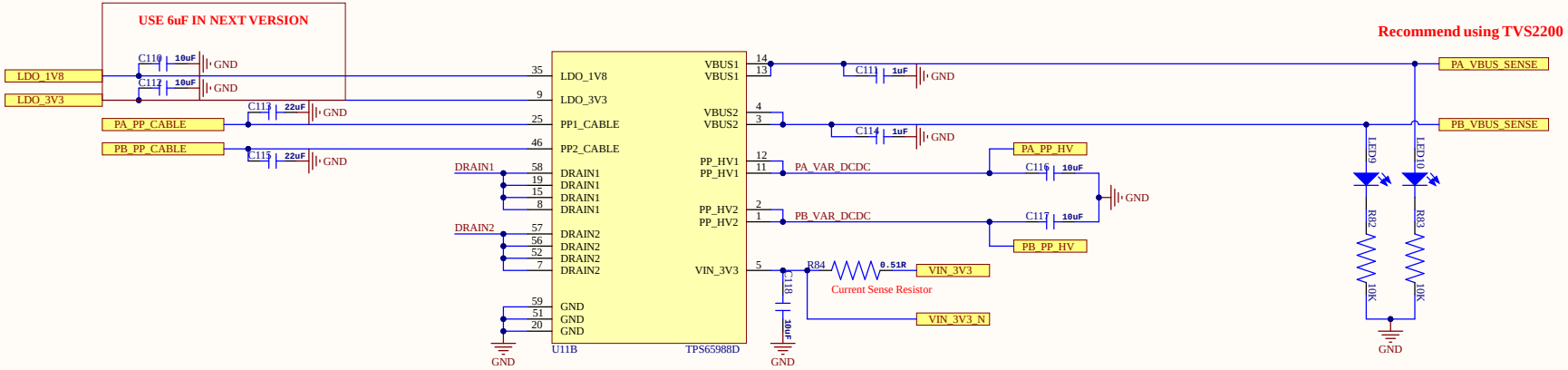
Designer:



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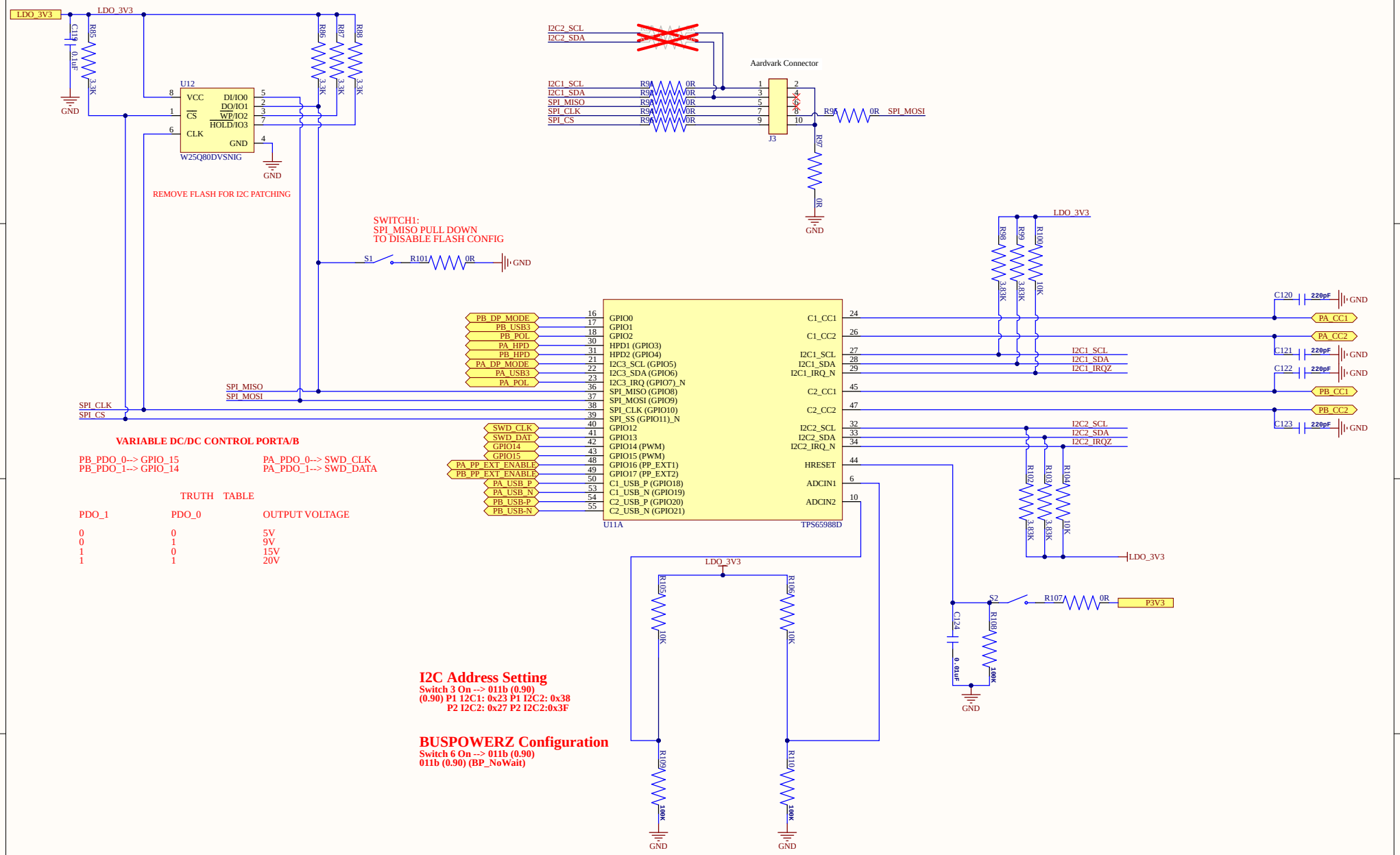
LDO_3V3
C119 0.1uF
R85 3.3K
GND
U12
VCC
CS
CLK
DI/IO0
DO/IO1
WP/IO2
HOLD/IO3
GND
W25Q80DVSNIG
R86 3.3K
R87 3.3K
R88 3.3K
REMOVE FLASH FOR I2C PATCHING
I2C2_SCL
I2C2_SDA
Aardvark Connector
I2C1_SCL
I2C1_SDA
SPI_MISO
SPI_CLK
SPI_CS
R94 0R
R95 0R
SPI_MOSI
J3
R97 0R
SWITCH1:
SPI_MISO PULL DOWN
TO DISABLE FLASH CONFIG
S1
R101 0R
R98 3.83K
R99 3.83K
R100 10K
C120 220pF
C121 220pF
C122 220pF
C123 220pF
PA_CC1
PA_CC2
PB_CC1
PB_CC2
I2C1_IRQZ
I2C2_IRQZ
PB_DP_MODE
PB_USB3
PB_POL
PA_HPD
PB_HPD
PA_DP_MODE
PA_USB3
PA_POL
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS
SWD_CLK
SWD_DAT
GPIO14
GPIO15
PA_PP_EXT_ENABLE
PB_PP_EXT_ENABLE
PA_USB_P
PA_USB_N
PB_USB-P
PB_USB-N
GPIO0
GPIO1
GPIO2
HPD1 (GPIO3)
HPD2 (GPIO4)
I2C3_SCL (GPIO5)
I2C3_SDA (GPIO6)
I2C3_IRQ (GPIO7)_N
SPI_MISO (GPIO8)
SPI_MOSI (GPIO9)
SPI_CLK (GPIO10)
SPI_SS (GPIO11)_N
GPIO12
GPIO13
GPIO14 (PWM)
GPIO15 (PWM)
GPIO16 (PP_EXT1)
GPIO17 (PP_EXT2)
C1_USB_P (GPIO18)
C1_USB_N (GPIO19)
C2_USB_P (GPIO20)
C2_USB_N (GPIO21)
C1_CC1
C1_CC2
I2C1_SCL
I2C1_SDA
I2C1_IRQ_N
C2_CC1
C2_CC2
I2C2_SCL
I2C2_SDA
I2C2_IRQ_N
HRESET
ADCIN1
ADCIN2
U11A
TPS65988D
R102 3.83K
R103 3.83K
R104 10K
S2
R107 0R
P3V3
C124 0.01uF
R108 100K
R105 10K
R106 10K
R109 100K
R110 100K
VARIABLE DC/DC CONTROL PORTA/B
PB_PDO_0--> GPIO_15
PB_PDO_1--> GPIO_14
PA_PDO_0--> SWD_CLK
PA_PDO_1--> SWD_DATA
TRUTH TABLE
PDO_1 PDO_0 OUTPUT VOLTAGE
0 0 5V
0 1 9V
1 0 15V
1 1 20V
I2C Address Setting
Switch 3 On --> 011b (0.90)
(0.90) P1 I2C1: 0x23 P1 I2C2: 0x38
P2 I2C2: 0x27 P2 I2C2:0x3F
BUSPOWERZ Configuration
Switch 6 On --> 011b (0.90)
011b (0.90) (BP_NoWait)
Title:
Size: A3
Number: 10.
Revision:
Date: 9/5/2022
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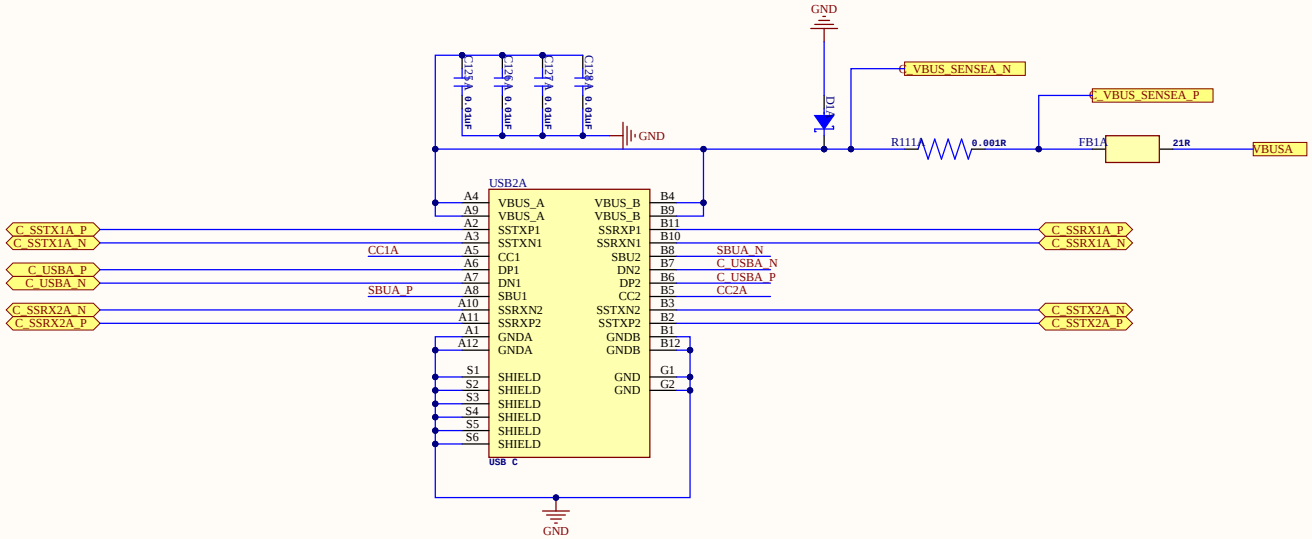

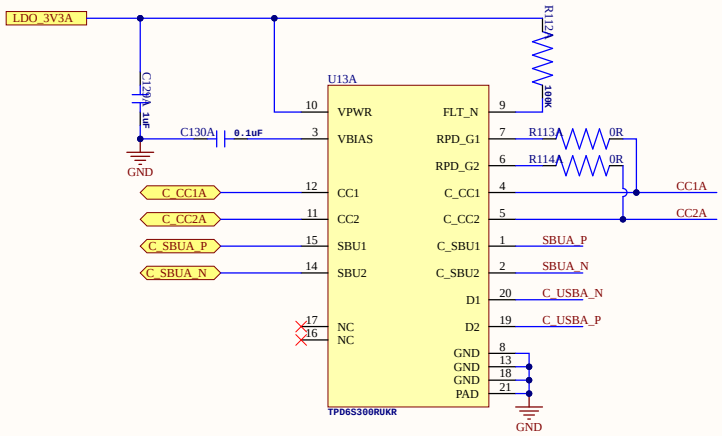

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Size: A3	Number: 11.2	Revision:	
Date: 9/5/2022	Time: 1:22:33 AM		
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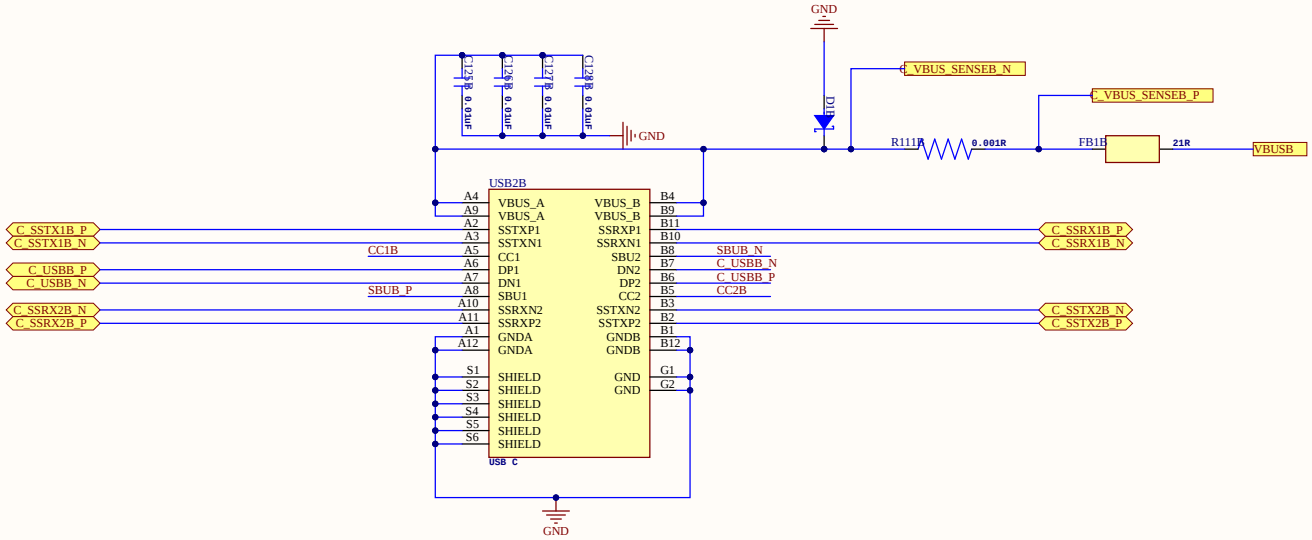

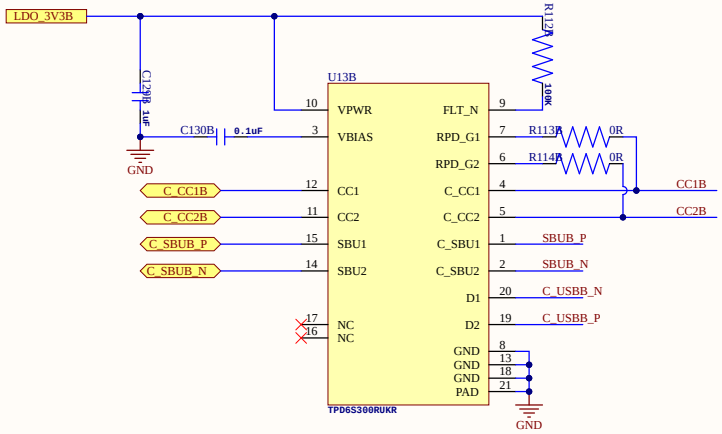

Title:			**Designer:**
Size: A3	Number: 11.1	Revision:	
Date: 9/5/2022	Time: 1:22:33 AM		
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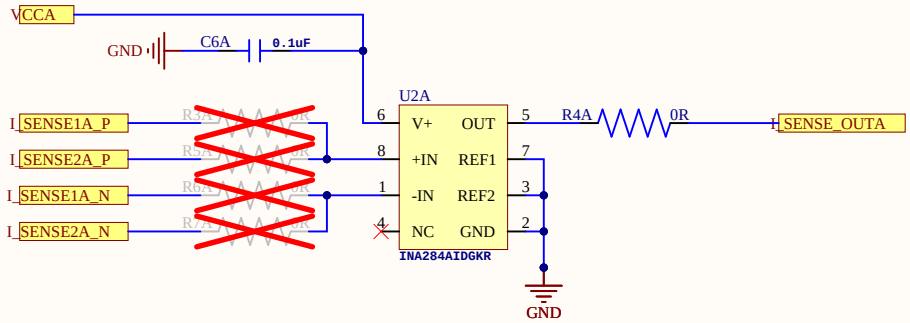

Title:			**Designer:**
Size: A4	Number: 12.2	Revision:	
Date: 9/5/2022	Time: 1:22:33 AM		
Sheet 12.1of 15			
Company: **Address:**			

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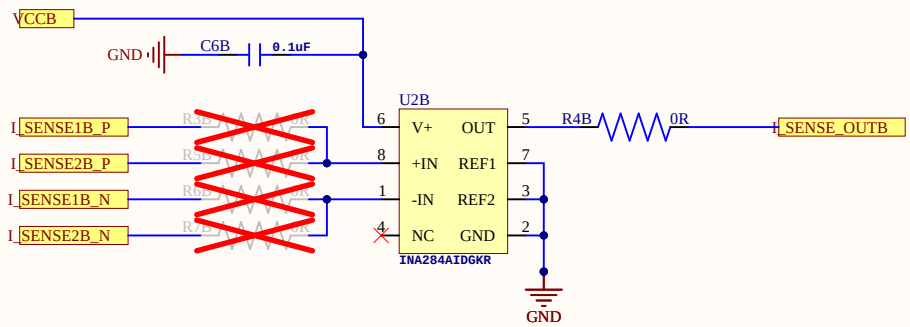

Title:			**Designer:**
Size: A4	Number: 12.1	Revision:	
Date: 9/5/2022	Time: 1:22:34 AM		
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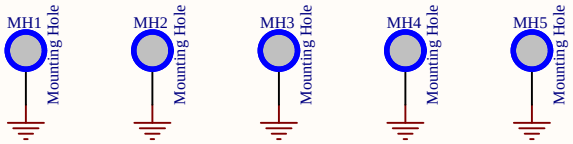
BOARD MECHANICS

MOUNTING HOLES



Title:			**Designer:**
Size: A4	Number: 13.	Revision:	
Date: 9/5/2022	Time: 1:22:34 AM		
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