MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated[1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation - usually a single resistor - adds to its attractiveness. However, this introduces a new problem - that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from yet containing elements of each. Although this has been addressed in part by several authors[1,2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

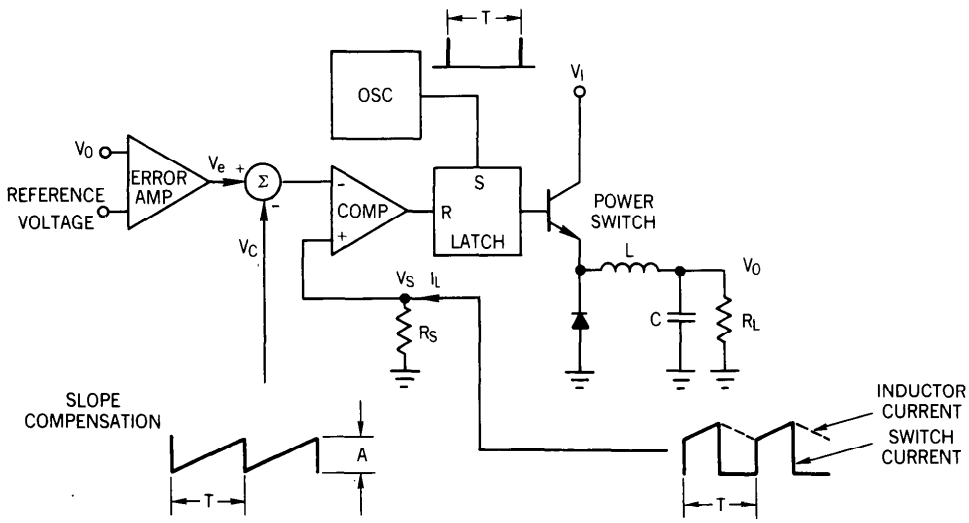


FIGURE 1 - A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in (1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle - regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

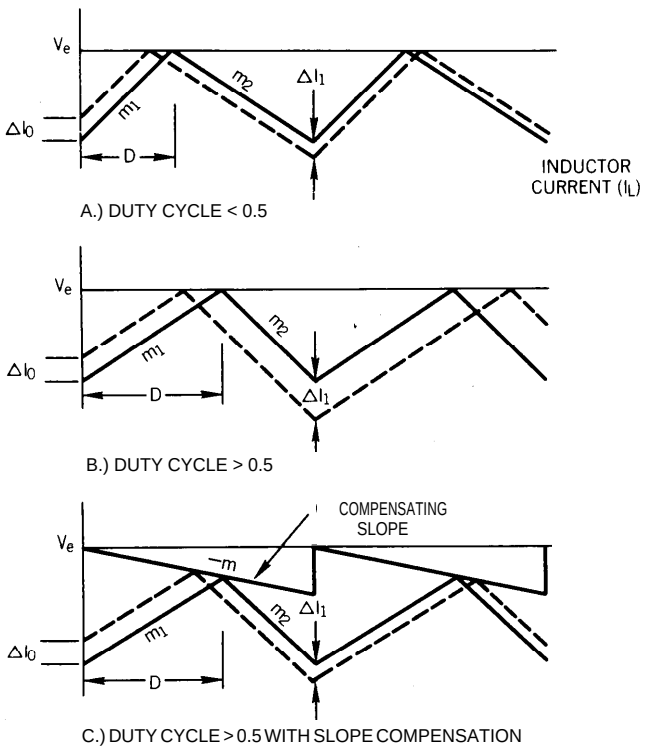


FIGURE 2 - DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for D < 0.5 (Figure 2A), and increase with time for D > 0.5 (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope -m as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

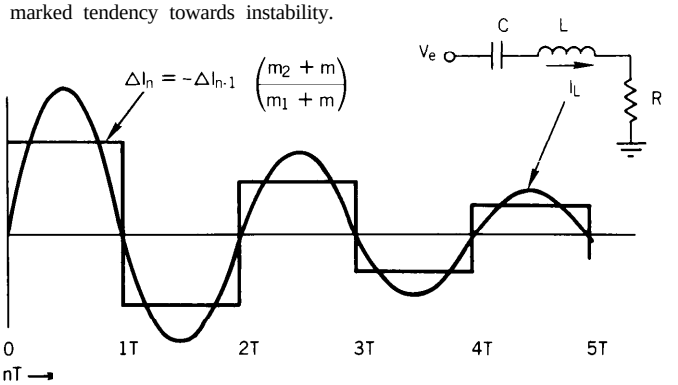


FIGURE 3 - ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

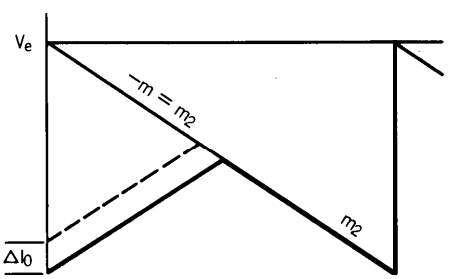


FIGURE 4 - FOR THE CASE OF m = - m_2, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and - because of excess phase shift in the modulator - can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

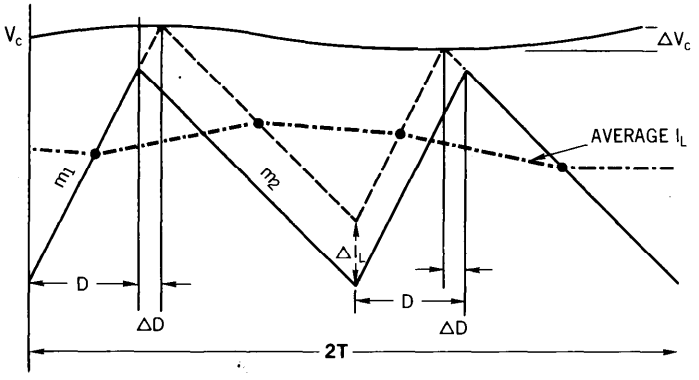


FIGURE 5- CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \quad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \quad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \quad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \quad (7)$$

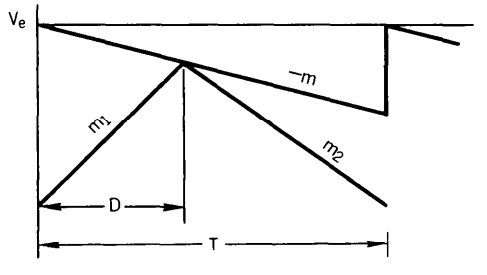


FIGURE 6- ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \quad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \quad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \quad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at f = ½f_S as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \quad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at f = ½f_S is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \quad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at f = ½f_S to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \quad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at f = ½f_S, then for the case of m = 0 (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to m = −½m_2, the point of instability moves out to a duty cycle of 1.0, however in any practical

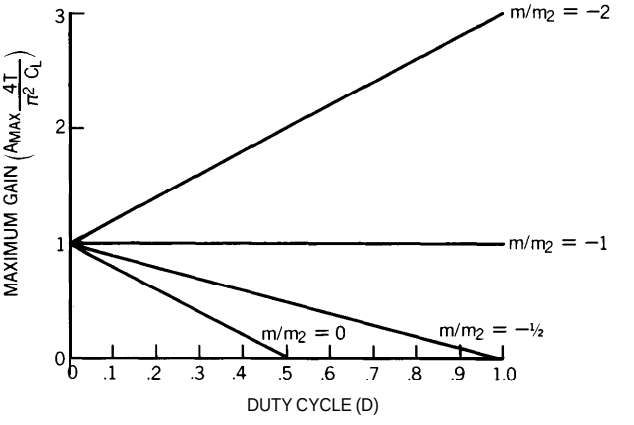


FIGURE 7 - MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum. gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage - in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output - or feedforward characteristics. If we choose to add slope compensation equal to $m = -½\ m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -½\ m_2$.

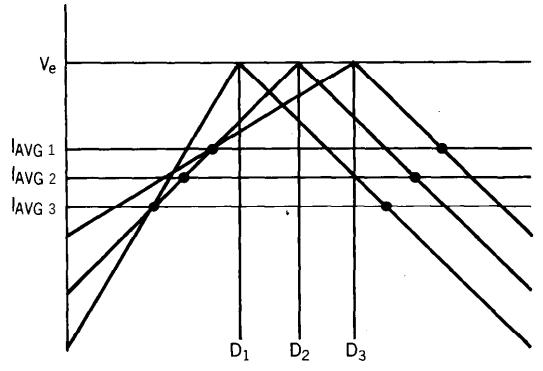


FIGURE 8 - PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

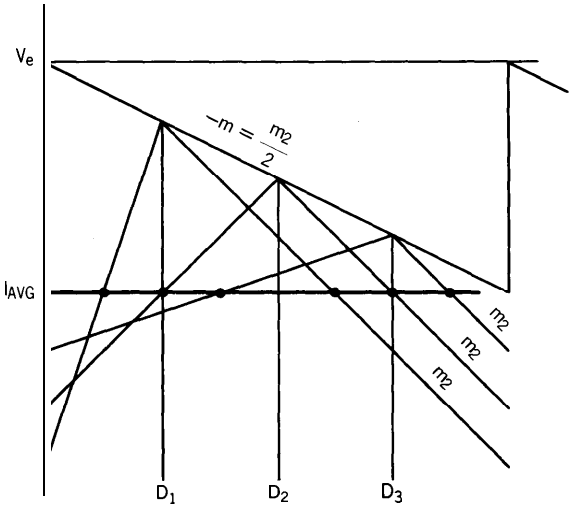


FIGURE 9 - AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUN CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -½\ m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons - reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current - not just the ripple current This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -½\ m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

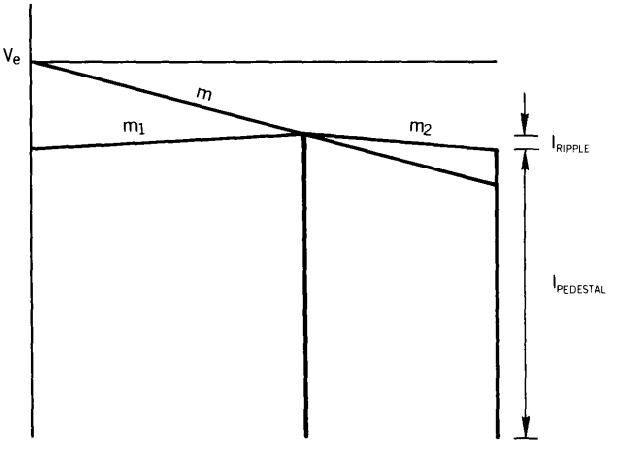


FIGURE 10 - A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11 a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

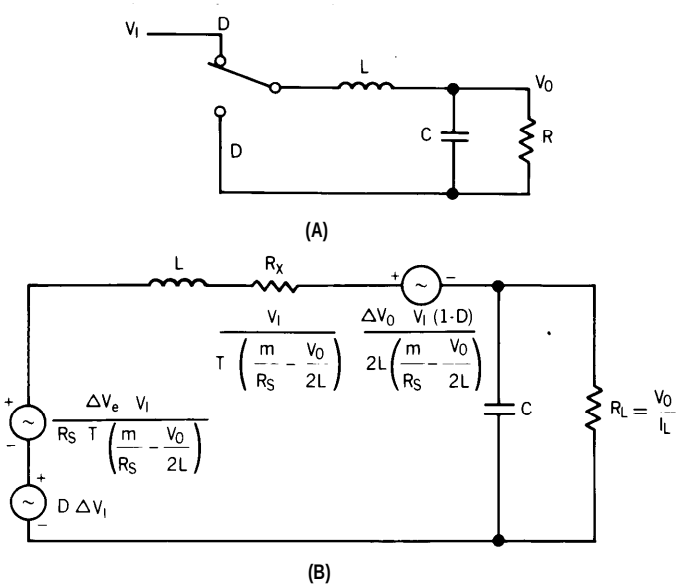


FIGURE 11: BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations - that in substitute $V_I + \Delta V_I, V_0 + \Delta V_0, D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables - and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_0}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (17)$$

A third equation - the control equation - relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\, V_0\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta D T \left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1-D)\Delta V_0 \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e\, V_I}{R_S\, LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0\, V_I\,(1-D)}{2L^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed In most cases, the dependent source between R_X and C can be ignored

If R_X is much greater than L, as is the case for little or no compensation (m = 0), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to L $\left(m \gg \frac{R_S V_0}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S V_0}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S V_0}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_0 = 12V
V_I = 25V
L = 200 µH
C = 300µf
T = 20µS
R_S = .5Ω
RL = 1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced ripple rejection slowly degrades to that of a voltage-mode converter (-6.4dB for this example).

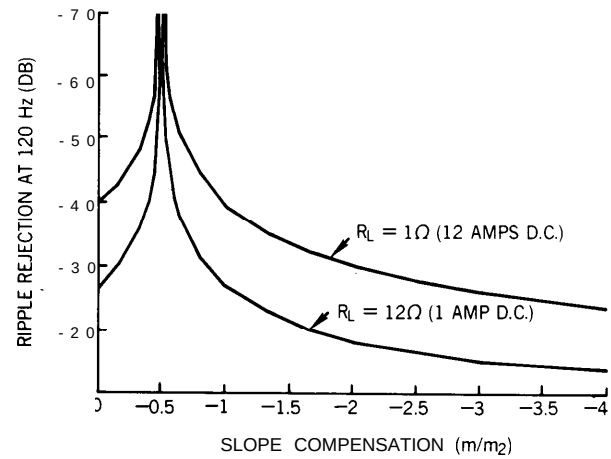


FIGURE 12 - RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used. as is the case for R_L = 1 ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}m_2$, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used. the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift

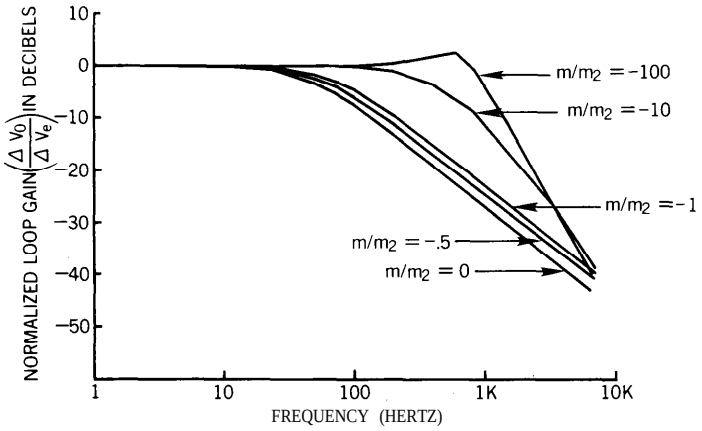
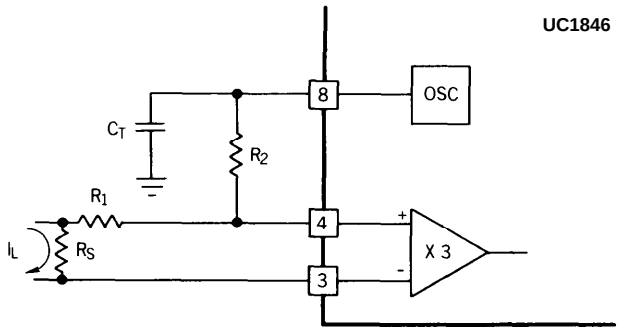
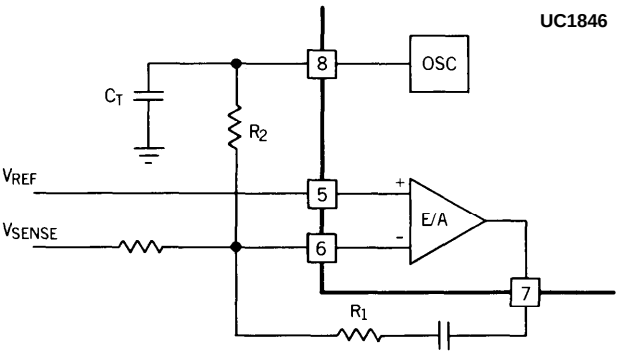


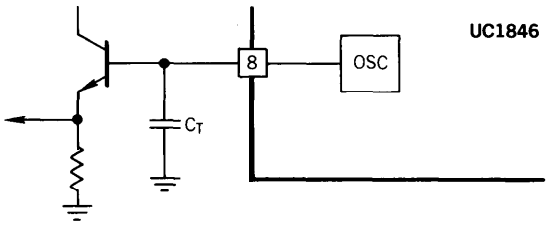
FIGURE 13 - NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 - ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

REFERENCES

(1) Shi-Ping Hsu, A. Brown, L. Rensink, R. Middlebrook "Modelling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current-Programmed Mode," PESC '79 Record (IEEE Publication 79CH1461-3 AES), pp. 284-301.

(2) E. Pivit, J. Saxarra, "On Dual Control Pulse Width Modulators for Stable Operation of Switched Mode Power Supplies", Wiss. Ber. AEG-Telefunken 52 (1979) 5, pp. 243-249.

(3) R. Redl, I. Novak "Instabilities in Current-Mode Controlled Switching Voltage Regulators," PESC '81 Record (IEEE Publication 81CH1652-7 AES), pp. 17-28.

(4) W. Bums, A. Ohri, "Improving Off-Line Converter Performance with Current-Mode Control," Powercon 10 Proceedings, Paper B-2, 1983.

(5) B. Holland, "A New Integrated Circuit for Current-Mode Control," Powercon 10 Proceedings, Paper C-2, 1983.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.