SwitcherPro Design Report
Schematic

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1V **Iout:** 3.02A

VIN

C1 Open
C9 4.7uF

U1
TPS54550

1 VIN
2 VIN
3 UVLO
4 PWRGD
5 RT
6 SYNC
7 SS/ENA
8 COMP

16 BOOT
15 PH
14 PH
13 LSG
12 VBIAS
11 PGND
10 AGND
9 VSENSE
PwrPad

C3 0.1uF
R10 24Ω
L1 4.7uH
Vout

Q1 CSD16321Q5
C10 8.2uF
C2 100uF

C4 1uF
Gnd

R18 10KΩ
R4 69.8KΩ

R1 10KΩ
R5 442Ω
C8 2700pF
R2 80.6KΩ

C6 8200pF
R3 3.57KΩ
C7 330pF

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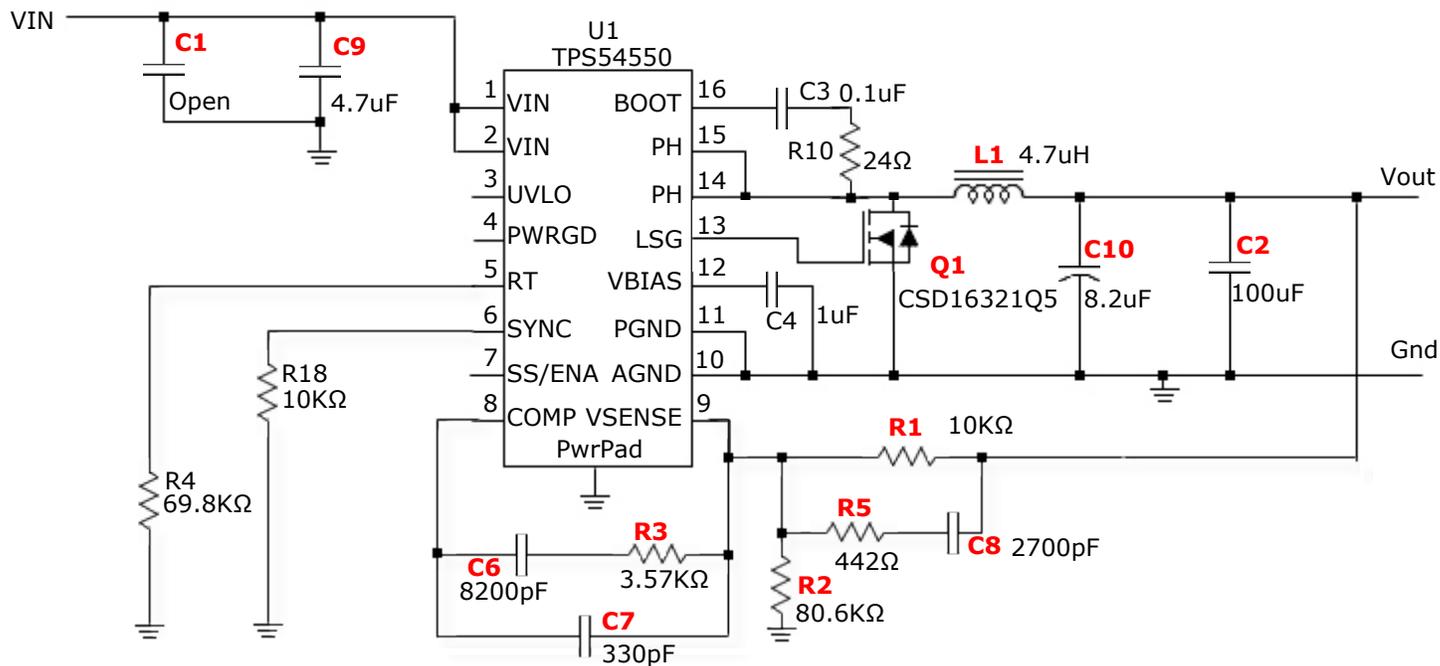
SwitcherPro Design Report
Analysis - Main

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1V **Iout:** 3.02A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	4.50	-	5.50	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	100	-	-	-	-	-	203.9
UVLO(Start) Volts - V	-	-	-	-	-	-	-	-	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	-	-
Switching Frequency KHz - KHz	-	700	-	-	-	-	560	700	840
Slow Start ms - ms	-	-	-	-	4.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	350	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	5

TEXAS INSTRUMENTS

SwitcherPro Design Report
Analysis - Output1

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1V **Iout:** 3.02A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	1.000	-	-	-	-	0.984	-	1.019
Output Ripple mVp-p - mVp-p	-	-	50	-	-	20	-	-	1.0
Output Current Amps - A	-	-	3.016	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.323	-	0.338
Current Limit Threshold Amps - A	-	-	-	-	4.200	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-20	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	62	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	63	-	68
Lower FET RDSon mOhms - mΩ	-	-	-	-	-	-	2	-	2
Duty Cycle % - %	-	-	-	-	-	-	20.1	-	24.8
On Time Min (switch) ns - ns	-	-	-	-	-	-	238.8	-	442.7
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	27	-

TEXAS INSTRUMENTS

SwitcherPro Design Report
Stress Results

Design Name: 5 to 1V0_MAX **Part:** TPS54550

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Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	25V	5.52V	3.5A	1.25A	-	3mW	-
C2 (Bulk Output Cap)	6.3V	1.01V	3.25A	98mA	-	19uW	-
C10 (Bulk Output Cap)	16V	1.01V	1.3A	0A	-	0W	-
L1 (Output Inductor)	-	-	4.1A	3.02A	-	182mW	-
Q1 (Sync. Rectifier)	25V	5.52V	100A	2.7A	-	108mW	29˚C
U1 (Converter)	21V	5.52V	9.5A	1.5A	-	367mW	40˚C

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SwitcherPro Design Report
Efficiency

Design Name: 5 to 1V0_MAX **Part:** TPS54550

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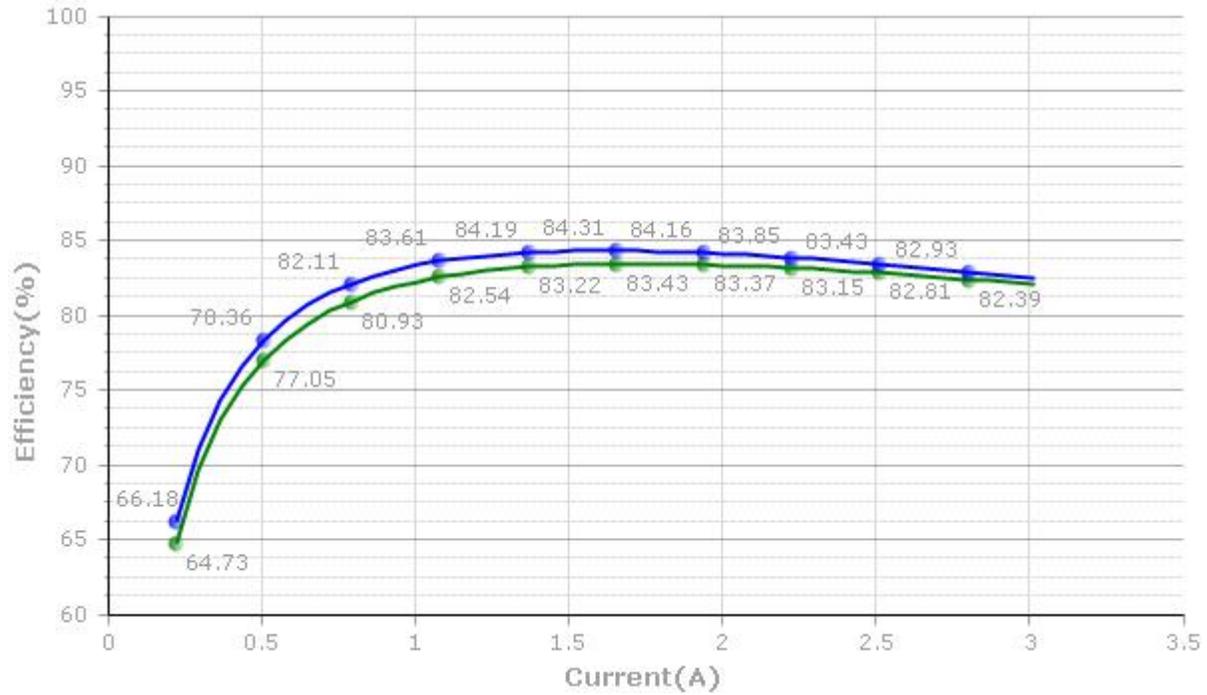
— Efficiency For Vin Max
— Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V   **VinMax:** 5.5V **Vout:** 1V   **Iout:** 3.02A
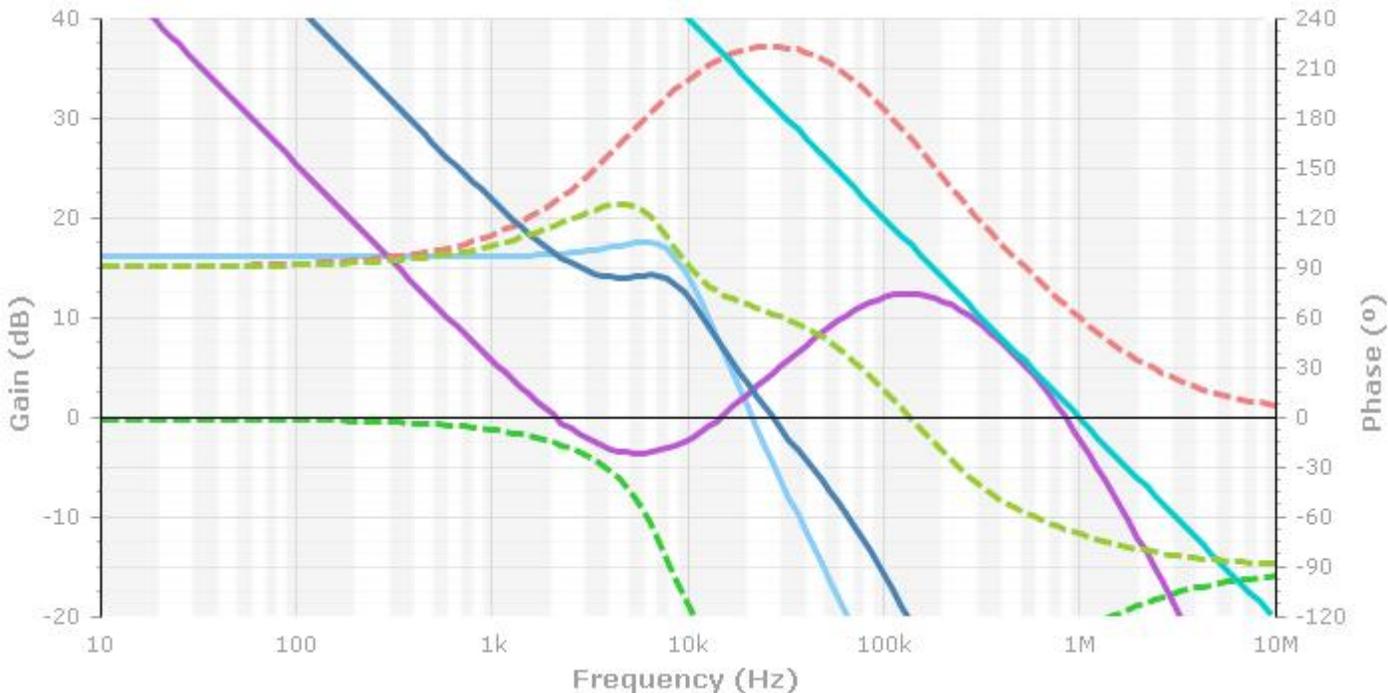
This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Maximum Load,and Maximum Capacitor ESR. To customize conditions use the 'What If Analysis' form

— Power Stage Gain
— Power Stage Phase
— Compensation Gain
— Compensation Phase
— Error Amp Gain
— Total Gain
— Total Phase

TEXAS INSTRUMENTS

SwitcherPro Design Report
Bill of Materials

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1V **Iout:** 3.02A

Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C10	1	EEFCD1C8R2R	Capacitor, NA, 8.2uF, 16V, 20%	Panasonic	EEFCD0	32	1
C2	1	C3225X5R0J107M	Capacitor, Ceramic, 100uF, 6.3V, 20%	TDK	C3225 1210	10	2
C3	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 1%	Standard	0603	2	1
C4	1	Standard	Capacitor, Ceramic, 1uF, 20V, 1%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 8200pF, 4V, 20%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 330pF, 4V, 20%	Standard	0603	2	1
C8	1	Standard	Capacitor, Ceramic, 2700pF, 4V, 20%	Standard	0603	2	1
C9	1	GRM21BR61E475MA12L	Capacitor, Ceramic, 4.7uF, 25V, 20%	Murata Manufacturing	0805	2.5	1.25
L1	1	CLF7045T-4R7N	Inductor, 4.7uH, 4.1A, 20mΩ	TDK	CLF10040	49.68	4.5
Q1	1	CSD16321Q5	Transistor, NFET, 25V, 100A, 3mΩ	Texas Instruments, Inc.	QFN 5x6	31	1
R1	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R10	1	Standard	Resistor, SurfaceMount, 24Ω, 100mW, 1%	Standard	0603	2	1
R15	1	Standard	Resistor, SurfaceMount, 0.0Ω, 100mW, 1%	Standard	0603	2	1
R18	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 80.6KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 3.57KΩ, 100mW, 1%	Standard	0603	2	1
R4	1	Standard	Resistor, SurfaceMount, 69.8KΩ, 100mW, 1%	Standard	0603	2	1
R5	1	Standard	Resistor, SurfaceMount, 442Ω, 100mW, 1%	Standard	0603	2	1
R7	1	Standard	Resistor, SurfaceMount, 0.0Ω, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54550	IC, Converter, 16 pins	Texas Instruments, Inc.	HTSSOP-Power PAD	34	2

TEXAS INSTRUMENTS

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Layout Image Not Available For this Part

TEXAS INSTRUMENTS

SwitcherPro Design Report
Layout Notes

Design Name: 5 to 1V0_MAX **Part:** TPS54550

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1V **Iout:** 3.02A

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and source of the low-side MOSFET. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the low-side MOSFET. The AGND and PGND pins should be tied to the PCB ground plane at the pins of the IC. The source of the low-side MOSFET should be connected directly to the PCB ground plane. The PH pins should be tied together and routed to the drain of the low-side MOSFET. Since the PH connection is the switching node, the MOSFET should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The recommended conductor width from pins 14 and 15 is 0.050 inch to 0.075 inch of 1-ounce to 2-ounce copper. The length of the copper land pattern should be no more than 0.2 inch. For operation at full rated load, the analog ground plane must provide adequate heat dissipating area. A 3-inch by 3-inch plane of copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the bottom or top layers also help dissipate heat, and any area available should be used when 5 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013-inch diameter vias to avoid solder wicking through the vias. Four vias should be in the PowerPAD area with four additional vias outside the pad area and underneath the package. Additional vias beyond those recommended to enhance thermal performance should be included in areas not under the device package.

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