Application Report
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Create an Inverting Power Supply Using Peak Current Mode Buck Converter

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ABSTRACT

The negative output voltage is required by applications such as operational amplifiers and a good solution is inverting buck-boost topology. This application report introduces the detailed design procedure to configure a Peak Current Mode (PCM) buck converter to the inverting buck-boost topology. The TPS560430 is a PCM buck converter with internal loop compensation, and it makes the design quite simple.

TPS560430 is introduced in Section 1. Section 2 provides the input voltage and output current ranges when a buck converter IC is configured as buck-boost topology. Section 3 provides the method to choose external components. A simple equation to calculate loop response is provided in this section, and it is used to design output capacitor. In Section 4, bench performance characteristics are provided.

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1 Introduction

The TPS560430 regulator is an easy to use synchronous step-down DC-DC converter operating from 4-V to 36-V supply voltage. It is capable of delivering up to 600-mA DC load current in a very small solution size. The family has different versions applicable for different applications, 1.1-MHz and 2.1-MHz switching frequency, PFM and FPWM, adjustable and fixed output voltage. The TPS560430 employs peak-current mode control with internal loop compensation, which reduces design time, and requires few external components.

A buck converter IC can be configured as inverting buck-boost topology, as shown in Figure 1. The GND pin of the original buck IC (GND_IC in the figure) is connected to V_O of the new system.

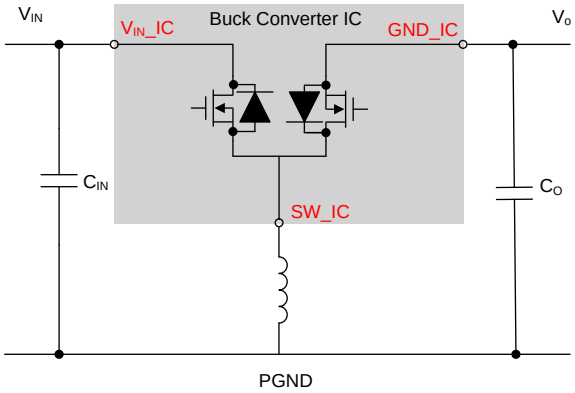

Figure 1. Configure a Buck Converter IC as Inverting Buck-Boost Topology

2 Specifications

When a buck converter IC is configured as inverting buck-boost topology, the maximum input voltage and output current decreases. The suitable buck IC needs to be chosen to satisfy the application requirement. The specification limit is calculated in this section. It should be pointed out that, V_O is negative in all the equations in this document.

2.1 Input Voltage Range

The difference in the maximum input voltage, output voltage should not exceed the maximum operating voltage of the device, see Equation 1. For TPS560430 the maximum operating voltage is 36 V. For example, when output is -12 V, the maximum input voltage of the inverting power supply is 24 V.

$$V_{IN\_max} \leq V_{IC\_max} + V_O \quad (1)$$

The minimum operating input voltage of the inverting power supply is the minimum device operating voltage, see Equation 2. For TPS560430 the minimum input voltage is 4V, so the inverting power supply input voltage must higher than 4 V.

$$V_{IN\_min} \geq V_{IC\_min} \quad (2)$$

2.2 Output Current Range

To estimate whether the selected switching regulator is capable of delivering the output current, use Equation 3. $I_{O\_IC\_max}$ is the maximum output current of the device ($I_{O\_IC\_max}$ = 0.6A for TPS560430). For TPS560430 the inverting power supply output current limit is calculated as shown in Figure 2. For example, if the minimum input voltage in the design spec is 4 V, the maximum output current is 0.15 A when V_O = -12 V.

$$I_{O\_max} \leq I_{O\_IC\_max} \times \frac{V_{IN\_min}}{V_{IN\_min} - V_O} \quad (3)$$

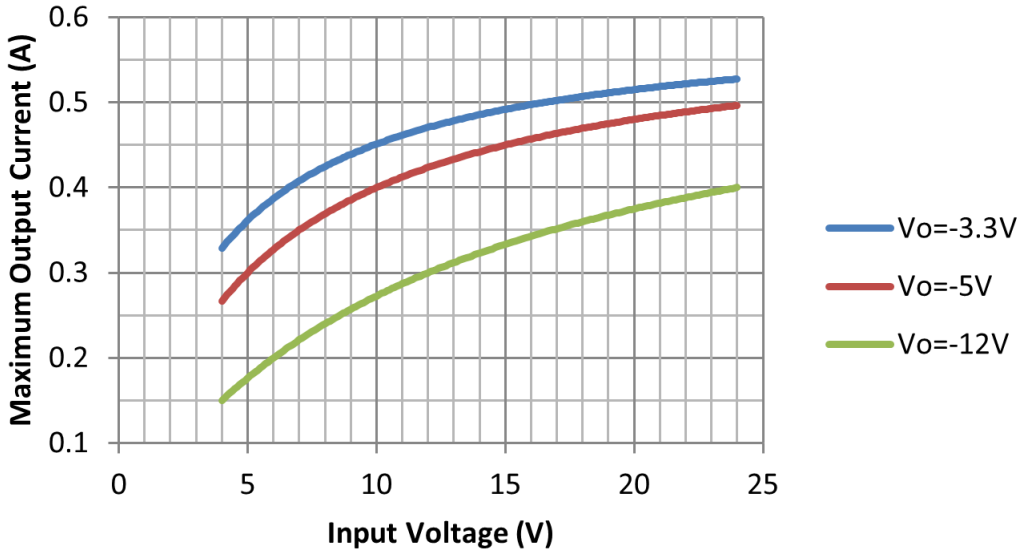

Figure 2. Maximum Output Current of the Inverting Power Supply

3 External Component Selection

In this section the inductor and output capacitor is designed in a practical application. The loop response is considered during the process. It should be pointed out that V_O is negative in all the equations.

Detailed design procedure is described based on a design example. For this design example, 1.1-MHz operating frequency, forced PWM (FPWM) version TPS560430XF is used with design specs as shown in Table 1.

Table 1. Design Example Specification

V_O (V)	V_{IN} (V)			I_O (A)	f_{SW} (kHz)	Output Voltage Ripple ΔV_O
	V_{IN_min}	V_{IN_norm}	V_{IN_max}			
-12	4	12	24	0.1	1100	0.5%*|V_O| = 60 mV

Figure 3 shows the reference design circuit.

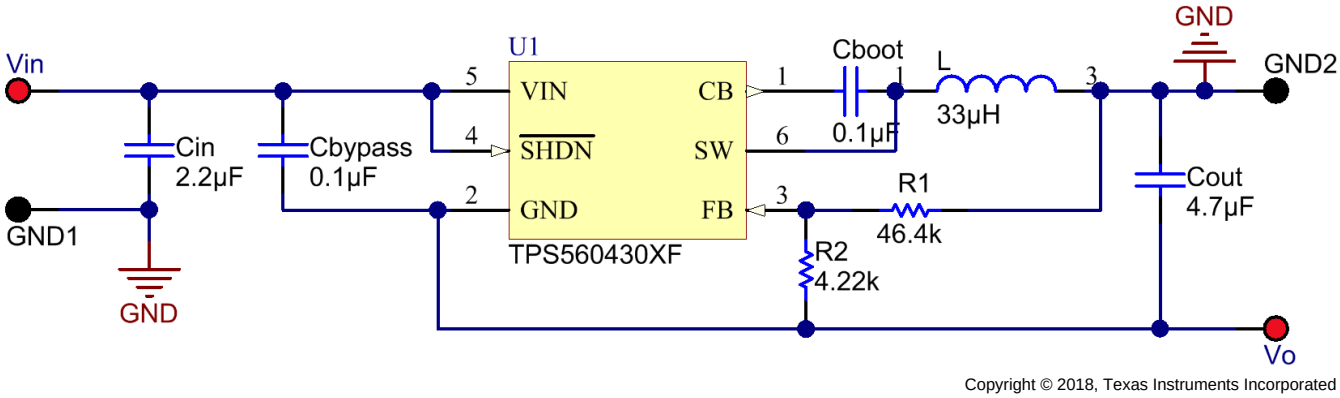

Figure 3. Design Example Circuit

3.1 Duty Cycle Calculation

Duty cycle is calculated using Equation 4. The maximum duty cycle is needed at the minimum input voltage. In this design example, D_{max} = 0.75 at V_{IN_min} = 4 V, D_{min} = 0.33 at V_{IN_max} = 24 V, D_{norm} = 0.5 at V_{IN_norm} = 12 V.

$$D = \frac{-V_O}{V_{IN} - V_O} \tag{4}$$

3.2 Output Voltage Set-Point

The output voltage of the TPS560430 device is externally adjustable using a resistor divider network. In this example, the divider network is comprised of R1 and R2. Equation 5 is used to determine the output voltage of the converter:

$$R1 = \frac{-V_O - V_{REF}}{V_{REF}} \times R2 \tag{5}$$

Choose the value of R2 to be 4.22 kΩ. With the desired output voltage set to -12 V and the V_{REF} = 1 V, the R1 value can then be calculated as 46.4 kΩ.

3.3 Inductor

To calculate the value of the output inductor, use Equation 6. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device: $I_{O\_IC\_max}$ ($I_{O\_IC\_max}$ = 0.6A for TPS560430). A reasonable value of K_{IND} should be 0.2 – 0.4. Since the ripple current increases with the input voltage, the maximum input voltage is used to calculate the minimum inductance L_{MIN}, while K_{IND} = 0.4 is selected. The minimum inductor value is calculated to be 30.3 µH. Choose the nearest standard inductor: L= 33 µH.

$$L_{min} = \frac{V_{IN\_max} \times D_{min}}{f_{SW} \times I_{O\_IC\_max} \times K_{IND}} \tag{6}$$

The TPS560430 is protected from over-current conditions by cycle-by-cycle current limit. To prevent inductor saturation in case of short circuit conditions, the inductor saturation current should be greater than the device maximum peak current limit, which is 1.4 A for TPS560430.

Select the inductor to satisfy the RMS current rating using Equation 7. The minimum V_{IN} is used to calculate the maximum RMS current, and the result is 0.4 A in this design example.

$$I_{L\_RMS} = \sqrt{\left(\frac{I_O}{1 - D_{max}}\right)^2 + \frac{1}{12} \times \left(\frac{V_{IN\_min} \times D_{max}}{f_{SW} \times L}\right)^2} \quad (7)$$

3.4 Output Capacitor

The output capacitor is designed considering output ripple and loop response. The output capacitor must supply the current when the high-side switch is on. Use the minimum input voltage to calculate the output capacitance needed, as shown in Equation 8. The maximum ESR of the output capacitor is calculated as shown in Equation 9 to satisfy the output ripple requirement. The target output ripple is 60 mV, so R_{ESR} < 136 mΩ and C_O > 1.1 µF. The capacitor needs to satisfy the RMS current rating, which is 0.17 A using Equation 10.

$$C_O > \frac{I_O \times D_{max}}{f_{SW} \times \Delta V_O} \quad (8)$$

$$R_{ESR} < \frac{\Delta V_O}{\frac{I_O}{1 - D_{max}} + \frac{V_{IN\_min} \times D_{max}}{2 \times f_{SW} \times L}} \quad (9)$$

$$I_{CO\_RMS} = I_O \times \sqrt{\frac{D_{max}}{1 - D_{max}}} \quad (10)$$

The selection of output capacitor directly determines the loop response in internally compensated converter. This article proposed a simple equation to calculate bandwidth and phase margin, which is derived in Appendix A. The conclusion is as Equation 30 to Equation 34. $R_O = -V_O / I_O = 120\ \Omega$ in this design example. With internal components value of TPS560430XF and considering 3 times margin, the output capacitor limit is as shown in Equation 11: C_O > 2 µF.

$$C_O > 3 \times \frac{D_{max} \times 9.54}{-\left(1 - D_{max}\right) V_O R_O} \times L \quad (11)$$

To summary, C_O > 2 µF and R_{ESR} < 136 mΩ is needed considering output voltage ripple and loop response. Consider of derating, one 4.7-µF, 25-V ceramic capacitor (part number 885012108020) is used. The capacitance after derating is 2.3 µF: C_O = 2.3 µF, R_{ESR} = 6 mΩ.

With internal components value of TPS560430XF, Equation 12 and Equation 13 are used to calculate bandwidth and phase margin. The loop response is calculated as Table 2 and it meets the design requirement.

$$f_c = \frac{\left(1 - D\right) \times 9.54}{-2\pi V_O C_O} \quad (12)$$

$$\begin{aligned}\text{PhaseMargin} &= 90^\circ - \arctan\left(\frac{2\pi f_C R_O C_O}{1+D}\right)\times\frac{180^\circ}{\pi} - \arctan\left(\frac{2\pi D f_C L}{(1-D)^2 R_O}\right)\times\frac{180^\circ}{\pi} \\ &- \arctan\left(\frac{2\pi f_C\left[D f_{SW} L\times 0.476 + (D-0.5)V_O\right]}{-V_O f_{SW}}\right)\times\frac{180^\circ}{\pi} + \arctan\left(2\pi f_C\times 26.5\mu\right)\times\frac{180^\circ}{\pi} \\ &- \arctan\left(2\pi f_C\times 1.06\mu\right)\times\frac{180^\circ}{\pi} + \arctan\left(2\pi f_C R_{ESR} C_O\right)\times\frac{180^\circ}{\pi}\end{aligned} \quad (13)$$

Table 2. Loop Response Calculation Results

V_{IN} (V)	I_O (A)	Crossover Frequency (kHz)	Phase Margin (°)
4	0.1	13.8	45.8
12	0.1	27.5	57.4
24	0.1	36.7	57.9

3.5 Input Capacitor

The input capacitors between V_{IN} and ground are used to limit the voltage ripple of the input supply. Equation 14 to Equation 16 are used to estimate the capacitance, maximum ESR, and current rating for the input capacitor. The target input ripple ΔV_{IN} is 2%*V_{IN_min}=80 mV, so ESR_{Cin} < 181 mΩ and C_{IN} > 0.85 µF. The RMS current rating is 0.17 A. Consider of derating, one 2.2-µF, 50-V ceramic capacitor is chosen. At V_{IN_max} = 24 V, the capacitance after derating is 1.4 µF, while ESR_{Cin} = 7 mΩ.

$$C_{IN} > \frac{I_O \times D_{max}}{f_{SW}\times\Delta V_{IN}} \quad (14)$$

$$ESR_{Cin} < \frac{\Delta V_{IN}}{\frac{I_O}{1-D_{max}} + \frac{V_{IN\_min}\times D_{max}}{2\times f_{SW}\times L}} \quad (15)$$

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{D_{max}}{1-D_{max}}} \quad (16)$$

3.6 Bypass Capacitor

The TPS560430 needs a tightly coupled, ceramic bypass capacitor, connected to the V_{IN} and GND pin of the device. Because the device GND is the power supply output voltage, the voltage rating of the capacitor must be greater than the differences in the maximum input and output voltage of the power supply, which is 36 V in this design example. One 0.1-µF, 50-V ceramic capacitor is chosen for high-frequency filtering and place it as close as possible to the device pins.

3.7 Bootstrap Capacitor

Every TPS560430 design requires a bootstrap capacitor. The recommended bootstrap capacitor is 0.1 µF and rated at 16 V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

4 Evaluation Results

4.1 Typical Performance

Figure 4 to Figure 13 show the experimental test results of the Figure 3 design. Unless otherwise specified, the following conditions apply: V_{IN} = 12 V, V_O = -12 V, I_O = 0.1 A, T_A = 25 °C.

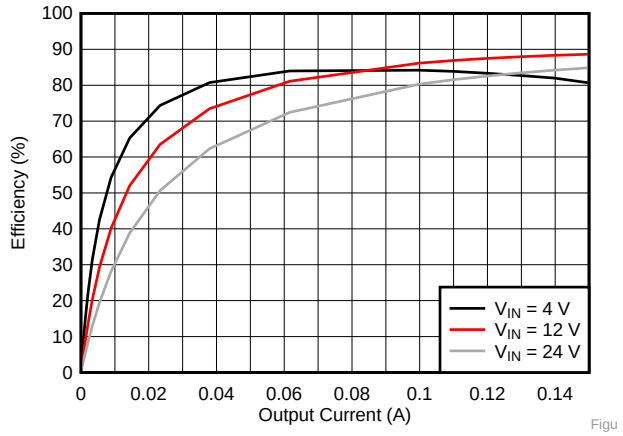

Figure 4. Efficiency vs Load Current

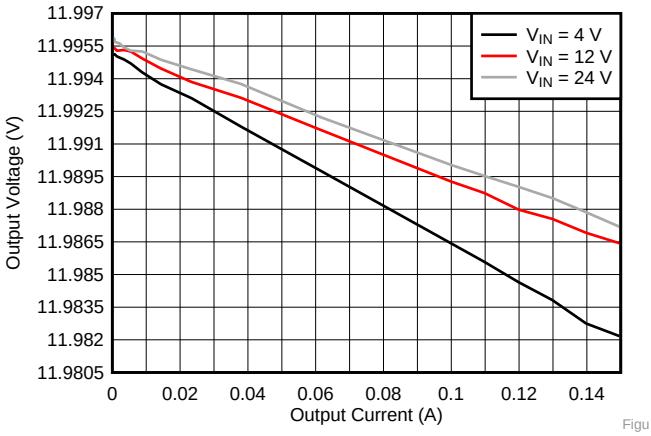

Figure 5. Load Regulation

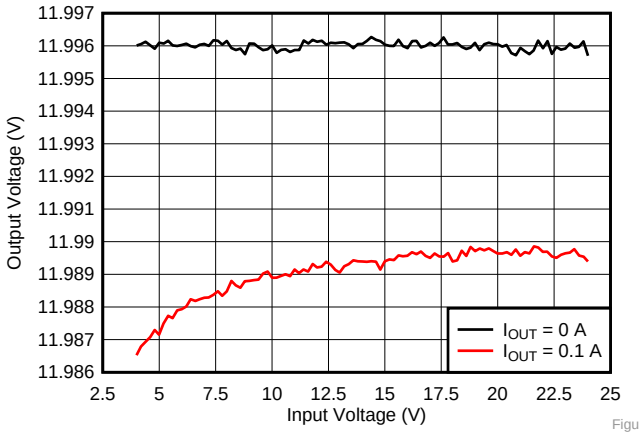

Figure 6. Line Regulation

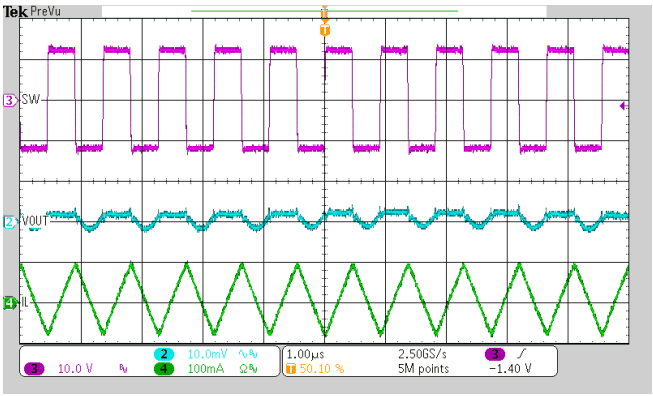

Figure 7. Output Voltage Ripple at No Load

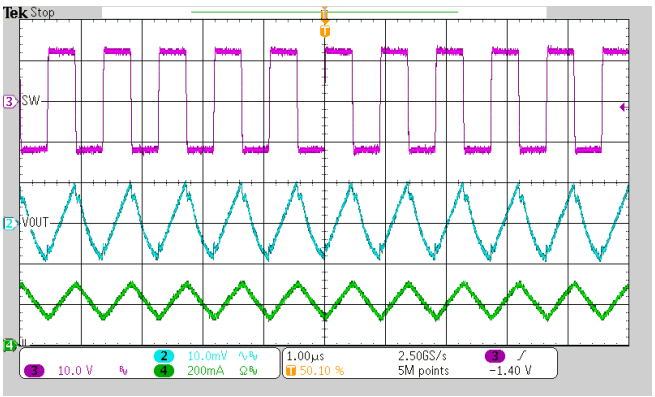

Figure 8. Output Voltage Ripple at 0.1A

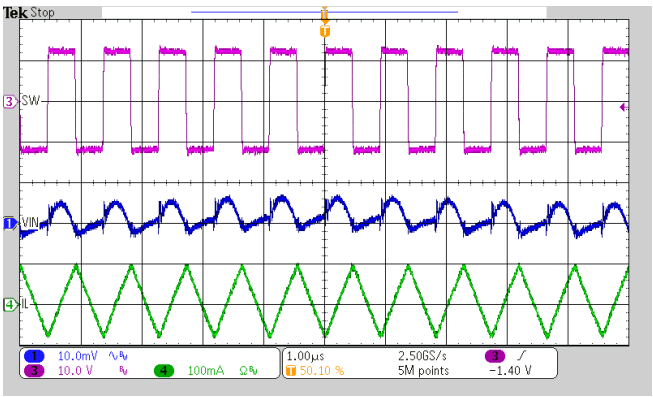

Figure 9. Input Voltage Ripple at No Load

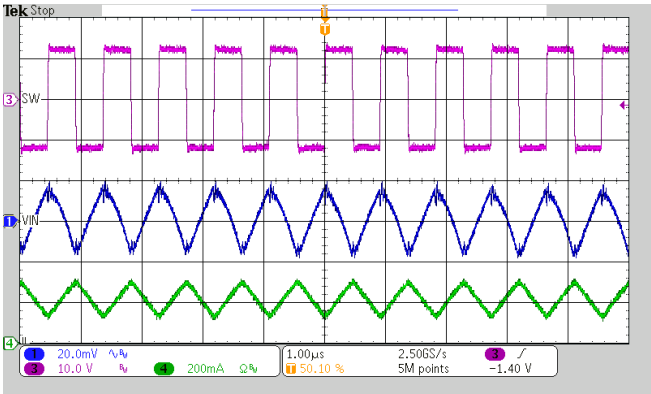

Figure 10. Input Voltage Ripple at 0.1A

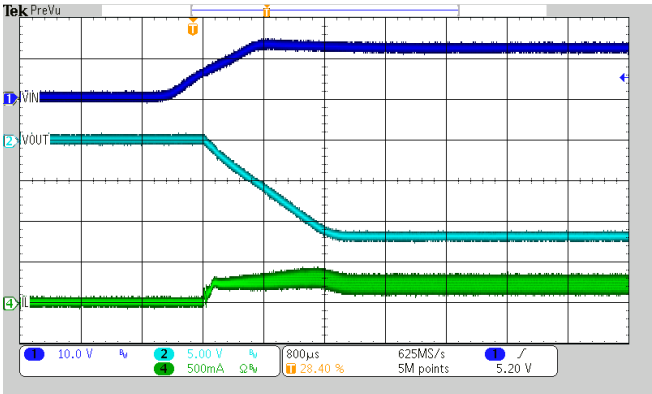

Figure 11. Start Up by V_{IN}

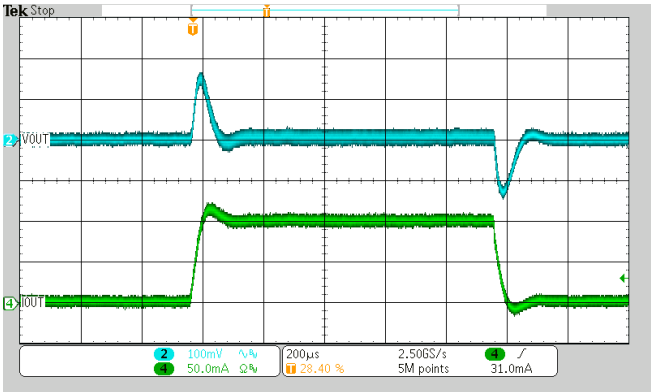

Figure 12. Load Transient

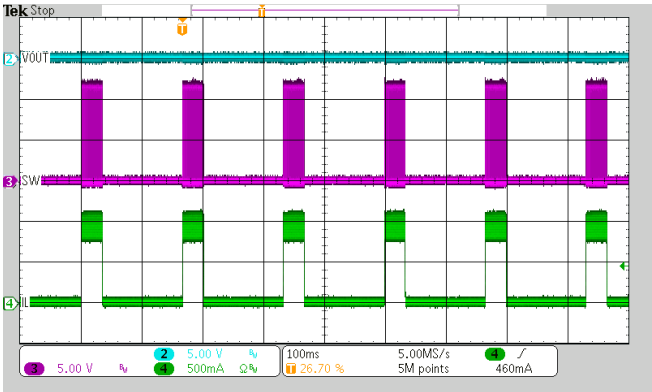

Figure 13. Short Protection

4.2 Loop Response Simulation and Bench Verification

SIMPLIS is used to simulate the loop response as Figure 14. Figure 15 and Figure 16 are the loop response from SIMPLIS simulation and bench test under V_{IN} = 12 V, V_O = -12 V, I_O = 0.1 A, f_{SW} = 1.1 MHz. The comparison of calculation results, simulation results and bench measurement at different V_{IN} is given in Table 3. It can be seen that the proposed model in this application report is accurate.

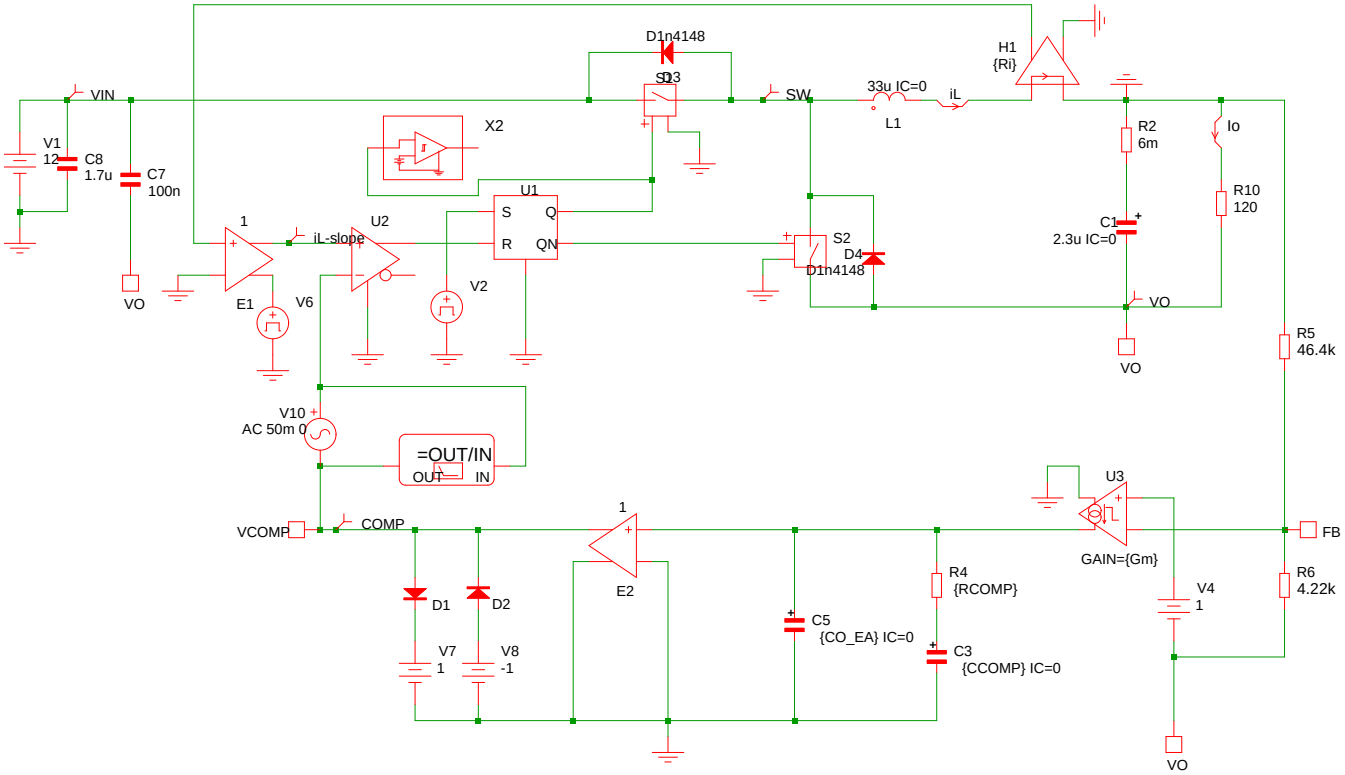

Figure 14. Schematic of Simplified SIMPLIS Model

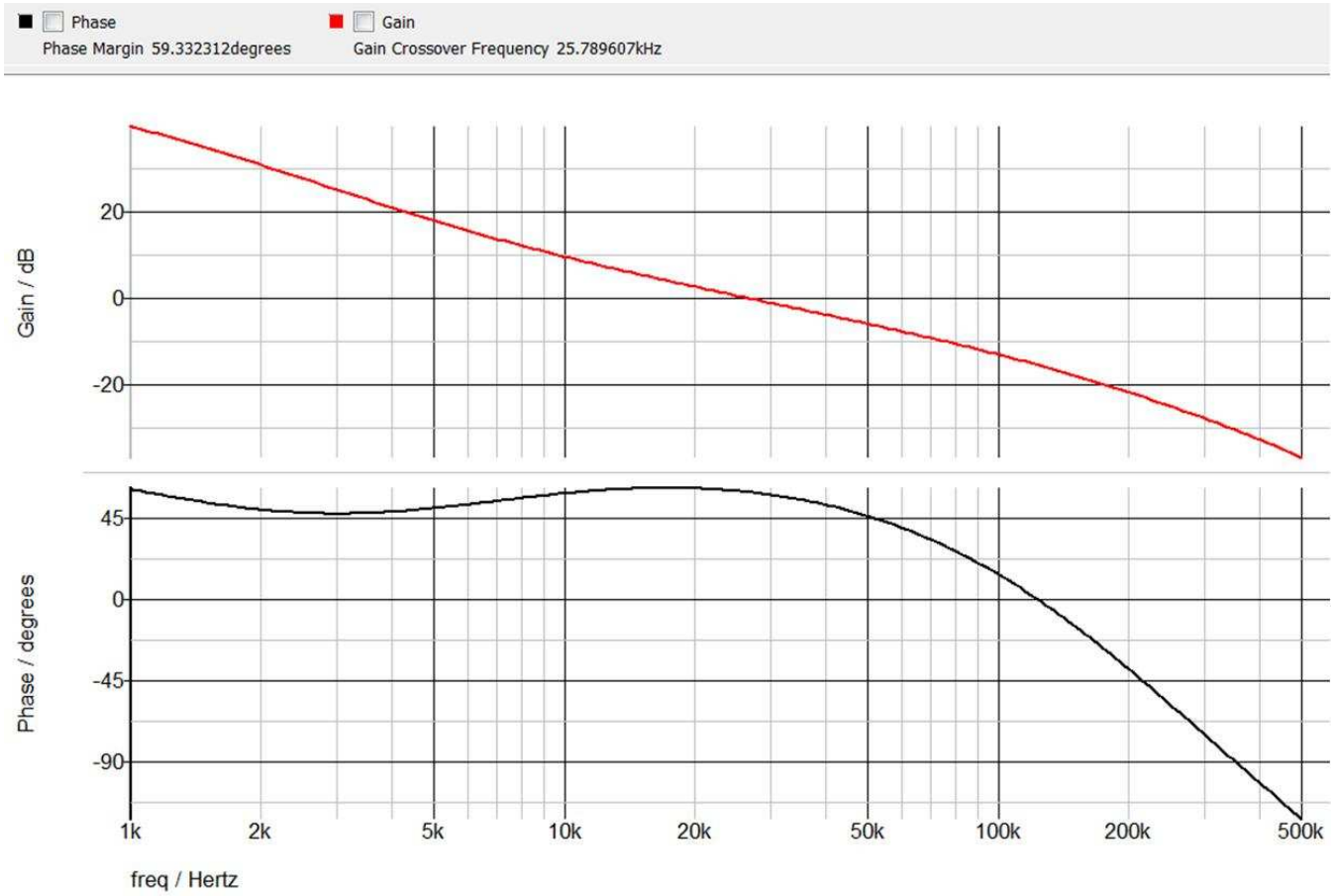

Figure 15. Bode Plot Simulation Result at V_{IN} = 12 V, I_O = 0.1 A

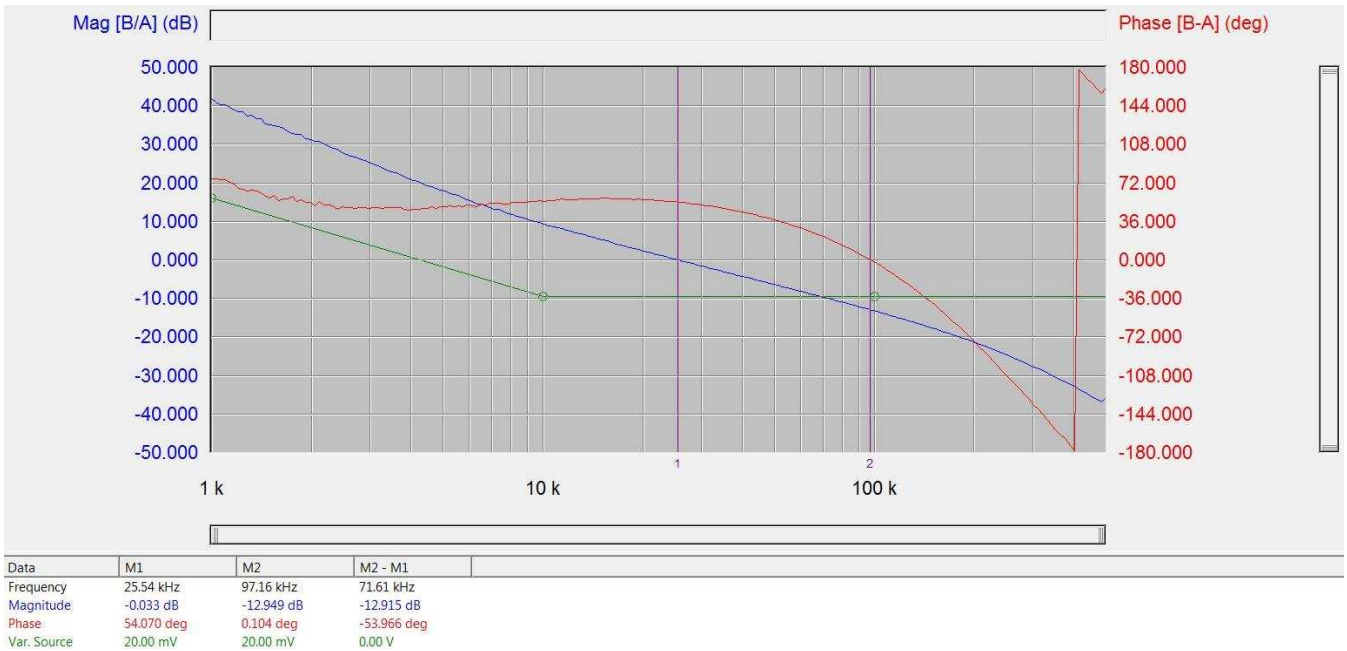

Figure 16. Bode Plot Test Result at V_{IN} = 12 V, I_O = 0.1 A

Table 3. Calculation, Simulation and Bench Measurement Results Comparison

V_{IN} (V)	I_O (A)	Calculation Results		Simulation Results		Bench Measurement	
		f_c (kHz)	Phase Margin (°)	f_c (kHz)	Phase Margin (°)	f_c (kHz)	Phase Margin (°)
4	0.1	13.8	45.8	14.3	46	13.3	41.2
12	0.1	27.5	57.4	25.8	59.3	25.5	54.1
24	0.1	36.7	57.9	33.5	60.7	32.5	57.9

5 References

1. Texas Instruments, *TPS560430 4-V to 36-V, 600-mA Synchronous Step-Down Converter Data Sheet*
2. Texas Instruments, *Create an Inverting Power Supply Using a Synchronous Step-Down Regulator*
3. Texas Instruments, *Create an Inverting Power Supply From a Step-Down Regulator*
4. Texas Instruments, *Achieving High-Efficiency with a Multi-Output CCM Flyback Supply Using Self-Driven Synchronous Rectifiers*
5. R.B. Ridley, *A New Small-Signal Model for Current-Mode Control*, PhD Dissertation, Virginia Polytechnic Institute and State University, November, 1990.

A Simple Equation to Calculate Loop Response of Peak Current Mode Buck Boost Converter

A.1 Introduction

PCM control has been widely used in buck-boost converters for many years and lots of loop models are available for system design. In [2] to [4], the first order model is used due to its simplicity, but the high frequency accuracy is bad, resulting in big phase margin error. Besides, it can't predict current loop instability. The most popular model is provided by R. Ridley [5]. The model predicted the sample and hold effects in the current loop. However, the model requires simulation tools to draw the bode plot, then find crossover frequency and phase margin based on the bode plot. Besides, the transfer function of inner current loop is quite complex, making it hard to understand how each component value impact the whole loop response.

In this document, a simple equation to calculate bandwidth and phase margin is obtained by simplifying the inside current loop as a single pole. Each zero and pole in the model has a clear physical meaning, making it easy to analyze the impact of each component value on the loop response. The inductor and output capacitor design procedure of internally compensated PCM buck converter is given using the model. The model accuracy is verified by both simulation and bench measurement results.

A.2 Overall Control Block Diagram and Transfer Function Derivation

Figure 17 shows the simplified schematic for the PCM buck-boost converter.

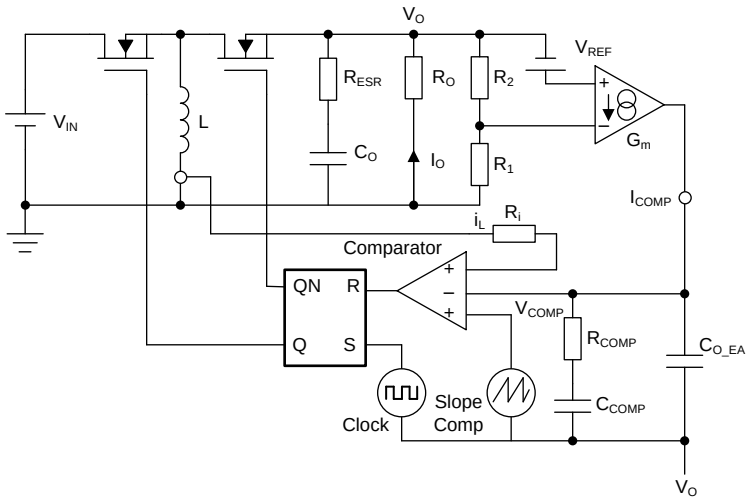

Figure 17. Simplified Schematic for PCM Buck-Boost Converter

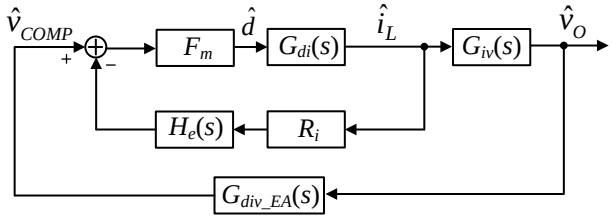

Figure 18. Overall Control Implementation

Figure 18 is the overall control block model.

Where:

- $G_{di}(s)$ is the duty cycle to inductor current transfer function
- $G_{iv}(s)$ is the inductor current to output voltage transfer function
- F_m is the gain of PCM PWM comparator
- R_i is the current sensing resistor
- $H_e(s)$ is the transfer function model of inductor current sampling-hold effect
- $G_{div\_EA}(s)$ is the output voltage to compensation voltage transfer function. It includes the feedback resistor network and the error amplifier with certain compensation

$G_{iv}(s)$ and $G_{di}(s)$ is relating to the power stage small signal model. They are derived using three-terminal switch model [4]. The transfer function from inductor current to output voltage is shown in Equation 17.

$$G_{iv}(s) = \frac{\hat{v}_O(s)}{\hat{i}_L(s)} = -\frac{(1-D)R_O}{(1+D)} \frac{\left(1+\frac{s}{w_{Z1\_iv}}\right)\times\left(1+\frac{s}{w_{Z2\_iv}}\right)}{\left(1+\frac{s}{w_{P1\_iv}}\right)} \tag{17}$$

Where:

$$w_{Z1\_iv} = -\frac{(1-D)^2 R_O}{DL}$$

$$w_{Z2\_iv} = \frac{1}{R_{ESR}C_O}$$

$$w_{P1\_iv} = \frac{1+D}{R_O C_O}$$

$G_{di}(s)$ is the duty cycle to inductor current transfer function, see Equation 18.

$$G_{di} = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{IN}\left(1+D+sC_O R_O\right)}{(1-D)\left[(1-D)^2 R_O + sL + s^2 LC_O R_O\right]} \tag{18}$$

The internal loop compensation is designed so that the crossover frequency is much higher than (1-D)/(2π√LC$_O$). For crossover frequency and higher frequency, Equation 18 can be simplified as Equation 19.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} \approx \frac{V_{IN}}{(1-D)sL} \tag{19}$$

The sensed inductor current, external ramp and the output of error amplifier V_{COMP} are compared, which determines when to turn off the high side MOSFET, hence the duty cycle is determined. F_m is the comparator gain, see Equation 20. f_{SW} is the switching frequency. S_n is the on-time slope of the sensed-current waveform and S_e is the external ramp slope.

$$F_m = \frac{f_{SW}}{S_n + S_e} \tag{20}$$

Where:

$$S_n = R_i \frac{V_{IN}}{L}$$

$$S_e = V_{Se} \times f_{SW}$$

$H_e(s)$ is the transfer function model of inductor current sampling-hold effect [5], see Equation 21.

$$H_e(s) = \frac{s/f_{SW}}{e^{s/fSW} - 1} \approx 1 - \frac{s}{2f_{sw}} + \frac{s^2}{(\pi f_{sw})^2} \tag{21}$$

$G_{div\_EA}(s)$ is the output voltage to compensation voltage transfer function, see Equation 22. It includes the feedback resistor network and the error amplifier with certain compensation.

$$G_{div\_EA}(s) = \frac{\hat{v}_{COMP}(s)}{\hat{v}_O(s)} = \frac{V_{REF}}{-V_O} \frac{G_m}{C_{COMP}} \frac{1 + sR_{COMP}C_{COMP}}{s(1 + sR_{COMP}C_{CO\_EA})} \tag{22}$$

A.3 Inside Current Loop Model

Based on Equation 19 to Equation 21 and Figure 18, the transfer function from compensation voltage to inductor current is $G_{ci}(s)$, see Equation 23.

$$G_{ci}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)} = \frac{1}{R_i} \frac{1}{1 + s \times \left[\frac{DV_{Se}f_{SW}L + (D-0.5)R_iV_O}{-R_iV_Of_{SW}}\right] + s^2 \times \frac{1}{(\pi f_{SW})^2}} \tag{23}$$

For PCM buck-boost converter, the crossover frequency is much smaller than half switching frequency, so around crossover frequency Equation 23 can be simplified as Equation 24. The inside current loop is simplified as a single pole, which is very helpful for the loop response analysis of PCM buck-boost converter.

$$G_{ci}(s)=\frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)}=\frac{1}{R_i}\frac{1}{1+s\times\left[\frac{DV_{Se}f_{SW}L+(D-0.5)R_iV_O}{-R_iV_Of_{SW}}\right]} \quad (24)$$

A.4 Overall Loop Model

Based on Equation 17, Equation 22 and Equation 24, the open loop transfer function L(s) around crossover frequency is obtained, see Equation 25. f_{Z_EA} ,f_{P_EA} are zeros and poles introduced by the error amplifier with certain compensation. f_{Z1_iv}, f_{Z2_iv}, f_{P1_iv} are zeros and poles introduced by the power stage inductor current to output voltage transfer function. f_{P_ci} is the simplified pole introduced by the inside current loop.

$$L(s)=-G_{iv}(s)\times G_{div\_EA}(s)\times G_{ci}(s)=K\frac{\left(1+\frac{s}{2\pi f_{Z1\_iv}}\right)\times\left(1+\frac{s}{2\pi f_{Z2\_iv}}\right)\times\left(1+\frac{s}{2\pi f_{Z\_EA}}\right)}{s\times\left(1+\frac{s}{2\pi f_{P1\_iv}}\right)\times\left(1+\frac{s}{2\pi f_{P\_EA}}\right)\times\left(1+\frac{s}{2\pi f_{P\_ci}}\right)} \quad (25)$$

Where:

$$K=\frac{(1-D)R_OV_{REF}G_m}{-(1+D)R_iV_OC_{COMP}}$$

$$f_{Z1\_iv}=-\frac{(1-D)^2R_O}{2\pi DL}$$

$$f_{Z2\_iv}=\frac{1}{2\pi R_{ESR}C_O}$$

$$f_{P1\_iv}=\frac{1+D}{2\pi R_OC_O}$$

$$f_{Z\_EA}=\frac{1}{2\pi R_{COMP}C_{COMP}}$$

$$f_{P\_EA}=\frac{1}{2\pi R_{COMP}C_{O\_EA}}$$

$$f_{P\_ci}=\frac{-R_iV_Of_{SW}}{2\pi\left[DV_{Se}f_{SW}L+(D-0.5)R_iV_O\right]}$$

A.5 Inductor and Output Capacitor Design Limits

With proper inductor and output capacitor design, the Bode plot is as shown in Figure 19. $f_{P1\_iv} \ll f_c$, $f_{Z\_EA} \ll f_c$, $f_{P\_ci} \gg f_c$, $|f_{Z1\_iv}| \gg f_c$, $f_{P\_EA} \gg f_c$, $f_{Z2\_iv} \gg f_c$.

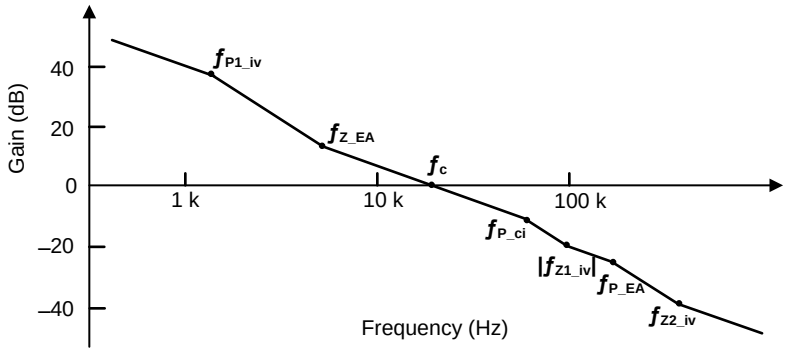

Figure 19. Bode Plot Model for PCM Buck-Boost Converter

The gain curve should go across 0dB with -20dB/dec slew rate, so that the phase margin is enough. The zero introduced by the compensation network f_{Z_EA} cancels the pole of output impedance f_{P1_iv}, and they are placed before crossover frequency: $f_{P1\_iv} \ll f_c$, $f_{Z\_EA} \ll f_c$. The parasitic capacitor of error amplifier C_{O_EA} is quite small, so $f_{P\_EA} \gg f_c$.

f_{Z1_iv} is calculated to be a negative value, which means it is a right half plan zero. The right half plane zero introduces an increasing gain and a decreasing phase, which may cause lower phase margin and instability. It is recommended to keep cross over frequency much lower than the right half plane zero, so that the right half plane zero doesn't affect the overall loop significantly: $|f_{Z1\_iv}| \gg f_c$. The maximum inductor value is calculated, see Equation 26.

$$L << \frac{\left(1-D\right)^2 R_O}{2\pi D f_c} \tag{26}$$

If L is too large, the pole introduced by the current loop f_{P_ci} will be smaller than the crossover frequency f_c. The gain curve will go across 0dB with -40dB/dec slew rate, and the phase margin will not be enough. To prevent that happens, L should be properly designed to ensure $f_{P\_ci} \gg f_c$. The maximum inductor value is calculated, see Equation 27.

$$L << \frac{-V_O R_i}{2\pi D f_c V_{Se}} - \frac{\left(D-0.5\right) V_O R_i}{D V_{Se} f_{SW}} \tag{27}$$

If the Equivalent Series Resistance (ESR) of output capacitor is too large, the zero introduced by output capacitor f_{Z2_iv} will be smaller than the crossover frequency f_c. The gain curve will have 0dB/dec slew rate after f_{Z2_iv}, which will make the crossover frequency too large. Some high frequency poles introduced by the parasitic parameters in the IC will influence the phase margin, and the phase margin will not be enough. To prevent that happens, ESR of output capacitor should be properly designed to ensure $f_{Z2\_iv} \gg f_c$. The maximum ESR is calculated, see Equation 28.

$$R_{ESR} << \frac{1}{2\pi f_c C_O} \tag{28}$$

A.6 The Equation to Calculate Bandwidth and Phase Margin

From Equation 25 and considering $f_{P1\_iv} \ll f_c$, $f_{Z\_EA} \ll f_c$, $f_{P\_ci} \gg f_c$, $|f_{Z1\_iv}| \gg f_c$, $f_{P\_EA} \gg f_c$, $f_{Z2\_iv} \gg f_c$, the magnitude of open loop transfer function at crossover frequency f_c is shown in Equation 29.

$$\left|L\left(j2\pi f_c\right)\right| = K\frac{\left|1+j\frac{f_c}{f_{Z1\_iv}}\right| \times \left|1+j\frac{f_c}{f_{Z2\_iv}}\right| \times \left|1+j\frac{f_c}{f_{Z\_EA}}\right|}{2\pi f_c \times \left|1+j\frac{f_c}{f_{P1\_iv}}\right| \times \left|1+j\frac{f_c}{f_{P\_EA}}\right| \times \left|1+j\frac{f_c}{f_{P\_ci}}\right|} \approx K \times \frac{\frac{f_c}{f_{Z\_EA}}}{2\pi f_c \times \frac{f_c}{f_{P1\_iv}}} = 1 \tag{29}$$

Considering usually $R_{ESR} \ll R_O$, the crossover frequency f_c is obtained, see Equation 30.

$$f_c = \frac{\left(1-D\right)V_{REF}G_m R_{COMP}}{-2\pi V_O R_i C_O} \tag{30}$$

Phase margin is the phase of open loop transfer function at f_c minus -180º, see Equation 31.

$$\begin{aligned}&\text{PhaseMargin}\\ &= 90° - \arctan\left(\frac{2\pi f_c R_O C_O}{1+D}\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_C R_{COMP} C_{COMP}\right) \times \frac{180°}{\pi}\\ &- \arctan\left(\frac{2\pi D f_C L}{\left(1-D\right)^2 R_O}\right) \times \frac{180°}{\pi} - \arctan\left(\frac{2\pi f_C\left[DV_{Se} f_{SW} L + \left(D-0.5\right)R_i V_O\right]}{-R_i V_O f_{SW}}\right) \times \frac{180°}{\pi}\\ &- \arctan\left(2\pi f_C R_{COMP} C_{O\_EA}\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_C R_{ESR} C_O\right) \times \frac{180°}{\pi}\end{aligned} \tag{31}$$

Substitute Equation 30 into Equation 26 to Equation 28, inductor and output capacitor design limits is obtained, see Equation 32 to Equation 34. It is suggested to have 3 times margin when choosing inductor and output capacitor values.

$$C_O >> \frac{DV_{REF}G_m R_{COMP}}{-\left(1-D\right)V_O R_i R_O} \times L \tag{32}$$

$$C_O >> \left[L + \frac{\left(D-0.5\right)V_O R_i}{DV_{Se} f_{SW}}\right] \times \frac{D\left(1-D\right)V_{REF}G_m R_{COMP} V_{Se}}{V_O^2 R_i^2} \tag{33}$$

$$R_{ESR} << \frac{-V_O R_i}{\left(1-D\right)V_{REF}G_m R_{COMP}} \tag{34}$$

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