# UCC28950, UCC28951 Debug

The best way to start to debug a PSFB using the UCC28951 is to apply the bias supplies to the control circuit while keeping the DC input to the power stage very low, <5% of nominal or less for example (about 20V on a nominal 400V input). The controller does not have an undervoltage lock out on the input voltage and so it will operate at Dmax. Vout will be low but it allows you to check the gate drives, MOSFET switching and the voltages across the transformer primary and secondary while reducing the possibility of catastrophic power stage damage.

1/ Defeat the Synchronous rectifiers by removing their gate drive resistors and tying their gates to their sources. The SRs will operate as diodes.

2/ Put ‘scope probes at the OUTA, OUTB, OUTC and OUTD pins

3/ Set the input voltage to the power stage to zero

4/ Apply Vcc to the UCC28951 controller

5/ Measure the switching frequency of OUTx – is it what you expect. Duty cycle on OUTx should be 50% (less the dead times set by the resistors at the DELAB and DELCD pins)

6/ Turn the controller off. Move the ‘scope probes to QB\_Gate, QD\_gate, QB\_Drain, QD\_Drain

7/ Apply Vcc to the controller and increase Vin to the power stage slowly. Observe the waveforms on the ‘scope. The gates should be driven with the expected voltage and the drains should switch cleanly from 0V to Vin.

8/ Turn off Vcc and Vin. Change the probe at QB\_Gate to monitor the CS pin – you should use a ‘tip and barrel’ method to do this.



9/ Reapply Vcc and slowly increase Vin to about 50V and then apply a load to the power stage. Observe the CS signal. Is it ‘clean’

10/ Once operation at a very low input voltage is confirmed then increase the input voltage in steps until Vout is at about 50% of its setpoint. Then increase the load current to about 25% of its full load value. At this point you should check that the OUTE and OUTF gate drives are active and correct. Check the waveforms across the output rectifiers. Are there any excessive spikes or poorly damped overshoots on the leading or trailing edges of the waveforms. Check the current sense waveform that is delivered to the CS pin. Noise spikes induced on this pin can trip the PWM comparator prematurely – causing Vout to drop, among other things.

11/ Reconnect the SR gate drives and repeat the steps above. The SR drives won’t activate until the load current is high enough to bring the DCM pin above the DCM threshold.

12/ Increase the input voltage in steps until the output voltage is just below the regulation setpoint. Increase the load current to about 50% of full load. Repeat the checks above.

13/ Verify ZVS on the QA/QB switches. The easiest way to do this is to observe the Vgs of the QB switch. The absence of a Miller Plateau on the gate voltage indicates ZVS is being achieved.

14/ Verify ZVS on the QC/QD switches. The easiest way to do this is to observe the Vgs of the QD switch. The absence of a Miller Plateau on the gate voltage indicates ZVS is being achieved.

15/ Slowly increase Vin until the Vout reaches its setpoint – at this time the duty cycle should start to reduce from Dmax as the controller begins to regulate the output.

16/ Slowly increase Vin until it is at its nominal value. Check the duty cycle is stable – the easiest way to do this is to observe the CS signal.

17/ Check efficiency, voltage regulation, current limiting, burst mode etc.