Trouble shootings for TI PSR controllers

Meeting troubles in the debugging process is very common for power supply designers. The troubles may include smoke when you first power the supply or it doesn't start up at all without any light or noise. The fundamentals of debugging should be to make sure the components are assembled right as the schematic and no wrong connections in the PCB[1]. In this paper, I will assume that you have checked the board and have repaired the failure components. We will focus on the design issues in the remainder of the application note. This application note can be used for TI's primary-side regulated (PSR) controllers and switchers such as UCC2870X, UCC2871X, UCC2872X, and UCC2891X.

Background

Table 1 is a comparison table for TI's PSR controllers and switchers. We will note there are minor differences however the control laws and working principles are similar.

Table 1. Comparison table for TI PSR parts

TI PSR Part	HV Start	Output Drive for
UCC2870X	No	MOSFET
UCC2871X	Yes	MOSFET
UCC28720	Yes	BJT
UCC28722	No	BJT
UCC28730	Yes	MOSFET
UCC2891X	Yes	Integrated MOSFET

We use Figure 1 as a simplified basic reference circuit for the description in this application note. Please be noted that the part used in Figure 1 is UCC28700. If using other parts, there would be minor differences in the circuit. But it will not affect the troubleshooting. Also note that primary and secondary snubbers are not shown.

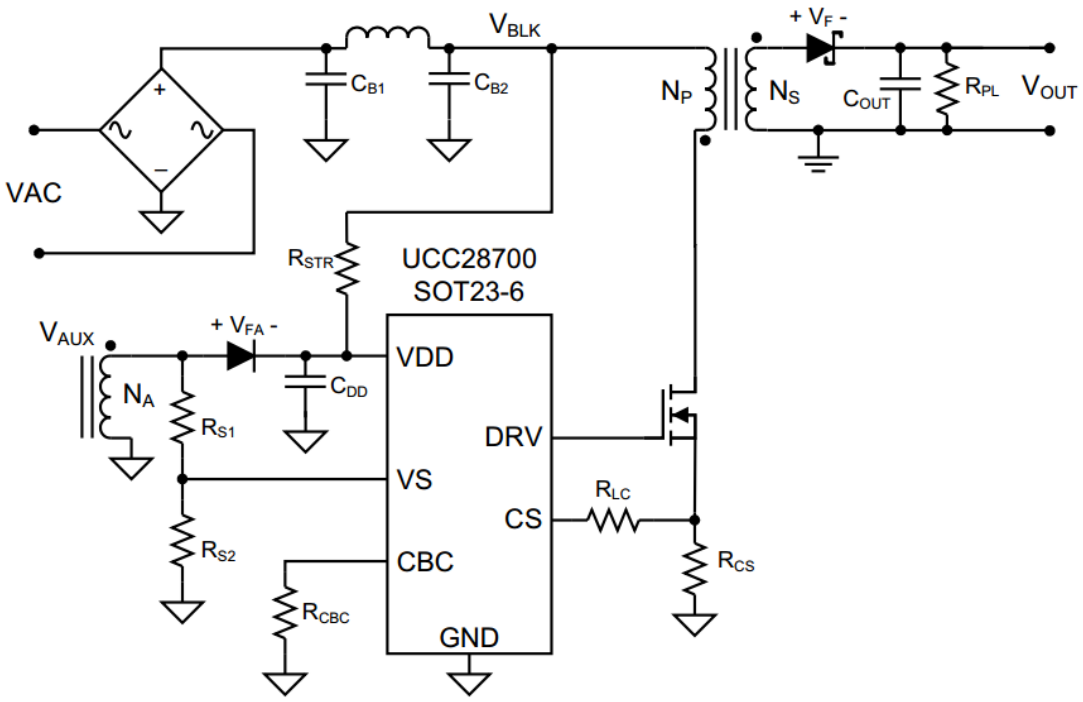

Figure 1. Simplified Typical TI PSR Flyback Application

Issue 1: The power converter cannot startup or shutdown unexpected

Cause 1: VDD UVLO

Phenomenon:

Before VDD goes down to $V_{VDD(off)}$, there are switching pulses with which the frequency is higher than minimum frequency $F_{sw(min)}$ as shown in Figure 2.

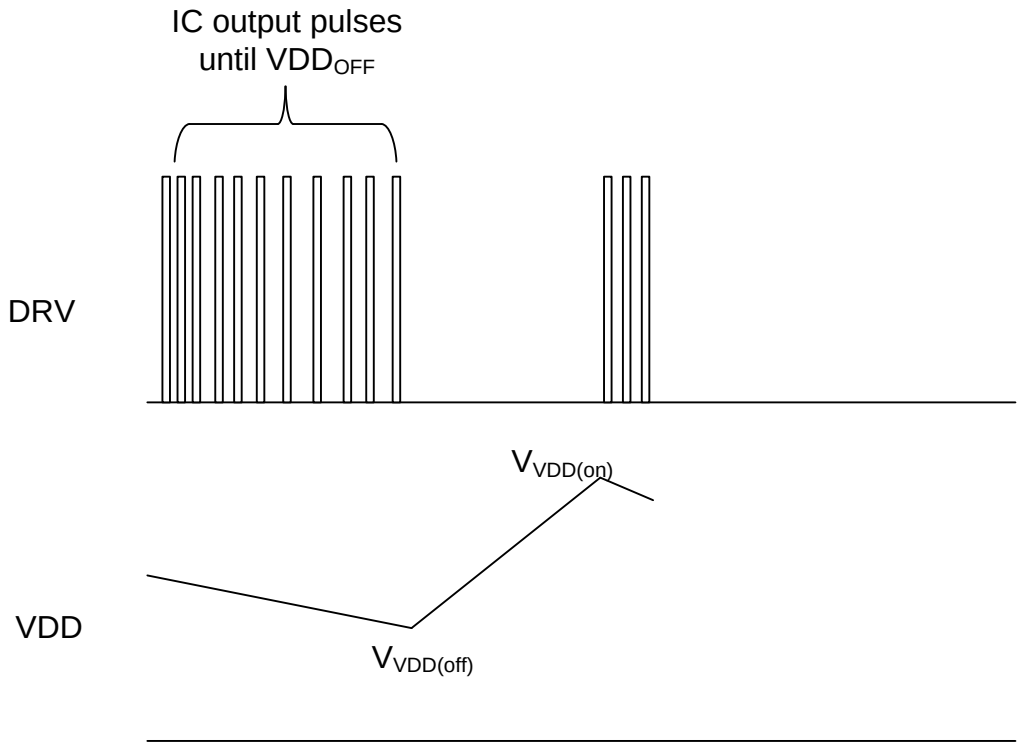

Figure 2. The VDD UVLO protection

Potential Solutions:

- Increase Aux winding turns. It will elevate the VDD level.
- Increase VDD CAP. This will help the VDD sustain time so it will also help in the startup case.
- Decrease Output Cap, Increase constant current point.. Refer the "primary side regulation" of datasheet for the constant current. A simple way to increase constant current point is to decrease R_{CS} resistor.These ways can be used to increase the rising time of Vout to help startup.
- Decrease resistor in series with aux diode (if any). It will elevate the VDD level by collecting more leakage energy of transformer with some load.
- "Full Load, CC Mode, load-on point=0V" is the serious configuration of E-load for startup. Sometimes some changes on the E-load configuration such as setting Half load or CR Mode or setting load-on point at higher value are accepted by the system requirements.

Cause 2: VDD Clamp Current exceeding rating (only for UCC2891X)

Phenomenon: VDD reaches VDD_{CLAMP} (Minimum 26V), and the clamp flowing current exceeds 6 mA [2].

Potential Solutions: Make sure VDD stays lower than VDD_{CLAMP} at all conditions by setting the Na/Ns properly and adjust the resistor in series with VDD diode.

Cause 3: VIN UVLO:

For TI PSR parts, there are AC-line input under-voltage protection functions by detecting current information at VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through RS1 is monitored to determine a sample of the bulk capacitor voltage[4]. To make the converter work properly, the VS dividers should be designed carefully according to the datasheet.

However if you believe your calculation is right, but there is shutdown or startup issue, capturing the last three cycles of V_{BLK}, V_{AUX} and DRV like in Figure 3 is suggested. You can distinguish the root cause by checking below items.

a. Is the voltage of V_{BLK} too low? - Too small bulk cap value would make the ripple on VBLK too much, especially at low-line input and full load. A rough suggestion for Bulk cap selection is about 2uF/W. For 10W design, 22uF cap(22uf is standard value) is suggested.
b. Is the V_{AUX} waveform flat and V_{AUX} approach to V_{BLK}*Na/Np during MOSFET on-time? - If not, there is something wrong; you need to check the transformer turn ratio and the voltage on primary windings during Q1 on-time. A common issue is improper BJT selection.
c. Is the current from VS pin at startup (for the issues where there are only three cycles of pulses) V_{AUX}/RS1 larger than $I_{VSL(run)}$. Make sure the current is larger than $I_{VSL(run)}$, or else go back check the related parameters.
d. Is the current from VS pin at last switching cycle (for the issues where there are many cycles) V_{AUX}/RS1 lower than $I_{VSL(stop)}$. - If yes, it will cause the converter to shut down.

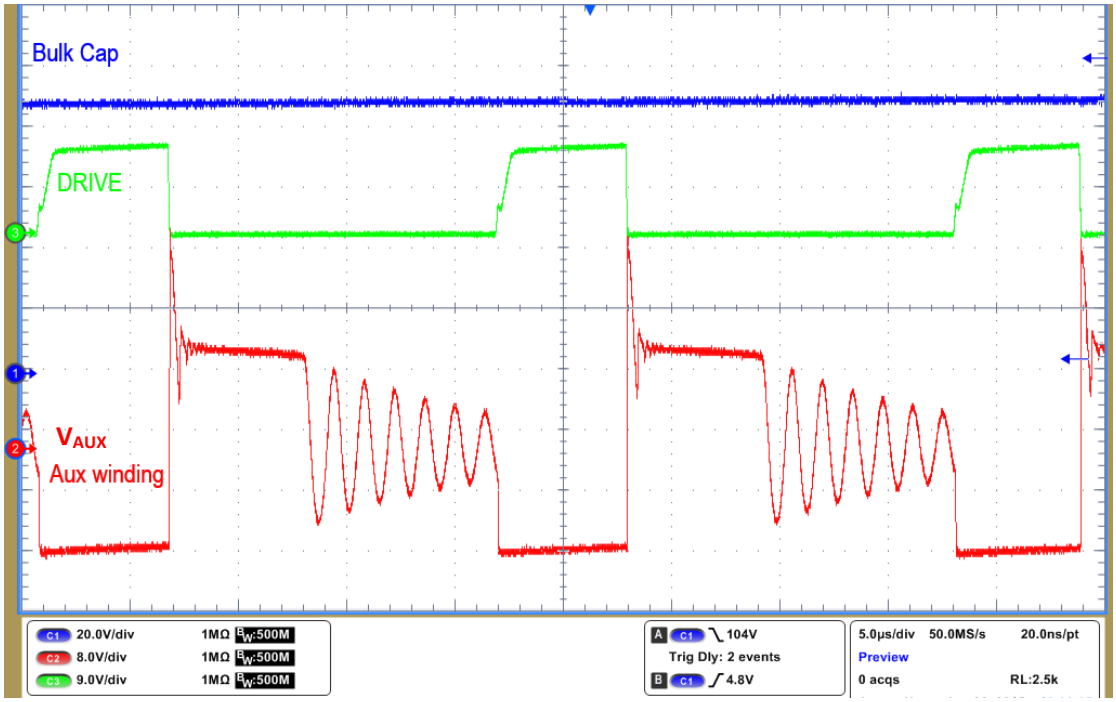

Figure 3. The waveforms needed to distinguish Input UVLO issue

Improper BJT selection

For UCC28722/UCC28720 devices, improper selection for BJT could cause the input UVLO protection. The BJT may not be fully switched on due to the low current gain. You would see that the VAUX during MOSFET on-time isn't flat and doesn't match V_{BLK}*Na/Np near the end of MOSFET on-time. Figure 4 shows a typical UVLO protection caused by improper BJT selection.

An important parameter for a BJT is h_{FE}, DC CURRENT GAIN. It varies with I_B, V_{CE} and Temperature. It could be quite low. For UCC2872X application, base current I_B is decided by controller's driving current I_{DRS} (19mA to 37mA).

So the h_{FE} current gain of BJT should be high enough to make the BJT operate with lower on-state V_{CE}.

Figure 4. UVLO protection caused by improper BJT selection

Cause 4: On-time Detection:

- On-time is too long at first startup cycle

Phenomenon: TI PSR controller and switchers checked the on-time of MOSFET by detecting the voltage on CS pin on the very first cycle after VDD UVLO on. If the voltage on CS pin doesn't reach $I_{PP(min)}$ in desired time, IC will confirm the fault and discharge VDD to $V_{VDD(off)}$ where $I_{PP(min)}=V_{CST(min)}/R_{CS}$. For UCC28704 and UCC28730, this desired time is typical 4us. For UCC28700/1/2/3, UCC28710/1/2/3, UCC28720/2, UCC28740 the desired time for Ton fault is 1/

$F_{SW(max)}$. As for the first cycle, $Ton = \frac{L_{PRI} \cdot I_{PRI}}{Vblk}$, too high inductance or very low input voltage can cause this startup issue. Figure 5 and Figure 6 showed the Ton fault of UCC28704 circuit.

Potential Solutions: To verify the issue, increasing input voltage, decreasing L_{PRI} or increasing R_{CS} can be used. However circuit designer should check the power system design completely to find out why the Ton time is so large.

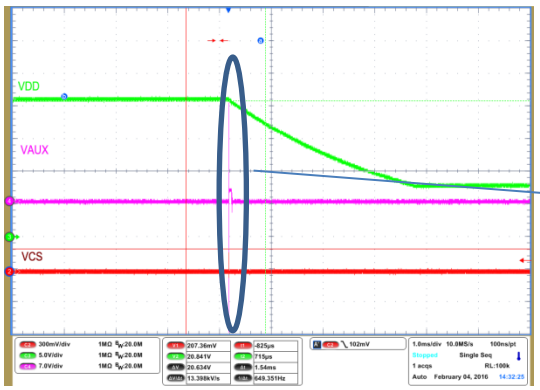

Figure 5. the startup issue caused by Long Ton at UCC28704EVM

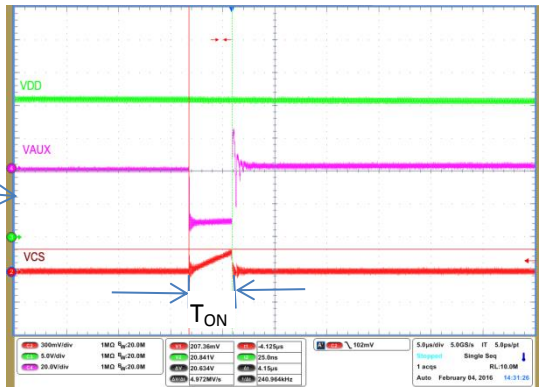

Figure 6.the startup issue caused by Long Ton at UCC28704EVM(in zoom) ; Ton larger than 4us

- Too long on time cause shutdown

Phenomenon: This only suited for UCC2891X. The IC will stop DRV output and start VDD UVLO cycle when it detect three consecutive on time larger than $t_{ONMAX(max)}$ at high load and $t_{ONMAX(min)}$ at light load.

Potential Solutions: To verify the issue, decreasing Lp or increasing R_{IPK} can be done. However, the circuit designer should check the power system design completely to find out why the Ton time is so large.

Cause 5: CS short circuit (1.5V) protection

The converter will stop switching cycle and start a VDD reset cycle when IC detect voltage on CS pin higher than 1.5V for three consecutive cycles.

CS Noise caused by layout

Phenomenon: The typical noise caused by the suddenly raised dv/dt of Vds is like Figure 7. The voltage peak on CS pin after MOSFET turn off exceeded the over current threshold V_{OCP}, for UCC28710 its typical value is 1.5V. The noise can be serious if there is bad layout and too high R_{LC}.

Potential Solutions: Improve the layout of CS circuit and MOSFET to decrease the noise is suggested.

The situation would be better with smaller R_{LC}. However change R_{LC} resistor will also impact the constant current regulation. Make sure R_{LC} is close to the controller package.

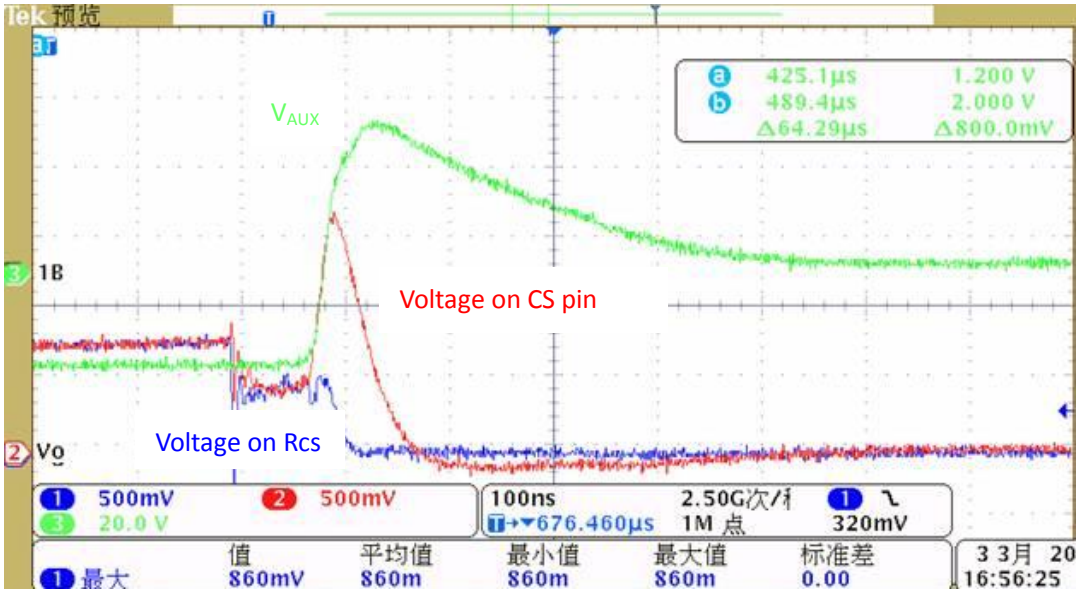

Figure 7. OCP caused by the noise

Transformer saturation

Phenomenon: The typical saturation for transformer is like Figure 8. The current through R_{CS} increases rapidly when the transformer became saturated.

Potential Solutions: Check the transformer design to make sure no saturation happens. The equation to check B_{MAX} is that $B_{MAX}=\frac{L_{PRI}\cdot I_{PK}}{N_P\cdot Ae}$ where $I_{PK}=\frac{V_{CST(max)}}{R_{CS}}$ for UCC2870X,UCC2871X and UCC2872X; $I_{PK}=\frac{V_{CCR}}{R_{IPK}}$ for UCC2891X; Np is the primary winding turns of transformer; L_{PRI} is the primary inductance; Ae is the cross-sectional area of the core. Bmax should always be lower than BSAT which is the core saturation flux density and decided by the core material. B_{SAT}'s curve or value can be found in the ferrite core book like in Figure 9 . The temperature characteristic of B_{SAT} should be considered.

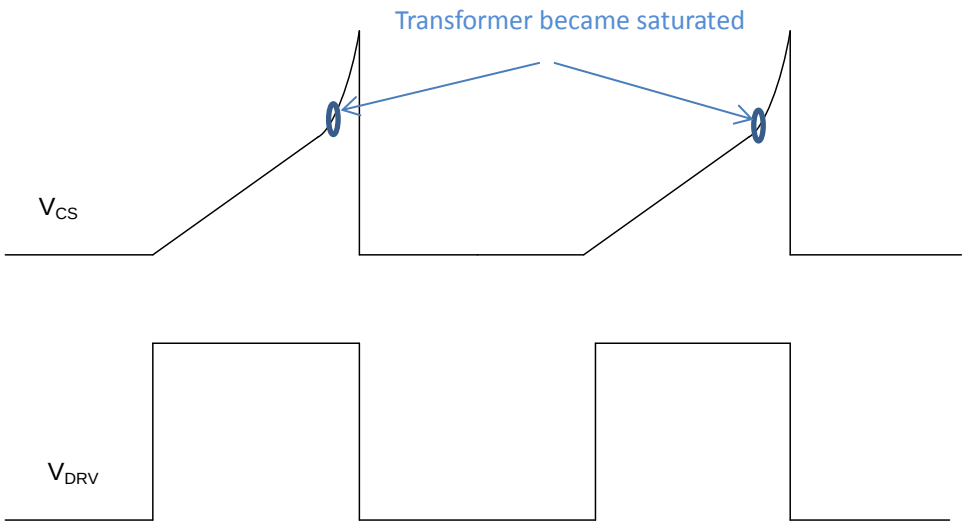

Figure 8. OCP protection caused by transformer saturation

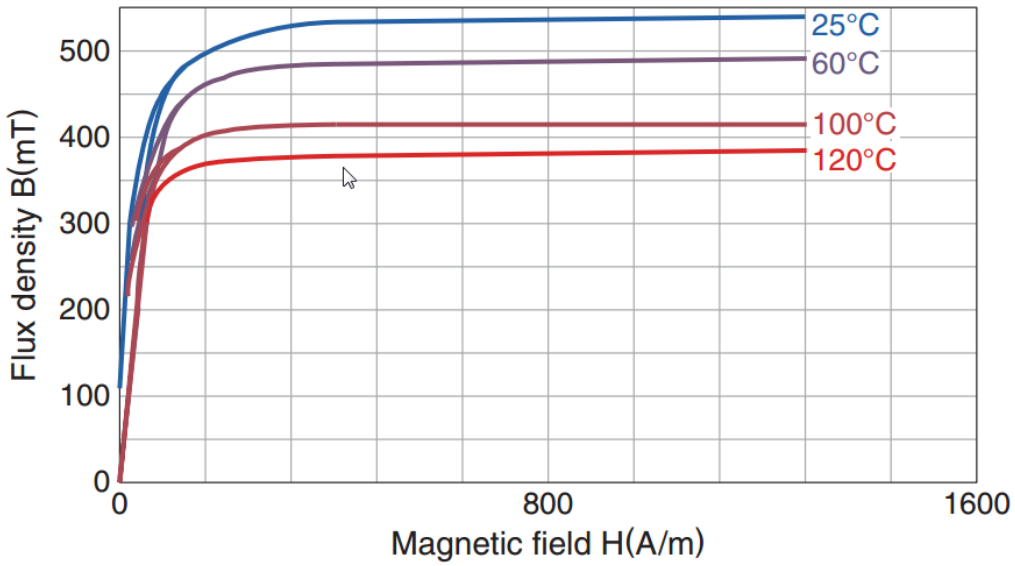

Figure 9. The B-H temperature characteristics of TDK's PC95

Cause 6: AUX winding detection (OVP)

The output over-voltage function is determined by the voltage feedback on the VS pin. The device stops switching and starts to discharge the VDD capacitor to $V_{VDD(off)}$ threshold when it detects over-voltage.

Output voltage trigger OVP at zero load

Phenomenon: When probing on the output voltage, you see output voltage exceed the regulation level and the voltage reflected to VS pin exceeds the over-voltage threshold V_{OVP}.

Potential Solutions: Decrease the capacitance of Drain node which mainly includes the Coss of MOSFET and input capacitance of transformer; To Decrease the preload resistor value; To Check if

the turn-off of MOSFET is too slow which maybe caused be too large of a series resistor in the gate.

The shape on VS pin affect the detection

The PSR controller doesn't sense the output directly like traditional opto feedback. It is more sensitive by its working scheme of detecting Auxiliary winding voltage. The shape of voltage on VS pin is very important to avoid misdetection and OVP. Because probing on VS pin could affect the detection also, we can estimate the waveform of VS pin by probing on Auxiliary winding.
Please refer the datasheet for the shapes needed.
However, snubber adjusting especially on the damping resistor can affect the waveforms.
Too high of leakage inductance of the transformer would make the detection less accurate.
Layout of VS relative circuit should be also careful. The trace between VS dividers and VS pin should be as short as possible to reduce possible EMI coupling [4].