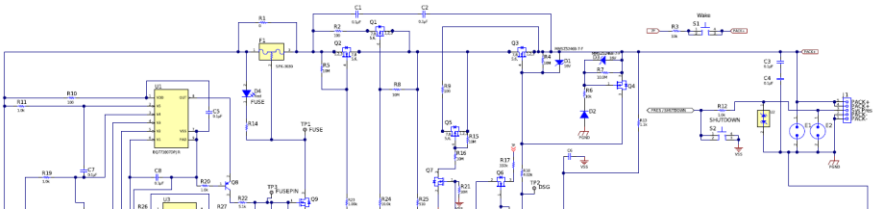
Following is a brief on our internal analysis on the issue mentioned to you

Few items which are under suspicion based on our analysis are as below:

1. The BQ40Z80 eval kits have an errata mentioned as below

5.2 bq40z80 RevBSchematic

NOTE: The bq40z80EVM-020 has an incorrect implementation for the reverse polarity circuit. For proper charge and discharge behavior, D3 and R7 should be removed. This will be corrected on a future version of the EVM.

2. 

I do not know if this could impact the issue we are seeing but this is something which is not done in the eval kits we have inhouse. Although D3 and R7 are removed on the BMS designs which we built so shouldn't be an issue while testing the eval kit with our BMS boards.

3. SMBus

The SMBus interface of the BQ40Z80 IC is very weirdly defined in datasheet. Below image defined the pins to have a max rating of 32V.

V_{IN}	Input voltage range	SMBC, SMBD, $\overline{DISP}$/GPIO, PDSG/GPIO, $\overline{PRES}$/ $\overline{SHUTDN}$/, $\overline{DISP}$/PDSG/GPIO[1]			32	V
		TS1, TS2, TS3/ADCIN1/GPIO, $\overline{DISP}$/TS4/ADCIN2/GPIO			V_{REG}	
		LEDCNTLA/PDSG/GPIO, LEDCNTLB/GPIO, LEDCNTLC/ GPIO[1]			V_{BAT}	

Below describes the pins to be Digital IO and not open drain.

			GPIO: Customizable GPIO
SMBD	18	I/OD	SMBus data pin
SMBC	19	I/OD	SMBus clock pin

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

The below description looks like the SMBus pins are referenced to Vreg (internal LDO) at 1.8V(while above reference mentioned a max of 32V allowance. Also, no mention of VOH inspite of it being defined as a digital IO.

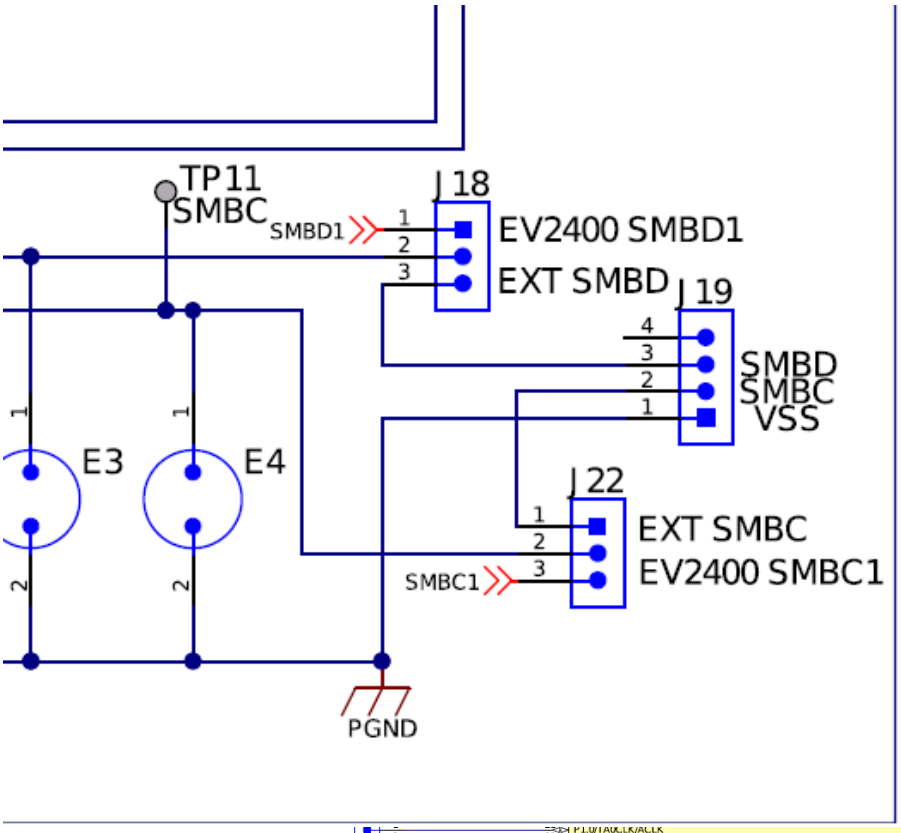
SMBD, SMBC High Voltage I/O				
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8 V	1.3	V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8 V	0.8	V

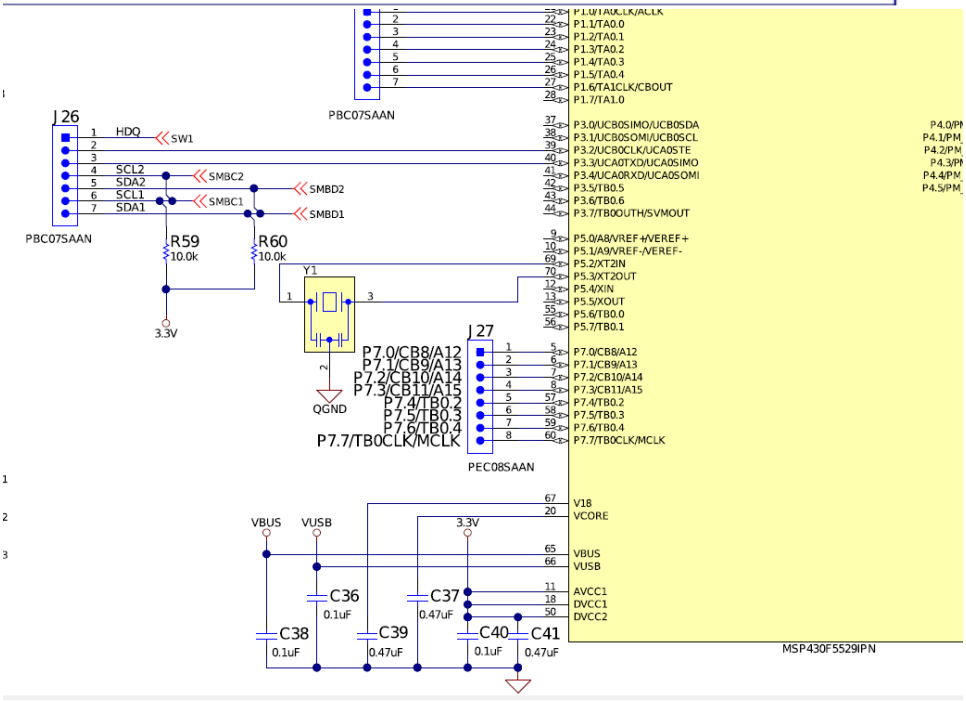
Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8 V, I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF

It's unclear whether this SMBus interface can even be directly interfaced with a 3.3V level I2C chipset or no. However, on looking at eval kit below, the SMbus of the BMS chip does interface directly with the 3.3V TI controller whilst having 3.3V pull ups on both the pins.

This is exactly how we were using the eval kits setup at our end by shorting pins 1 and 2 of J18 and J22. They did not burn yet in this setup though.





It's a discrepancy right now to understand if this could be any issue since the board burnout isn't consistent.

4. We checked if there is any sort of ESD burnout. However, the chip has sufficient ESD protections in built as well as externally added. This application definitely has a high amount of connect disconnect which might involve ESD as well. So we want you to analyse if this could be a potential issue as well.

9.2.2.3.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits; however, adding a ESD protection device, TPD1E10B06D (U5 and U6) and series resistor (R50 and R51), provides more robust ESD performance.

The SMBus clock and data lines have an internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

5.