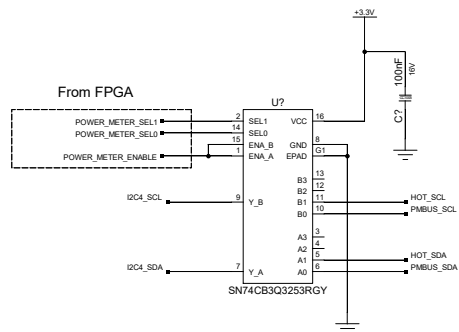
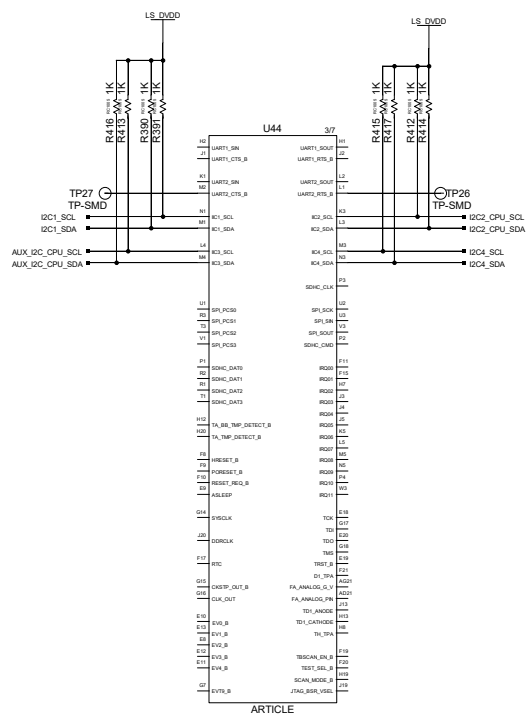
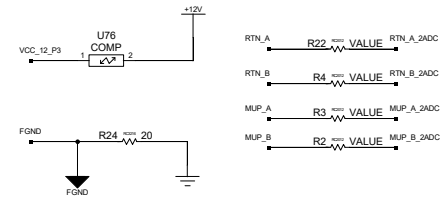




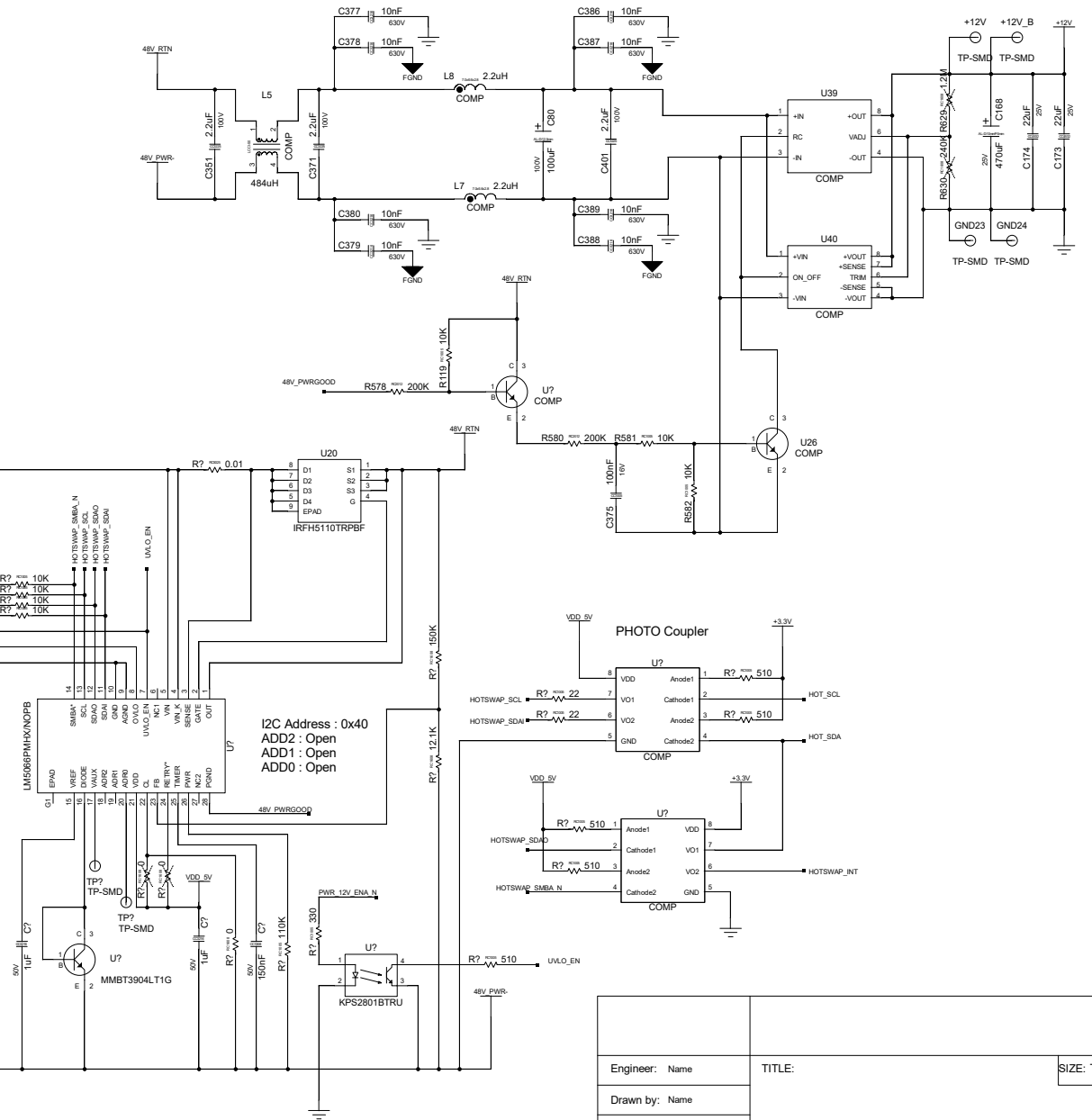
Engineer: Name		TITLE:	
Drawn by: Name			
R&D CHK: Team name			
QA CHK: Yes / No	REV:	Drawing Number:	5 / 21

NO	SIGNAL NAME	NO	SIGNAL NAME	NO	SIGNAL NAME	NO	SIGNAL NAME	NO	SIGNAL NAME
A1	VCC_12_P3	B1	FGND	C1	RTN_A	D1	RTN_B	E1	MUP_A
A2	VCC_12_P3	B2	FGND	C2	RTN_A	D2	RTN_B	E2	MUP_B
A3	VCC_12_P3	B3	FGND	C3	RTN_A	D3	RTN_B	E3	MUP_A
A4	VCC_12_P3	B4	FGND	C4	RTN_A	D4	RTN_B	E4	MUP_B

COMP



48V CARD INPUT POWER



Engineer: Name	TITLE:	SIZE: T
Drawn by: Name		
R&D CHK: Team name		
QA CHK: Yes / No	REV:	Drawing Number:

Changed by:	Date Changed:	Time:	M/DD	QA CHK: Yes / No	REV:	Drawing Number:	8 / 21
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