Application Report
SNVA638A–April 2012–Revised April 2013

AN-2155 Layout Tips for EMI Reduction in DC / DC Converters

ABSTRACT

This application note will explore how the layout of your DC/DC power supply can significantly affect the amount of EMI that it produces. It will discuss several variations of a layout, analyze the results, and provide answers to some common EMI questions such whether or not to use a shielded inductor.

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1 Overview

Electromagnetic interference (EMI) is the disruption of proper operation of an electronic device, caused by an electromagnetic field generated by a different device. To prevent electronics from interfering with the operation of other devices, EMI is regulated by the government where the electronic device is being sold. There are several norms, for example, in the European norms (EN55022, etc.), in the USA there is FCC part 15, in Canada there is ICES-003, in Japan there is VCCI, and so on. EMI is difficult to accurately predict, so the best thing you can do is to minimize the known causes of EMI when planning your layout and design.

2 Theory

2.1 How to Make Loop Antennas

The study of EMI is really the study of antennas. So the things that make a good antenna, will also increase EMI. Let's examine an electrically small loop antenna. An electrically small loop antenna is one where the conductor length is small compared to the wavelength of the radiating signal. As radiated EMI standards are generally only concerned with frequencies up to 1 GHZ (which has a wavelength of 0.3 meters) and a typical DC/DC converter is usually less than .075m in any given dimension, the electrically small loop antenna is a good starting point.

$$E = 263 \text{ e-}16 \times (f^2 \times A \times I) / r \text{ Volts per meter} \quad (1)$$

The equation above is for the E field of differential mode EMI. We see that the radiated field is proportional to the frequency (f) squared, the loop area (A), the current (I) and the measured distance from the radiating source to the receiving antenna (r) [(1)] . Frequency is in Hz, A is in m^2, I is in Amps and r is in meters. From this we can see what makes a good loop antenna.

2.2 Good loop antennas

1. Radiate significantly more power for higher frequencies than for lower.
2. Radiate more power when their area is increased
3. Radiate more power when the signal current is higher

These three items play key roles in making good antennas. So to reduce EMI we need to locate all the loops in our design with high frequency currents. Then we need to decide whether we can lower the frequency, reduce the loop area, lower the current of the signal, or some combination of all of these.

2.3 Locating High di/dt Currents

For this example, we will look at the layout of a Buck (step down) regulator. A Buck converter chops the input voltage (VIN) into a pulse waveform at a specific duty cycle (D) such that the average voltage at the output of an LC filter (Vo) is D * VIN. It is important that we understand the current paths formed by the switching action of the regulator.

In **Loop 1**, shown in Figure 1, current flow originates at the input bypass capacitor, Cin1 and then continues through the high side MOSFET during its on-time, followed by the inductor and the output bypass capacitor Co1, finally returning to the input bypass capacitor.

(1) Henry W. Ott, "Noise Reduction Techniques In Electronics Systems", New York: Wiley- Interscience, 1988

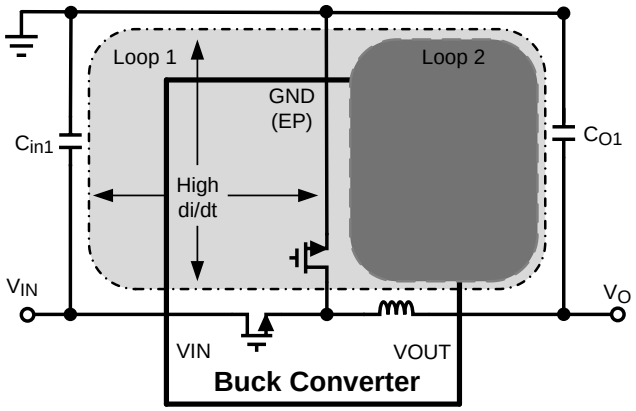

Figure 1. Current Loops

Loop 2 is formed during the off-time of the high side MOSFET and the on-time of the low side MOSFET. The energy stored in the inductor flows through the output bypass capacitor and the low side MOSFET returning through GND and back to Co1 as shown. **The area where these two loops don't overlap, and including the boundary between the loops, is a high di/dt current area**. Large high frequency AC currents flow on these traces. These high frequency currents are the source of most of the far field EMI, while the high frequency voltage changes are contributing to near field EMI.

The length of the high di/dt traces should be kept as short as possible to minimize the loop antenna area. Two of the high di/dt traces are connected to the input bypass capacitor. The input bypass capacitor Cin1 plays a critical role in supplying high frequency currents to the converter and returning them to their source. High frequency noise that the input capacitor is unable to bypass will be conducted onto the input leads of the supply. This is known as conducted EMI. However, this high frequency conducted noise will see long input leads as antennas and radiate.

The other high di/dt area is the switch node, the common connection between the inductor, low-side and high-side MOSFET. The switch node creates EMI in two ways. First, the large voltage swings on the switch node will capacitively couple to other traces. Second the trace itself can radiate due to the high switching currents.

The output bypass capacitor Co1 does not supply large ac current but does act as a high frequency filter for switching noise. The inductor will have some stray capacitance that couples high frequency switching noise to the output. The output filter capacitor bank needs low impedance at these frequencies which can be up to 100 times higher than the switching frequency. For these reasons the input and output capacitors should be placed as close as possible to the VIN, GND and VOUT nodes. Make the traces between the bypass capacitors and their respective components as short and wide as possible; thereby minimizing the inductance of these connections. A capacitor with smaller parasitic inductance will exhibit low impedance to high frequencies, and consequently reduce conducted emissions. Ceramic (X7R or X5R) or other low ESR type capacitors are recommended. If the regulator requires output capacitors with a defined ESR then small ceramics can be placed in parallel with this bulk capacitor to handle the high frequency bypassing.

2.4 How to Make Worse Antennas

The goal of our DC/DC converter design is to make bad antennas out of the loops that carry the high di/dt currents.

Just to re-iterate, for differential mode EMI the radiated field is proportional to the frequency (f) squared, the loop area (A), the current (I) and the measured distance from the EMI source to measurement antenna (r) [2]. The distance, r, is 3 meters in our test chamber, which sets the CISPR 22 limit for frequencies below 300MHz at 40dBµV/m. The radiated limits are adjusted for different test chamber sizes. For example, in a 10 meter chamber the measured signal is reduced by 20 x log(10m / 3m) ≅ 10db. Thus the limit for a 10 meter chamber is 10db below the limit for the 3 meter chamber.

$$E = 263 \text{ e-16} \times (f^2 \times A \times I) / r \text{ Volts per meter} \quad (2)$$

Let's look at an example. We have a layout with an input bypass loop area of 12 mm^2. Since high frequencies radiate more easily we will use the highest frequency of the high di/dt currents as f in our equation. If we look at the high di/dt currents that are bypassed by the input capacitor, these switching currents have a very fast rise time. We will simplify the calculation with the assumption that the highest frequency component with significant energy (the Band Width) is equal to 0.35 divided by the rise time of the switch node [3] in Figure 1.

$$f = \text{Band Width} = 0.35 / \text{Rise Time} \quad (3)$$

If the measured rise time of the switch node is 10ns, then the band width is 35MHz. The current, I, associated with this frequency can be approximated by the rms input current. Which is the DC output current multiplied by the square root of the duty cycle.

$$I = \text{Output current} \times (D)^{1/2} \quad (4)$$

$$I = \text{Output current} \times (\text{Output Voltage} / \text{Input Voltage})^{1/2} \quad (5)$$

For this example: the input voltage is 12 volts, the output voltage is 3.3 volts and the output current is 2 amps. Thus, I = 1.05A. Therefore:

$$E = 263 \text{ e-16} \times ((35\text{e}6\text{Hz})^2 \times 12\text{e-}6\text{m}^2 \times 1.05\text{A}) / 3\text{m}$$

$$E = 135\text{e-}6 \text{ Volts / meter} \quad (6)$$

Are we really worrying about 135 micro volts per meter? Yes we are. The limit line for Cispr 22 Class B, at 3 meters, is around 40 dBµV/m or 100 µV/m. Converting our answers into dbµV/m yields.

$$E = 20 \times \log(135\text{e-}6 / 1\text{e-}6)$$

$$E = 42.6 \text{ dBµV/m} \quad (7)$$

So 135 µV/m puts us just over the limit line.

Our goal is to reduce this field so that we fall under the limit. We have no control over r; the distance to the measuring antenna is determined by the regulations. What choices are left to us?

The switching frequency (f) will probably be dictated by requirements for transient response, efficiency, ripple, and component cost so let's assume this is fixed. One thing that we can do is slow down the rise time of the high-side fet to remove the higher frequency components and improve EMI. The downside of this approach is an increase in switching losses because of the increased time the FET spends in the linear region. A snubber can also be used to slow the rise time of this signal and has a similar tradeoff of improved EMI for increased power loss. In many cases this additional power loss is not acceptable, but in a pinch, adding a few ohms to the gate drive of the high side FET in parallel with a diode can slow down the turn on of the FET while keeping the turn off properties unchanged. This can also be accomplished by adding the resistor between the top of the bootstrap capacitor that powers the high-side driver.Figure 2

[2] Henry W. Ott, "Noise Reduction Techniques In Electronics Systems", New York: Wiley- Interscience, 1988
[3] Eric Bogatin, "Signal Integrity Simplified",New Jersey: Prentice-Hall, 2004

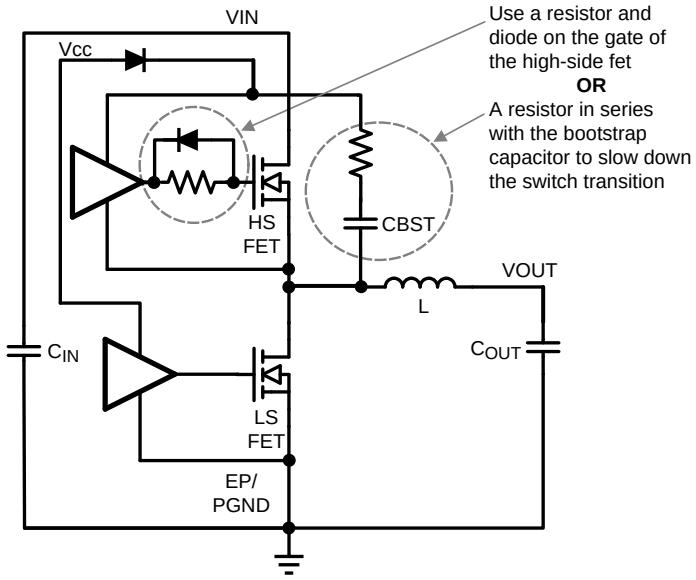

Figure 2. Methods for Slowing Down the Transition Rise-Time

Although we have no control over the DC input current, we can control the level of switching current that reaches the input leads. As stated above (for a buck converter) the input bypass capacitor, Cin, is bypassing a high di/dt current. We have some control over how much of this current (I) escapes the converter, through bypass capacitor selection and filtering. If we add an LC filter before the input capacitor we can greatly diminish the currents on the board before they make it to longer leads or traces that can radiate. This is very useful for the input side of a buck or the output side of a boost. Note that just adding more input capacitors can help reduce the high frequency current that reaches long input leads. This bank of capacitors should be designed such that the impedance is low up to very high frequencies. See *Input and Output Capacitor Selection Application Report* SLTA055 for an example of a low impedance capacitor network. For guidelines on input filter design see *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* (SNVA489).

Finally, we have the most control over the layout and this will determine the loop area (A). When trying to reduce the loop area to design for low EMI, one of the most important things we can do is to add a ground plane. A ground plane will reduce the area of the current loops shown in Figure 1 by providing a return path that is a mirror image of the current path. You might ask, how does this reduce the loop area? The components are still in the same place. Doesn't component placement define the loop area?

Think of it this way. Without the ground plane the loop area is exactly defined by the placement of the components. The current must flow around the loop. If the loop is defined by a 3mm by 4mm box then the area will be 12 mm^2.

When a ground plane is added, the high frequency currents on the top layer will induce an opposing current on the ground plane to cancel the magnetic field. This is often called an image current making the ground plane the image plane. This return current on the ground plane reduces the area of the loop. Think of it by laying out the loop with a piece of rope. A second rope is placed on top of the first, with the ends tied together. The loop area is now defined by twice the length of the rope multiplied by the distance between the ropes. The loop now has two layers and the area is now 28mm (twice the perimeter of the initial loop) multiplied by the distance between the two layers (0.25mm for a typical PCB stack up). The loop area is reduced to 7mm^2 and a reduction in radiated energy can be achieved.

Recalculating the radiated emissions from above with the ground plane yields E= 37.94 dBµV/m a calculated improvement of 4.65 dBµV/m, and under the limit 40 dBµV/m.

In summary, the primary sources of radiated noise come from the high di/dt traces. Make these traces short and wide enough to handle the current and bypass them effectively with a capacitor bank designed for low impedance over a wide frequency range. Use a ground plane to decrease the area of the current loops. If this is not enough add an LC filter to stop the high frequency currents from reaching long input/output wires which can radiate.

3 Setting up the Experiment

With some theory in place, we can look at the effects of different layouts to test the following theories. Does a ground plane reduce EMI? Does bypass capacitor placement effect EMI? Do breaks in a ground plane effect EMI? Does rounding the edges of our traces lower EMI? ... For this experiment we took the *LM3102 SIMPLE SWITCHER® Synchronous 1MHz 2.5A Step-Down Voltage Regulator* (SNVS515) and created eight different layouts. All versions of the board are slight variations of the control board, board number one. The summary below describes how the layouts differ from the control board.

3.1 Layouts

1. Layout 1 is the control board, a typical layout for this particular part on a 2-layer board.
2. Two additional ground planes were added to #1 to create a four-layer board.
3. The ground copper beneath the switch node has been removed from #1.
4. The ground copper beneath the switch node has been removed from #2.
5. The length of the switch node has been doubled from #1.
6. The length of the switch node has been doubled from #2.
7. All traces were rounded to remove sharp corners from #1.
8. The switch node was routed from the top layer to the bottom layer to connect to L1 on #2.

Board number 2 was also used to test the following: a) the effect of input capacitor placement b) the effect of shielded versus non-shielded inductors, and c) the benefits of an input filter composed of L2 and Cin7.

A summary of results is shown in the following table.

4 Result of Experiments

Experiment	Result	Conclusion	Level of Importance in Low noise / Low EMI layout
Does adding a ground plane reduce EMI?	Board 2 increased its margin for passing Cispr-22 by 4dBµV/m over Board 1.	Adding a ground plane reduces EMI.	HIGH
Does cutting the ground plane beneath the high current path increase EMI?	Board 2 increased its margin for passing Cispr-22 by 6dBµV/m over Board 4.	Cutting the ground plane under the high current path increases EMI.	HIGH
Does bypass capacitor placement affect EMI?	Switching spike noise decreased by 3.6V. Output ripple noise decreased by 28mV. Margin for passing Cispr-22 increased by several dBµV/m.	Small well bypassed loops decrease EMI and noise in a DC/DC converter design.	HIGH
Does adding an input filter reduce EMI?	Adding an input filter to a buck converter, powered by short wires to a battery, reduced the radiated EMI by up to 20db	Input filters can be used to improve radiated as well as conducted emmissions	HIGH
Does using a shielded inductor reduce EMI?	Near field and Far field EMI is improved by using a shielded inductor	Shielded inductors have improved EMI performance over non-shielded incuctors.	HIGH
Does routing the switch node on multiple layers increase EMI	Board 8 had a slight decrease in its margin versus board 2.	It appears that it is not the routing of the switch to multiple layers that greatly increases EMI but the fact that doing so can interrupt the return path	MEDIUM
Does the length of the switch node affect far field EMI?	Board 6 decreased its margin for passing Cispr-22 by less than 1dBµV/m over Board 2.	Doubling the length of the switch node on a board with a ground plane had little effect on the farfield EMI. The longer switch node did increase near field.	MEDIUM
Does rounding the edges of the traces reduce EMI?	Board 7 increased its margin for passing Cispr-22 by less than 1dBµV/m over Board 2.	Rounding the edges of the traces had little effect on passing EMI,	LOW

5 Conclusions

EMI is difficult to accurately predict, so the best thing you can do is to minimize the known causes of EMI when planning your layout and design. This application note explored the effects of board design, filters, Mosfet slew rates, inductor shielding, and bypass capacitor placement on the EMI performance of your design. In the end it all boils down to making bad antennas.

6 Results

6.1 EMI Results for Board Layout, tested at 12Vin, 3.3Vout and Iout = 2Amps.

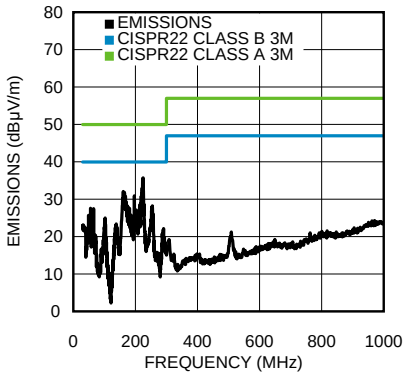

Figure 3. Board 1 (Control 2 Layer)

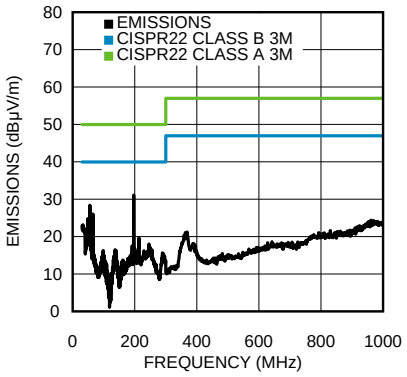

Figure 4. Board 2 (+GND PLANE 4 Layer)

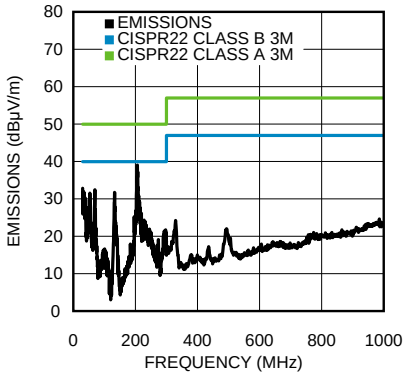

Figure 5. Board 3 (- SW NODE COPPER 2 Layer)

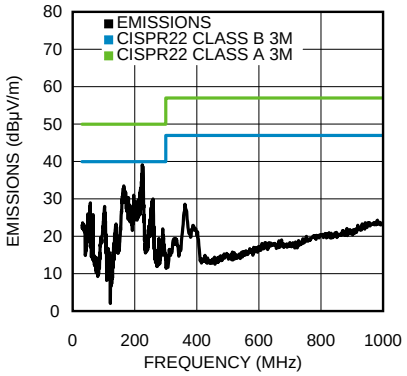

Figure 6. Board 4 (- SW NODE COPPER 4 Layer)

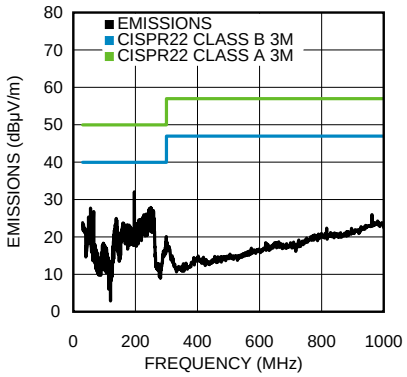

Figure 7. Board 5 (Extend Switch node 2 Layer)

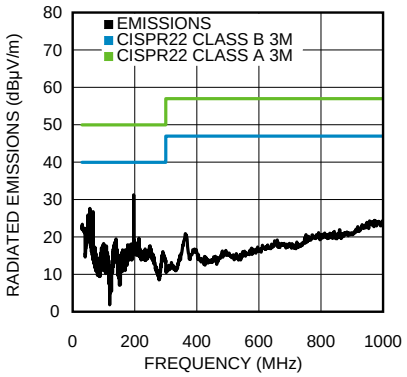

Figure 8. Board 6 (Extend Switch node 4 Layer)

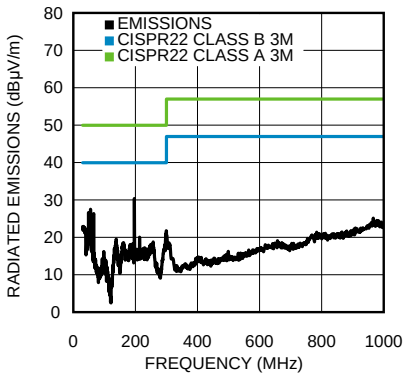

Figure 9. Board 7
(Round Traces 2 Layer)

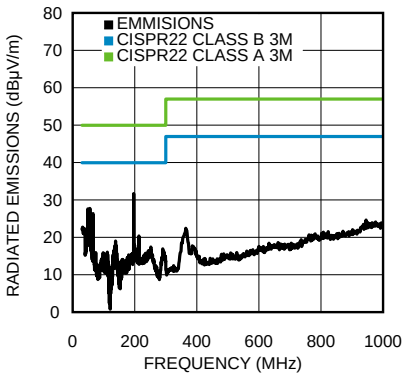

Figure 10. Board 8
(Switch node routed from top to bottom layer, 4 Layer)

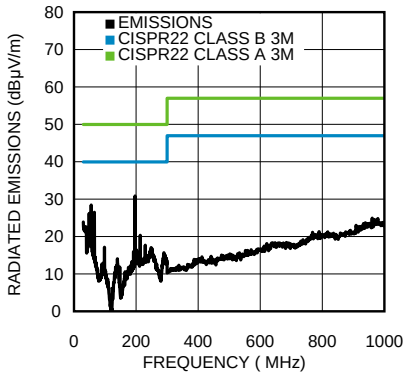

Figure 11. Noise Floor

6.2 EMI Comparisons for Board Layout

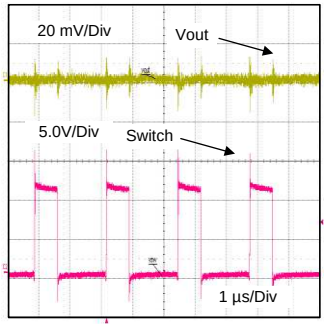

Figure 12. Switching waveform for control (Board1)

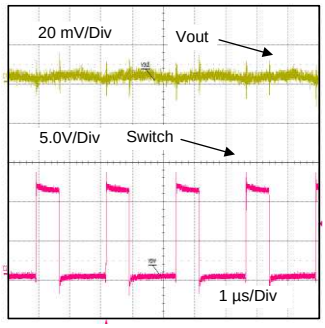

Figure 13. Switching waveform with extra ground plane (Board2)

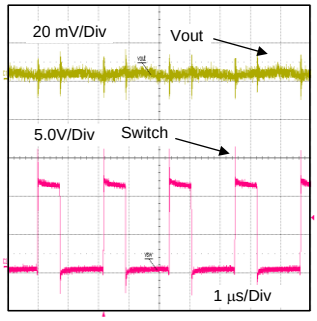

Figure 14. Switching waveform with ground plane beneath switch node cut (Board4)

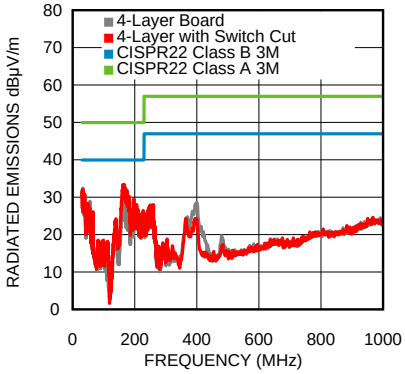

Figure 15. BOARD 2 vs BOARD 4 (Solid ground plane vs. ground plane beneath switch node cut)

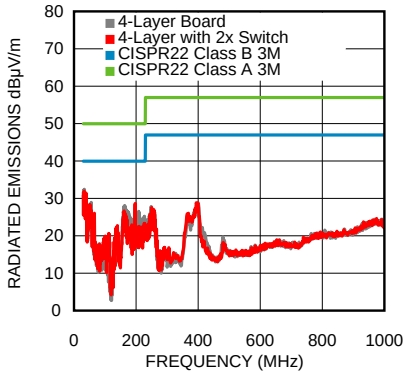

Figure 16. BOARD 2 vs BOARD 6 (Original switch node length vs extended switch node length)

6.3 EMI Results for Capacitor Placement

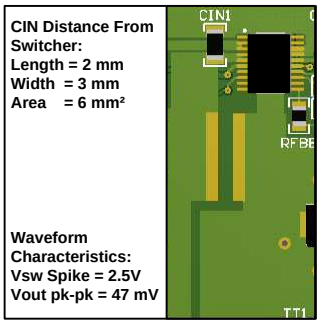

Figure 17. Placement 1

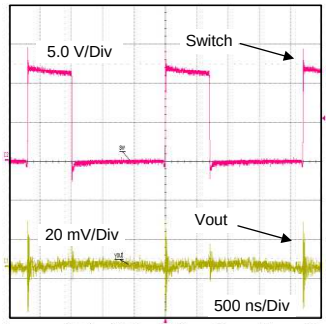

Figure 18. Switching Waveform for Placement 1

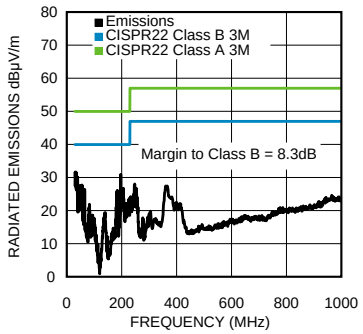

Figure 19. EMI for Placement 1

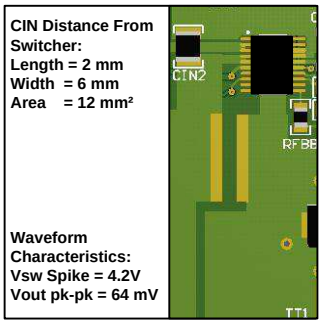

Figure 20. Placement 2

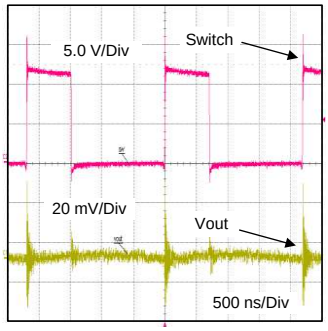

Figure 21. Switching Waveform for Placement 2

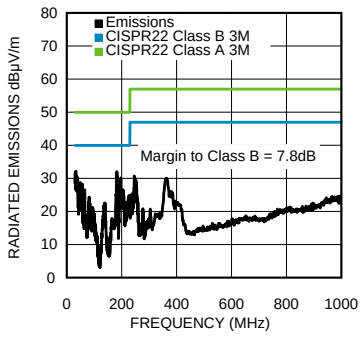

Figure 22. EMI for Placement 2

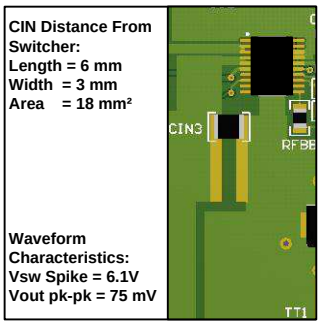

Figure 23. Placement 3

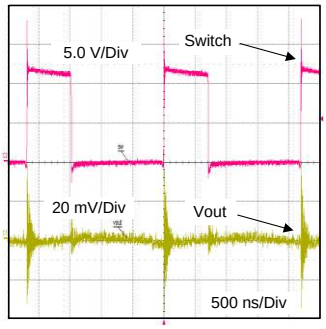

Figure 24. Switching Waveform for Placement 3

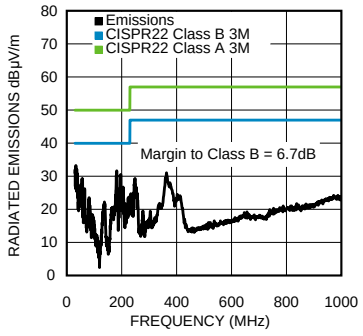

Figure 25. EMI for Placement 3

6.4 Board 2 Gerbers and Schematic

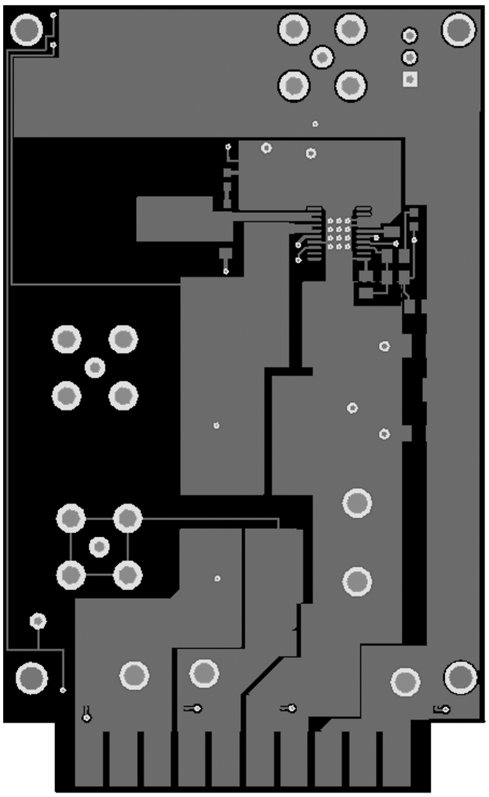

Figure 26. Top Layer

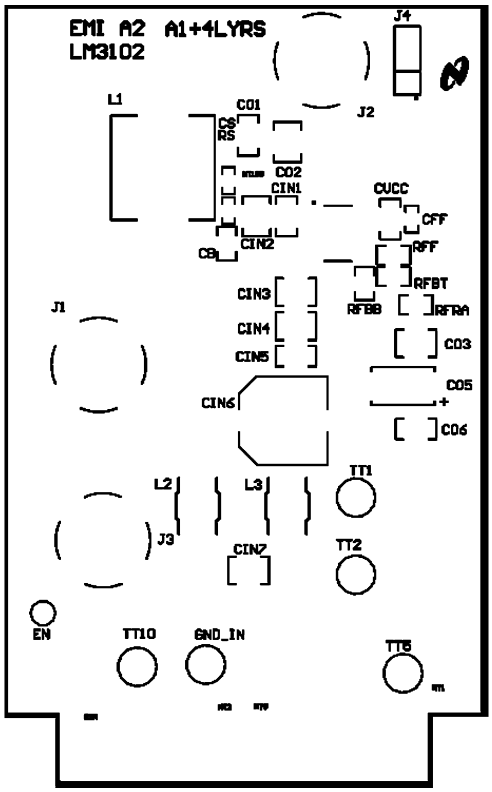

Figure 27. Top Overlay

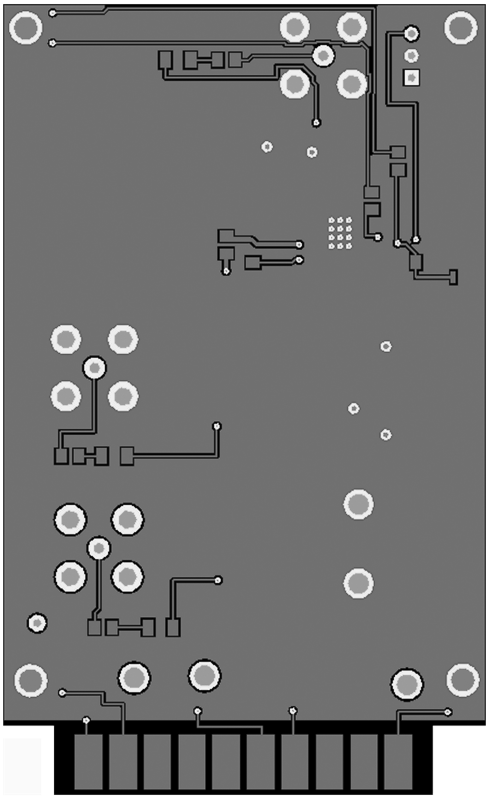

Figure 28. Bottom Layer

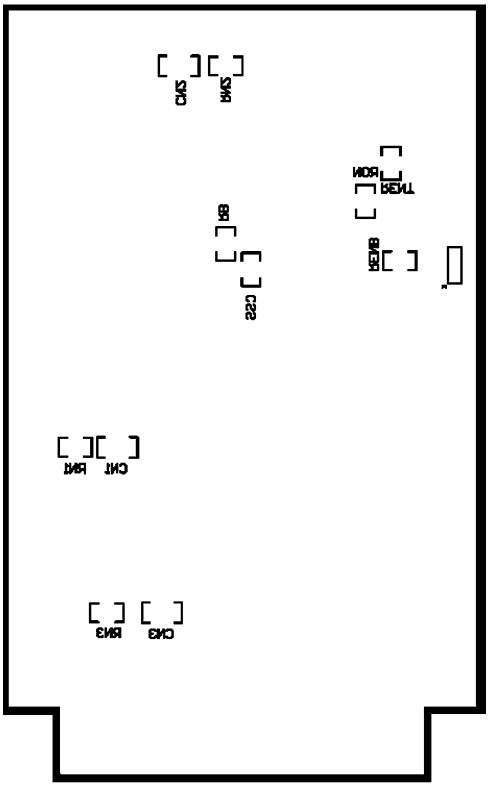

Figure 29. Bottom Overlay

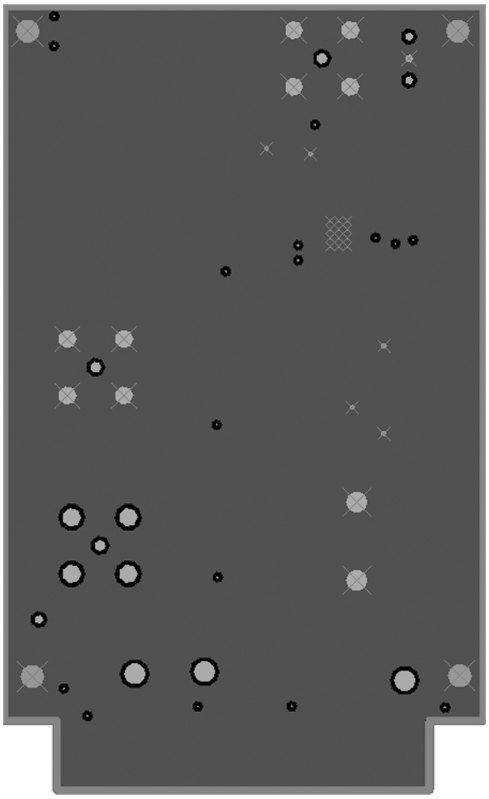

Figure 30. Ground Plane

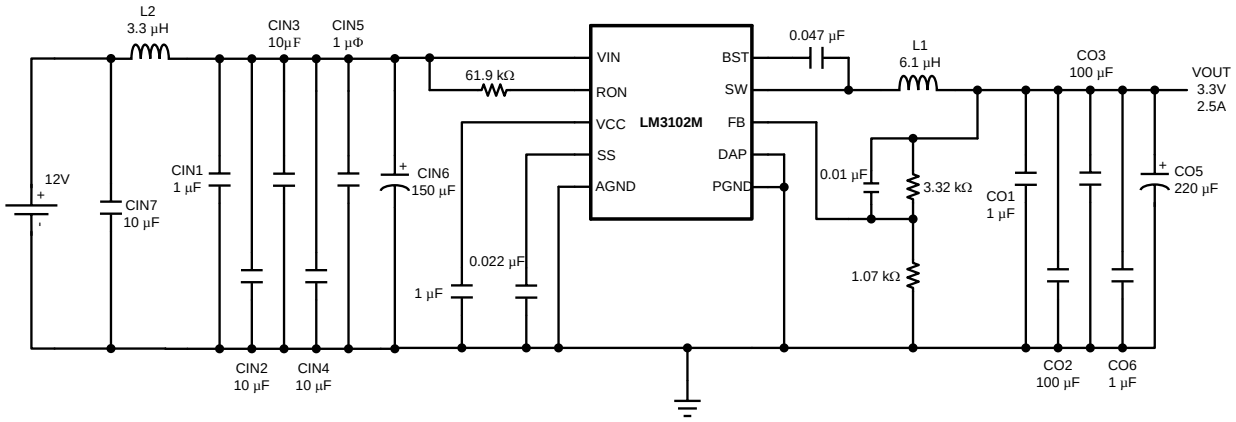

Figure 31. EMI Test Board Schematic
*** Cin1 - Cin4 are placement options**

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