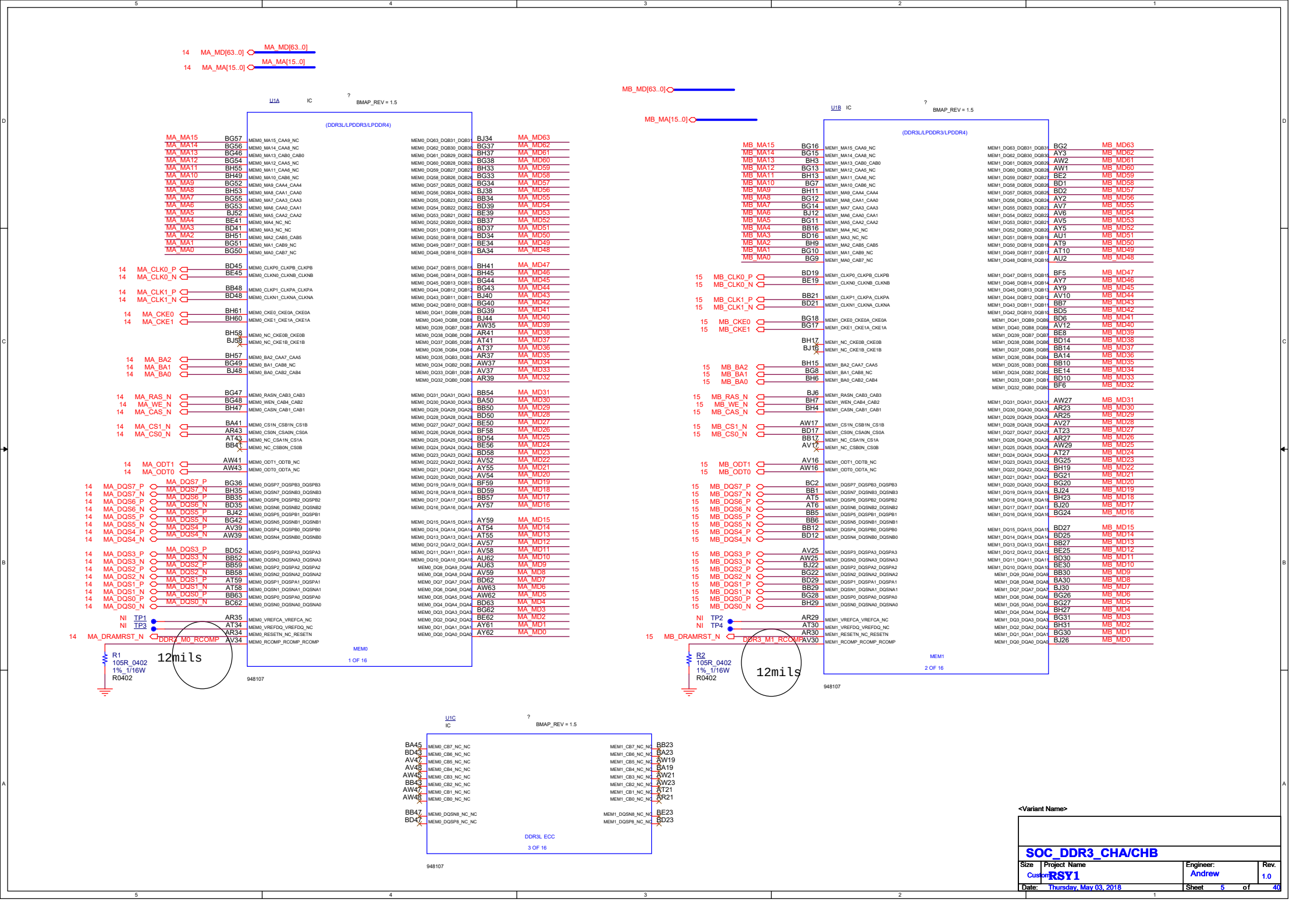
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MA_MD[63..0]
14 MA_MA[15..0]
MA_MA[15..0]
U1A
IC
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(DDR3L/LPDDR3/LPDDR4)
MA_MA15 BG57
MA_MA14 BG56
MA_MA13 BG46
MA_MA12 BG54
MA_MA11 BH55
MA_MA10 BH49
MA_MA9 BG52
MA_MA8 BH53
MA_MA7 BG55
MA_MA6 BG53
MA_MA5 BJ52
MA_MA4 BE41
MA_MA3 BD41
MA_MA2 BH51
MA_MA1 BG51
MA_MA0 BG50
14 MA_CLK0_P BD45
14 MA_CLK0_N BE45
14 MA_CLK1_P BB48
14 MA_CLK1_N BD48
14 MA_CKE0 BH61
14 MA_CKE1 BH60
BH58
BJ58
14 MA_BA2 BH57
14 MA_BA1 BG49
14 MA_BA0 BJ48
14 MA_RAS_N BG47
14 MA_WE_N BG48
14 MA_CAS_N BH47
14 MA_CS1_N BA41
14 MA_CS0_N AR43
AT43
BB41
14 MA_ODT1 AW41
14 MA_ODT0 AW43
MA_DQS7_P BG36
14 MA_DQS7_P
14 MA_DQS7_N BH35
MA_DQS7_N
14 MA_DQS6_P BB35
MA_DQS6_P
14 MA_DQS6_N BD35
MA_DQS6_N
14 MA_DQS5_P BJ42
MA_DQS5_P
14 MA_DQS5_N BG42
MA_DQS5_N
14 MA_DQS4_P AV39
MA_DQS4_P
14 MA_DQS4_N AW39
MA_DQS4_N
MA_DQS3_P BD52
14 MA_DQS3_P
14 MA_DQS3_N BB52
MA_DQS3_N
14 MA_DQS2_P BB59
MA_DQS2_P
14 MA_DQS2_N BB58
MA_DQS2_N
14 MA_DQS1_P AT59
MA_DQS1_P
14 MA_DQS1_N AT58
MA_DQS1_N
14 MA_DQS0_P BB63
MA_DQS0_P
14 MA_DQS0_N BC62
MA_DQS0_N
NI TP1
NI TP3
AR35
AT34
AR34
14 MA_DRAMRST_N
DDR3_M0_RCOMP AV34
R1
105R_0402
1%_1/16W
R0402
12mils
MEM0_MA15_CAA9_NC
MEM0_MA14_CAA8_NC
MEM0_MA13_CAB0_CAB0
MEM0_MA12_CAA5_NC
MEM0_MA11_CAA6_NC
MEM0_MA10_CAB6_NC
MEM0_MA9_CAA4_CAA4
MEM0_MA8_CAA1_CAA0
MEM0_MA7_CAA3_CAA3
MEM0_MA6_CAA0_CAA1
MEM0_MA5_CAA2_CAA2
MEM0_MA4_NC_NC
MEM0_MA3_NC_NC
MEM0_MA2_CAB5_CAB5
MEM0_MA1_CAB9_NC
MEM0_MA0_CAB7_NC
MEM0_CLKP0_CLKPB_CLKPB
MEM0_CLKN0_CLKNB_CLKNB
MEM0_CLKP1_CLKPA_CLKPA
MEM0_CLKN1_CLKNA_CLKNA
MEM0_CKE0_CKE0A_CKE0A
MEM0_CKE1_CKE1A_CKE1A
MEM0_NC_CKE0B_CKE0B
MEM0_NC_CKE1B_CKE1B
MEM0_BA2_CAA7_CAA5
MEM0_BA1_CAB8_NC
MEM0_BA0_CAB2_CAB4
MEM0_RASN_CAB3_CAB3
MEM0_WEN_CAB4_CAB2
MEM0_CASN_CAB1_CAB1
MEM0_CS1N_CSB1N_CS1B
MEM0_CS0N_CSA0N_CS0A
MEM0_NC_CSA1N_CS1A
MEM0_NC_CSB0N_CS0B
MEM0_0DT1_0DTB_NC
MEM0_0DT0_0DTA_NC
MEM0_DQSP7_DQSPB3_DQSPB3
MEM0_DQSN7_DQSNB3_DQSNB3
MEM0_DQSP6_DQSPB2_DQSPB2
MEM0_DQSN6_DQSNB2_DQSNB2
MEM0_DQSP5_DQSPB1_DQSPB1
MEM0_DQSN5_DQSNB1_DQSNB1
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MEM0_DQSP1_DQSPA1_DQSPA1
MEM0_DQSN1_DQSNA1_DQSNA1
MEM0_DQSP0_DQSPA0_DQSPA0
MEM0_DQSN0_DQSNA0_DQSNA0
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MEM0_RESETN_NC_RESETN
MEM0_RCOMP_RCOMP_RCOMP
MEM0
1 OF 16
948107
MEM0_DQ63_DQB31_DQB31 BJ34
MEM0_DQ62_DQB30_DQB30 BG37
MEM0_DQ61_DQB29_DQB29 BH37
MEM0_DQ60_DQB28_DQB28 BG38
MEM0_DQ59_DQB27_DQB27 BH33
MEM0_DQ58_DQB26_DQB26 BG33
MEM0_DQ57_DQB25_DQB25 BG34
MEM0_DQ56_DQB24_DQB24 BJ38
MEM0_DQ55_DQB23_DQB23 BB34
MEM0_DQ54_DQB22_DQB22 BD39
MEM0_DQ53_DQB21_DQB21 BE39
MEM0_DQ52_DQB20_DQB20 BB37
MEM0_DQ51_DQB19_DQB19 BD37
MEM0_DQ50_DQB18_DQB18 BD34
MEM0_DQ49_DQB17_DQB17 BE34
MEM0_DQ48_DQB16_DQB16 BA34
MEM0_DQ47_DQB15_DQB15 BH41
MEM0_DQ46_DQB14_DQB14 BH45
MEM0_DQ45_DQB13_DQB13 BG44
MEM0_DQ44_DQB12_DQB12 BG43
MEM0_DQ43_DQB11_DQB11 BJ40
MEM0_DQ42_DQB10_DQB10 BG40
MEM0_DQ41_DQB9_DQB9 BG39
MEM0_DQ40_DQB8_DQB8 BJ44
MEM0_DQ39_DQB7_DQB7 AW35
MEM0_DQ38_DQB6_DQB6 AR41
MEM0_DQ37_DQB5_DQB5 AT41
MEM0_DQ36_DQB4_DQB4 AT37
MEM0_DQ35_DQB3_DQB3 AR37
MEM0_DQ34_DQB2_DQB2 AW37
MEM0_DQ33_DQB1_DQB1 AV37
MEM0_DQ32_DQB0_DQB0 AR39
MEM0_DQ31_DQA31_DQA31 BB54
MEM0_DQ30_DQA30_DQA30 BA50
MEM0_DQ29_DQA29_DQA29 BB50
MEM0_DQ28_DQA28_DQA28 BD50
MEM0_DQ27_DQA27_DQA27 BE50
MEM0_DQ26_DQA26_DQA26 BF58
MEM0_DQ25_DQA25_DQA25 BD54
MEM0_DQ24_DQA24_DQA24 BE56
MEM0_DQ23_DQA23_DQA23 BD58
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MEM0_DQ20_DQA20_DQA20 AV54
MEM0_DQ19_DQA19_DQA19 BF59
MEM0_DQ18_DQA18_DQA18 BD59
MEM0_DQ17_DQA17_DQA17 BB57
MEM0_DQ16_DQA16_DQA16 AY57
MEM0_DQ15_DQA15_DQA15 AY59
MEM0_DQ14_DQA14_DQA14 AT54
MEM0_DQ13_DQA13_DQA13 AT55
MEM0_DQ12_DQA12_DQA12 AV57
MEM0_DQ11_DQA11_DQA11 AV58
MEM0_DQ10_DQA10_DQA10 AU62
MEM0_DQ9_DQA9_DQA9 AU63
MEM0_DQ8_DQA8_DQA8 AV59
MEM0_DQ7_DQA7_DQA7 BD62
MEM0_DQ6_DQA6_DQA6 AW63
MEM0_DQ5_DQA5_DQA5 AW62
MEM0_DQ4_DQA4_DQA4 BD63
MEM0_DQ3_DQA3_DQA3 BG62
MEM0_DQ2_DQA2_DQA2 BE62
MEM0_DQ1_DQA1_DQA1 AY61
MEM0_DQ0_DQA0_DQA0 AY62
MA_MD63
MA_MD62
MA_MD61
MA_MD60
MA_MD59
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MA_MD11
MA_MD10
MA_MD9
MA_MD8
MA_MD7
MA_MD6
MA_MD5
MA_MD4
MA_MD3
MA_MD2
MA_MD1
MA_MD0
MB_MD[63..0]
MB_MA[15..0]
U1B
IC
?
BMAP_REV = 1.5
(DDR3L/LPDDR3/LPDDR4)
MB_MA15 BG16
MB_MA14 BG15
MB_MA13 BH3
MB_MA12 BG13
MB_MA11 BH13
MB_MA10 BG7
MB_MA9 BH11
MB_MA8 BG12
MB_MA7 BG14
MB_MA6 BJ12
MB_MA5 BG11
MB_MA4 BB16
MB_MA3 BD16
MB_MA2 BH9
MB_MA1 BG10
MB_MA0 BG9
15 MB_CLK0_P BD19
15 MB_CLK0_N BE19
15 MB_CLK1_P BB21
15 MB_CLK1_N BD21
15 MB_CKE0 BG18
15 MB_CKE1 BG17
BH17
BJ16
15 MB_BA2 BH15
15 MB_BA1 BG8
15 MB_BA0 BH6
15 MB_RAS_N BJ6
15 MB_WE_N BH7
15 MB_CAS_N BH4
15 MB_CS1_N AW17
15 MB_CS0_N BD17
BB17
AV17
15 MB_ODT1 AV16
15 MB_ODT0 AW16
MB_DQS7_P BC2
15 MB_DQS7_P
15 MB_DQS7_N BB1
MB_DQS7_N
15 MB_DQS6_P AT5
MB_DQS6_P
15 MB_DQS6_N AT6
MB_DQS6_N
15 MB_DQS5_P BB5
MB_DQS5_P
15 MB_DQS5_N BB6
MB_DQS5_N
15 MB_DQS4_P BB12
MB_DQS4_P
15 MB_DQS4_N BD12
MB_DQS4_N
MB_DQS3_P AV25
15 MB_DQS3_P
15 MB_DQS3_N AW25
MB_DQS3_N
15 MB_DQS2_P BJ22
MB_DQS2_P
15 MB_DQS2_N BG22
MB_DQS2_N
15 MB_DQS1_P BD29
MB_DQS1_P
15 MB_DQS1_N BB29
MB_DQS1_N
15 MB_DQS0_P BG28
MB_DQS0_P
15 MB_DQS0_N BH29
MB_DQS0_N
NI TP2
NI TP4
AR29
AT30
AR30
15 MB_DRAMRST_N
DDR3_M1_RCOMP AV30
R2
105R_0402
1%_1/16W
R0402
12mils
MEM1_MA15_CAA9_NC
MEM1_MA14_CAA8_NC
MEM1_MA13_CAB0_CAB0
MEM1_MA12_CAA5_NC
MEM1_MA11_CAA6_NC
MEM1_MA10_CAB6_NC
MEM1_MA9_CAA4_CAA4
MEM1_MA8_CAA1_CAA0
MEM1_MA7_CAA3_CAA3
MEM1_MA6_CAA0_CAA1
MEM1_MA5_CAA2_CAA2
MEM1_MA4_NC_NC
MEM1_MA3_NC_NC
MEM1_MA2_CAB5_CAB5
MEM1_MA1_CAB9_NC
MEM1_MA0_CAB7_NC
MEM1_CLKP0_CLKPB_CLKPB
MEM1_CLKN0_CLKNB_CLKNB
MEM1_CLKP1_CLKPA_CLKPA
MEM1_CLKN1_CLKNA_CLKNA
MEM1_CKE0_CKE0A_CKE0A
MEM1_CKE1_CKE1A_CKE1A
MEM1_NC_CKE0B_CKE0B
MEM1_NC_CKE1B_CKE1B
MEM1_BA2_CAA7_CAA5
MEM1_BA1_CAB8_NC
MEM1_BA0_CAB2_CAB4
MEM1_RASN_CAB3_CAB3
MEM1_WEN_CAB4_CAB2
MEM1_CASN_CAB1_CAB1
MEM1_CS1N_CSB1N_CS1B
MEM1_CS0N_CSA0N_CS0A
MEM1_NC_CSA1N_CS1A
MEM1_NC_CSB0N_CS0B
MEM1_0DT1_0DTB_NC
MEM1_0DT0_0DTA_NC
MEM1_DQSP7_DQSPB3_DQSPB3
MEM1_DQSN7_DQSNB3_DQSNB3
MEM1_DQSP6_DQSPB2_DQSPB2
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MEM1_DQSP1_DQSPA1_DQSPA1
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MEM1_DQSP0_DQSPA0_DQSPA0
MEM1_DQSN0_DQSNA0_DQSNA0
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MEM1_RCOMP_RCOMP_RCOMP
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2 OF 16
948107
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MEM1_DQ62_DQB30_DQB30 AY3
MEM1_DQ61_DQB29_DQB29 AW2
MEM1_DQ60_DQB28_DQB28 AW1
MEM1_DQ59_DQB27_DQB27 BE2
MEM1_DQ58_DQB26_DQB26 BD1
MEM1_DQ57_DQB25_DQB25 BD2
MEM1_DQ56_DQB24_DQB24 AY2
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MEM1_DQ54_DQB22_DQB22 AV6
MEM1_DQ53_DQB21_DQB21 AV5
MEM1_DQ52_DQB20_DQB20 AY5
MEM1_DQ51_DQB19_DQB19 AU1
MEM1_DQ50_DQB18_DQB18 AT9
MEM1_DQ49_DQB17_DQB17 AT10
MEM1_DQ48_DQB16_DQB16 AU2
MEM1_DQ47_DQB15_DQB15 BF5
MEM1_DQ46_DQB14_DQB14 AY7
MEM1_DQ45_DQB13_DQB13 AY9
MEM1_DQ44_DQB12_DQB12 AV10
MEM1_DQ43_DQB11_DQB11 BB7
MEM1_DQ42_DQB10_DQB10 BD5
MEM1_DQ41_DQB9_DQB9 BD6
MEM1_DQ40_DQB8_DQB8 AV12
MEM1_DQ39_DQB7_DQB7 BE8
MEM1_DQ38_DQB6_DQB6 BD14
MEM1_DQ37_DQB5_DQB5 BB14
MEM1_DQ36_DQB4_DQB4 BA14
MEM1_DQ35_DQB3_DQB3 BB10
MEM1_DQ34_DQB2_DQB2 BE14
MEM1_DQ33_DQB1_DQB1 BD10
MEM1_DQ32_DQB0_DQB0 BF6
MEM1_DQ31_DQA31_DQA31 AW27
MEM1_DQ30_DQA30_DQA30 AR23
MEM1_DQ29_DQA29_DQA29 AR25
MEM1_DQ28_DQA28_DQA28 AV27
MEM1_DQ27_DQA27_DQA27 AT23
MEM1_DQ26_DQA26_DQA26 AR27
MEM1_DQ25_DQA25_DQA25 AW29
MEM1_DQ24_DQA24_DQA24 AT27
MEM1_DQ23_DQA23_DQA23 BG25
MEM1_DQ22_DQA22_DQA22 BH19
MEM1_DQ21_DQA21_DQA21 BG21
MEM1_DQ20_DQA20_DQA20 BG20
MEM1_DQ19_DQA19_DQA19 BJ24
MEM1_DQ18_DQA18_DQA18 BH23
MEM1_DQ17_DQA17_DQA17 BJ20
MEM1_DQ16_DQA16_DQA16 BG24
MEM1_DQ15_DQA15_DQA15 BD27
MEM1_DQ14_DQA14_DQA14 BD25
MEM1_DQ13_DQA13_DQA13 BB27
MEM1_DQ12_DQA12_DQA12 BE25
MEM1_DQ11_DQA11_DQA11 BD30
MEM1_DQ10_DQA10_DQA10 BE30
MEM1_DQ9_DQA9_DQA9 BB30
MEM1_DQ8_DQA8_DQA8 BA30
MEM1_DQ7_DQA7_DQA7 BJ30
MEM1_DQ6_DQA6_DQA6 BG26
MEM1_DQ5_DQA5_DQA5 BG27
MEM1_DQ4_DQA4_DQA4 BH27
MEM1_DQ3_DQA3_DQA3 BG31
MEM1_DQ2_DQA2_DQA2 BH31
MEM1_DQ1_DQA1_DQA1 BG30
MEM1_DQ0_DQA0_DQA0 BJ26
MB_MD63
MB_MD62
MB_MD61
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MB_MD59
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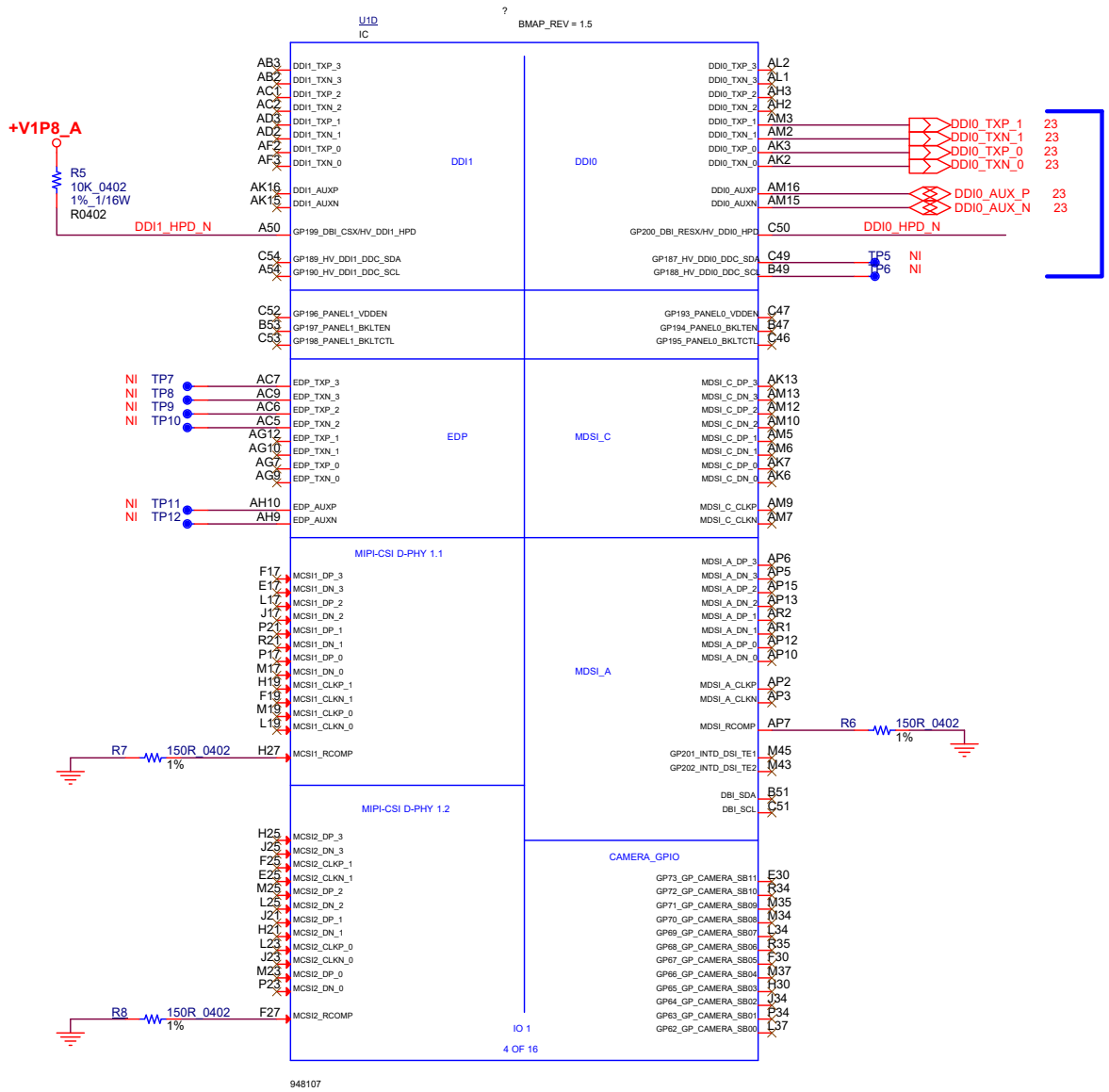
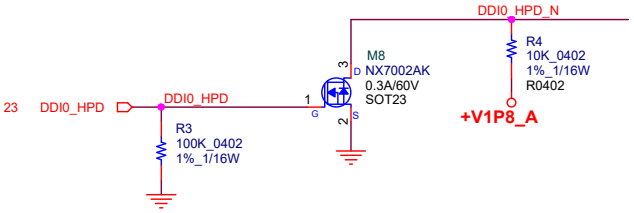
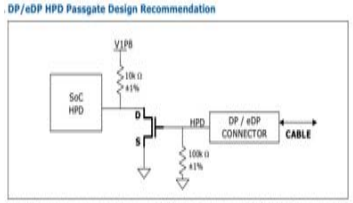
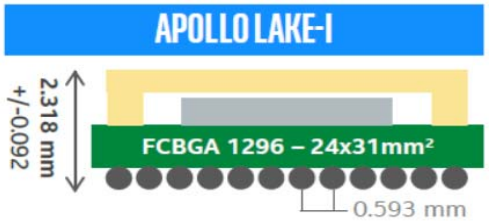
MB_MD6
MB_MD5
MB_MD4
MB_MD3
MB_MD2
MB_MD1
MB_MD0
U1C
IC
?
BMAP_REV = 1.5
BA45
BD43
AV47
AV48
AW45
BB43
AW47
AW48
BB47
BD47
MEM0_CB7_NC_NC
MEM0_CB6_NC_NC
MEM0_CB5_NC_NC
MEM0_CB4_NC_NC
MEM0_CB3_NC_NC
MEM0_CB2_NC_NC
MEM0_CB1_NC_NC
MEM0_CB0_NC_NC
MEM0_DQSN8_NC_NC
MEM0_DQSP8_NC_NC
MEM1_CB7_NC_NC BB23
MEM1_CB6_NC_NC BA23
MEM1_CB5_NC_NC AW19
MEM1_CB4_NC_NC BA19
MEM1_CB3_NC_NC AW21
MEM1_CB2_NC_NC AW23
MEM1_CB1_NC_NC AT21
MEM1_CB0_NC_NC AR21
MEM1_DQSN8_NC_NC BE23
MEM1_DQSP8_NC_NC BD23
DDR3L ECC
3 OF 16
948107
<Variant Name>
SOC_DDR3_CHA/CHB
Size
Custom
Project Name
RSY1
Engineer:
Andrew
Rev.
1.0
Date:
Thursday, May 03, 2018
Sheet 5 of 40









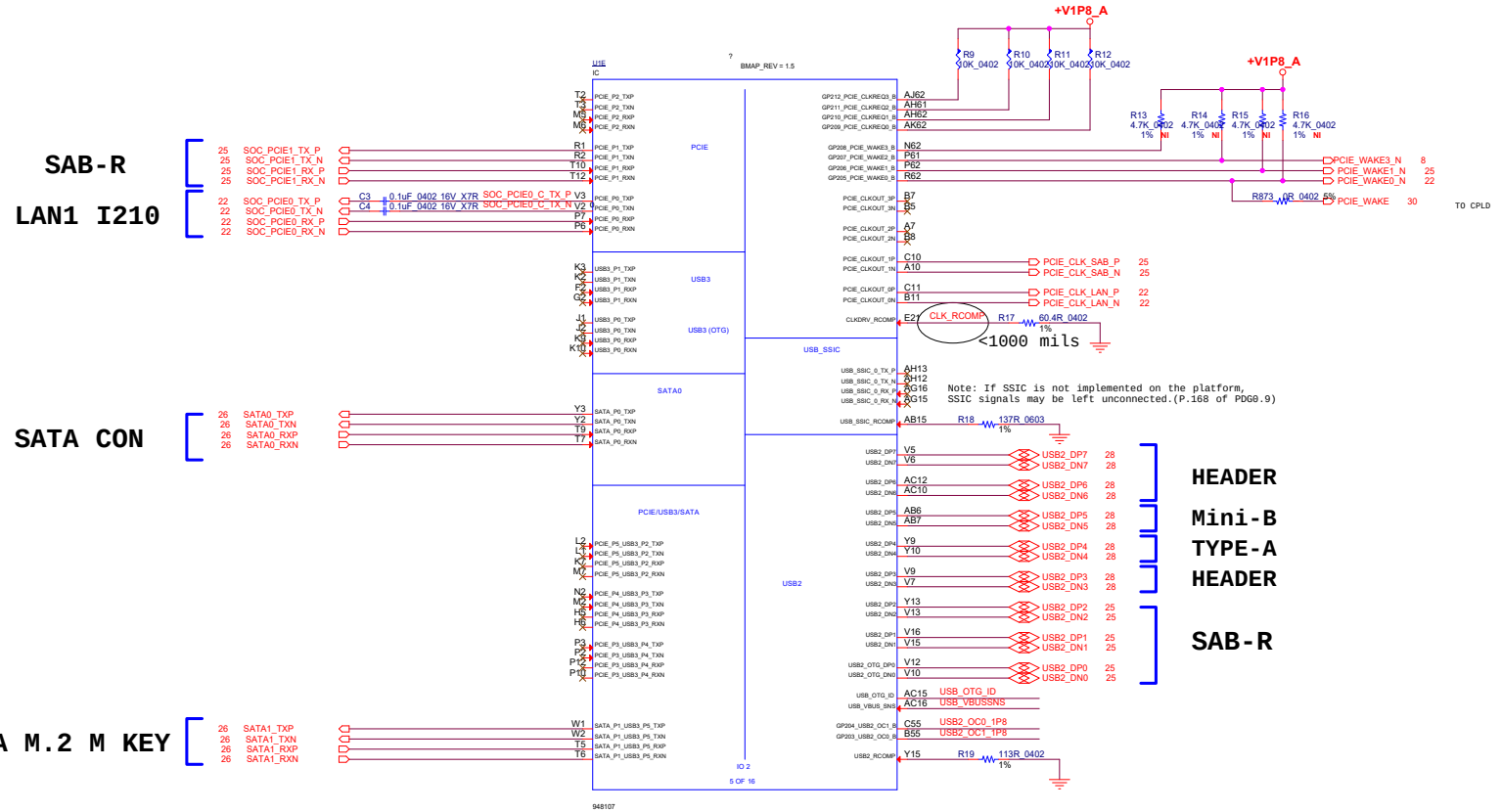
Precision Resistor Requirement for RCOMP

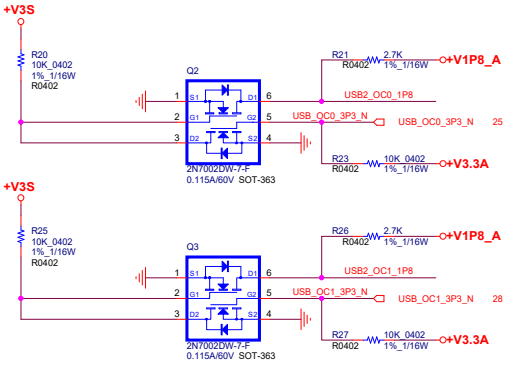
Interface	Pin name	Value (Ohm)
CSI1.1	MCSI_DPHY1.1_RCOMP	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSI_DPHY1.2_RCOMP	150 +/-1%
USB2 and 3.3V mode of dual voltage GPIO	USB2_RCOMP	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	60.4 +/-1%
modPHY (PCIE, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP_P/N	402 +/-1%
MDSI	MDSI_RCOMP	150 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode of SD Card, PMU, LPC, SMBUS.	EMMC_RCOMP GPIO_RCOMP PMU_RCOMP	200 +/-1%
eDP, DDI	EDP_RCOMP_P/N	402 +/-1%
Memory	MEM_CH0_RCOMP/ MEM_CH1_RCOMP	105 +/-1%
NOTE: USB_SSIC_RCOMP is not required to be connected, as the USB SSIC interface is not supported.		

<Variant Name>

SOC_EDP/DDI

Size	Project Name	Engineer:	Rev.
B	RSY1	Andrew	1.0
Date: Thursday, May 03, 2018		Sheet 6 of 40	





USB OTG feature is not required,

USB2_OTG_ID needs to be connected to GND.

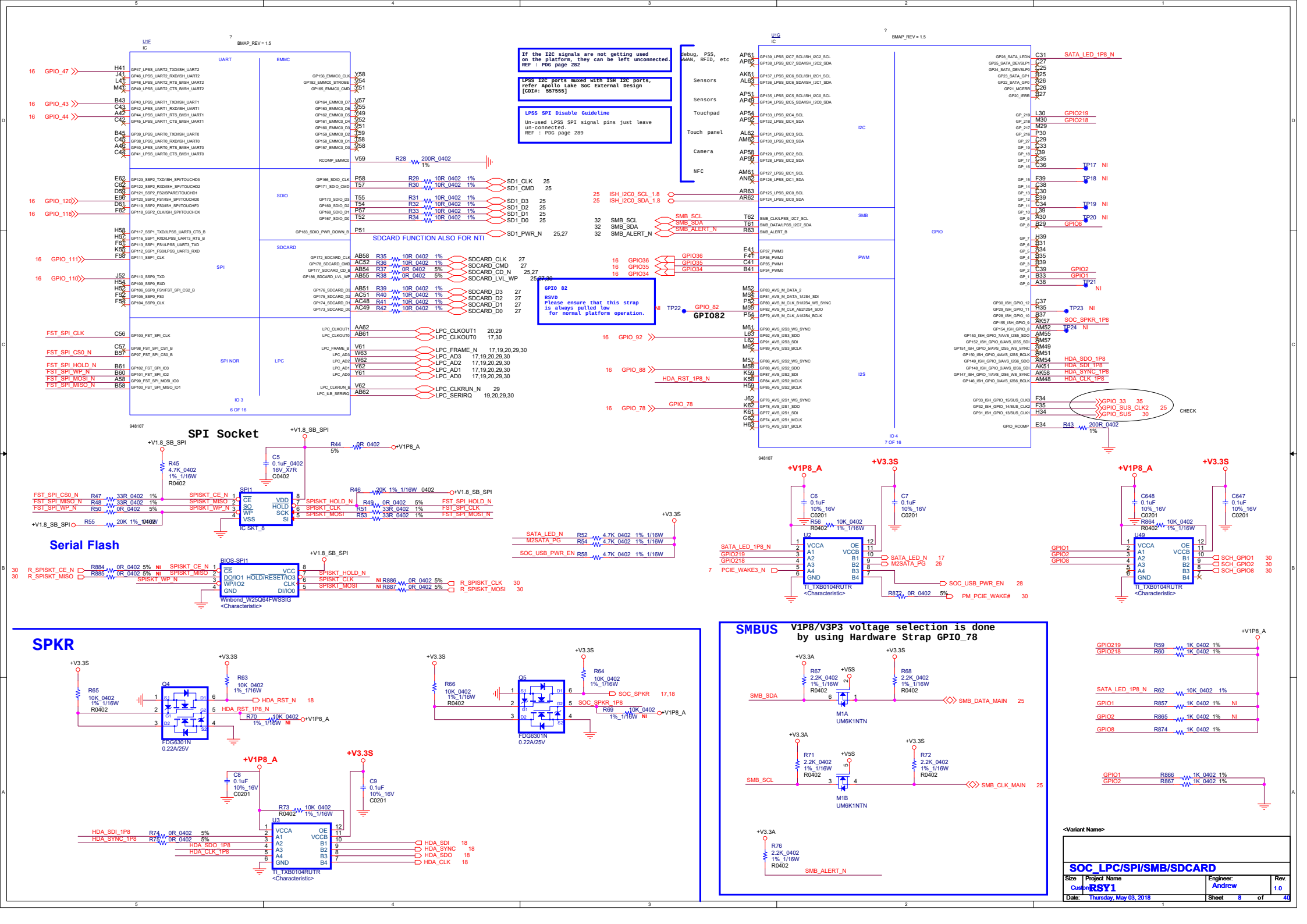
USB2_VBUS_SNS needs to be pull up to V1p8A with external 8-10kohm resistor (P.147 of PDG0.9)

High Speed I/O (HSIO) Lane Multiplexing in APL SoC

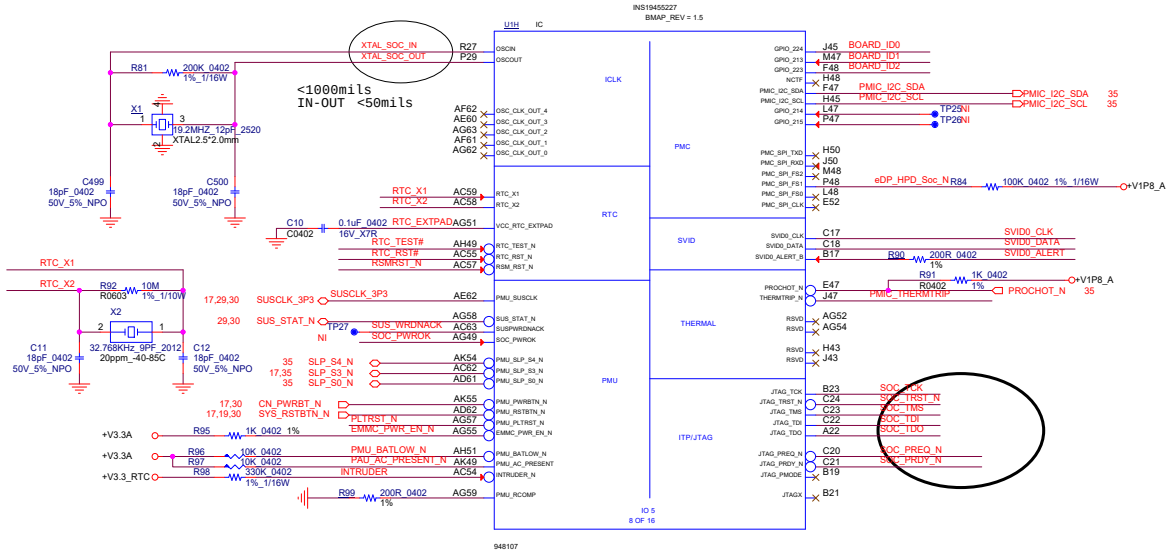
<Variant Name>

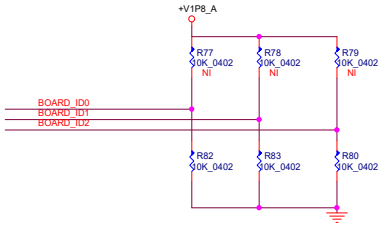
SOC_PCIE/SATA/CLK/USB

Size	Project Name	Engineer:	Rev.
C	RSY1	Andrew	1.0
Date: Thursday, May 03, 2018		Sheet 7 of 40	

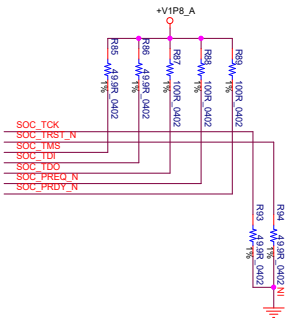

U1F
BMAP_REV = 1.5
UART
EMMC
SDIO
SDCARD
SPI
SPI NOR
LPC
IO 3
6 OF 16
U1G
IC
IO 4
7 OF 16
I2C
SMB
PWM
I2S
GPIO
SDCARD FUNCTION ALSO FOR NTI
GPIO 82
RSVD
Please ensure that this strap is always pulled low for normal platform operation.
GPIO82
If the I2C signals are not getting used on the platform, they can be left unconnected.
REF : PDG page 282
LPSS I2C ports muxed with ISH I2C ports, refer Apollo Lake SoC External Design [CDI#: 557555]
LPSS SPI Disable Guideline
Un-used LPSS SPI signal pins just leave un-connected.
REF : PDG page 289
Sensors
Touchpad
Touch panel
Camera
NFC
SPI Socket
Serial Flash
SPKR
SMBUS
V1P8/V3P3 voltage selection is done by using Hardware Strap GPIO_78
CHECK
<Variant Name>
SOC_LPC/SPI/SMB/SDCARD
RSY1
Andrew
Thursday, May 03, 2018

PMU_BATLOW_N,PMU_PLTRST_N,PMU_PWRBTN_N,
PMU_RSTBTN_N,PMU_SLP_S0_N,PMU_SLP_S3_N,
PMU_SLP_S4_N,PMU_SUSCLK,SUS_STAT_N
V1P8/V3P3 voltage selection is done by using Hardware Strap GPIO_78

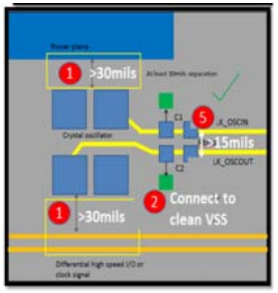


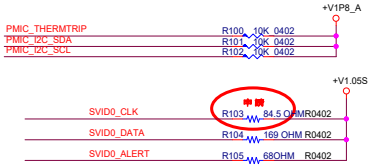


SKU ID			
GPIO	D6	D5	D4
NET NAME	ID2	ID1	ID0
REV A	0	0	0
REV B	0	0	1
REV C	0	1	0

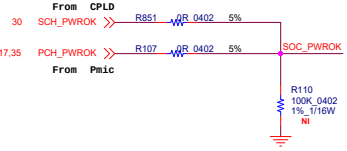


X1 Ref Layout

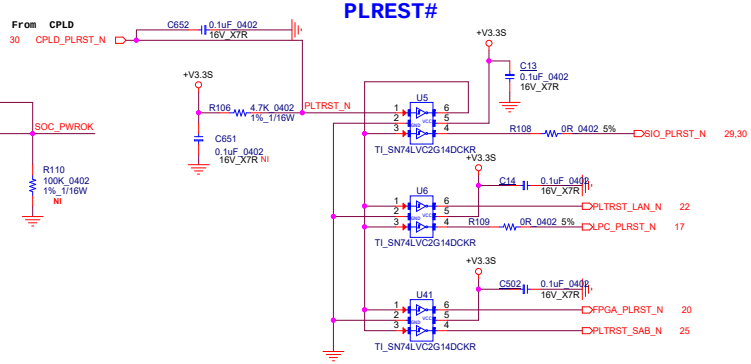




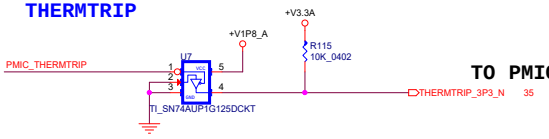
PCH_PWROK



PLREST#

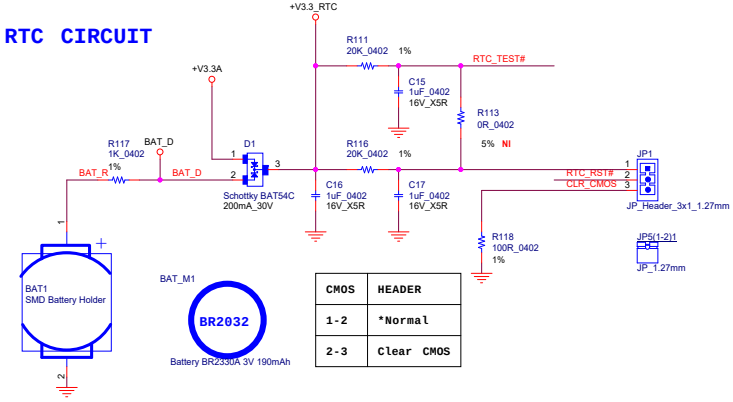


THERMTRIP



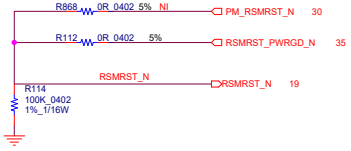
TO PMIC

RTC CIRCUIT



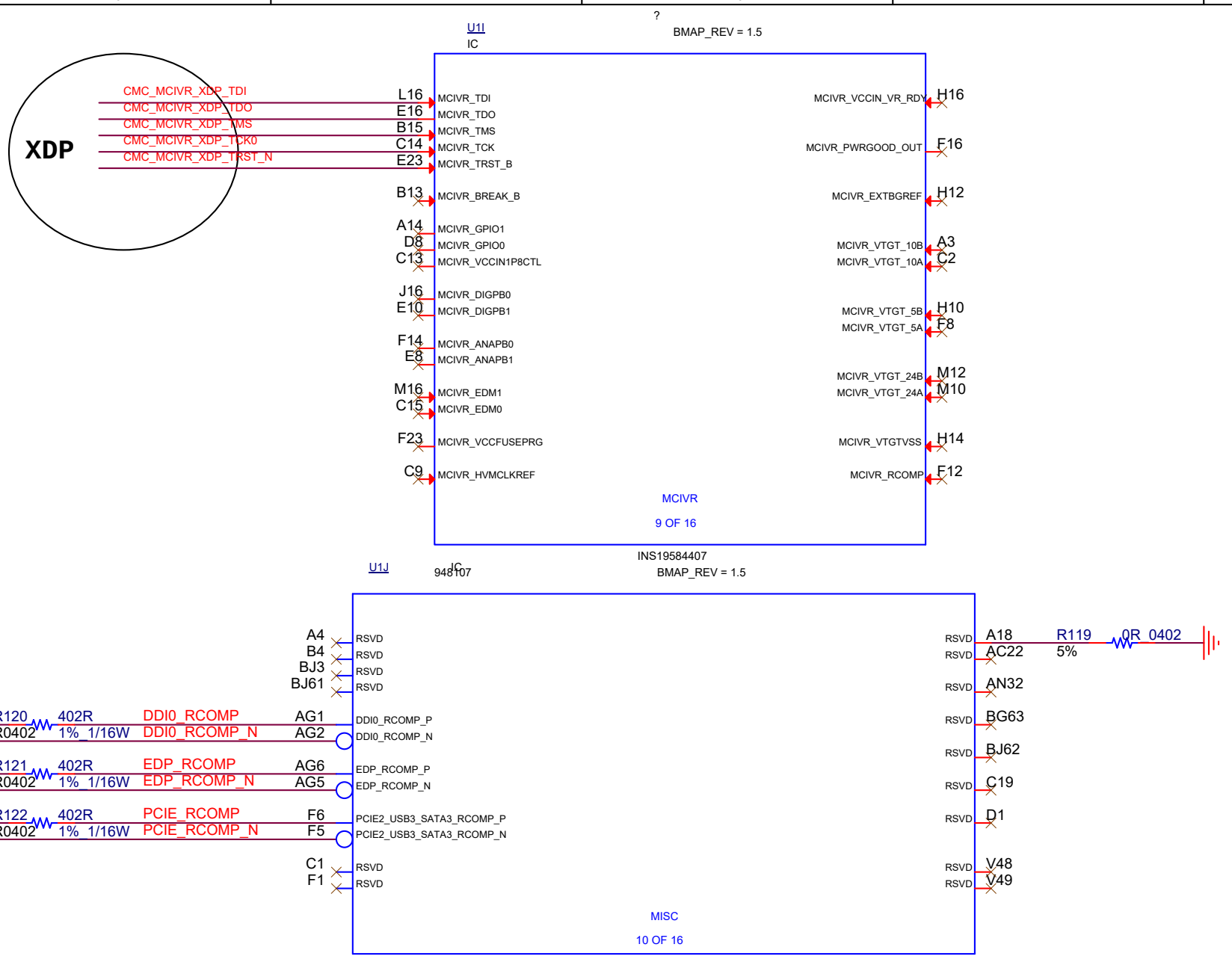
CMOS	HEADER
1-2	*Normal
2-3	Clear CMOS

RSRMST#



<Variant Name>

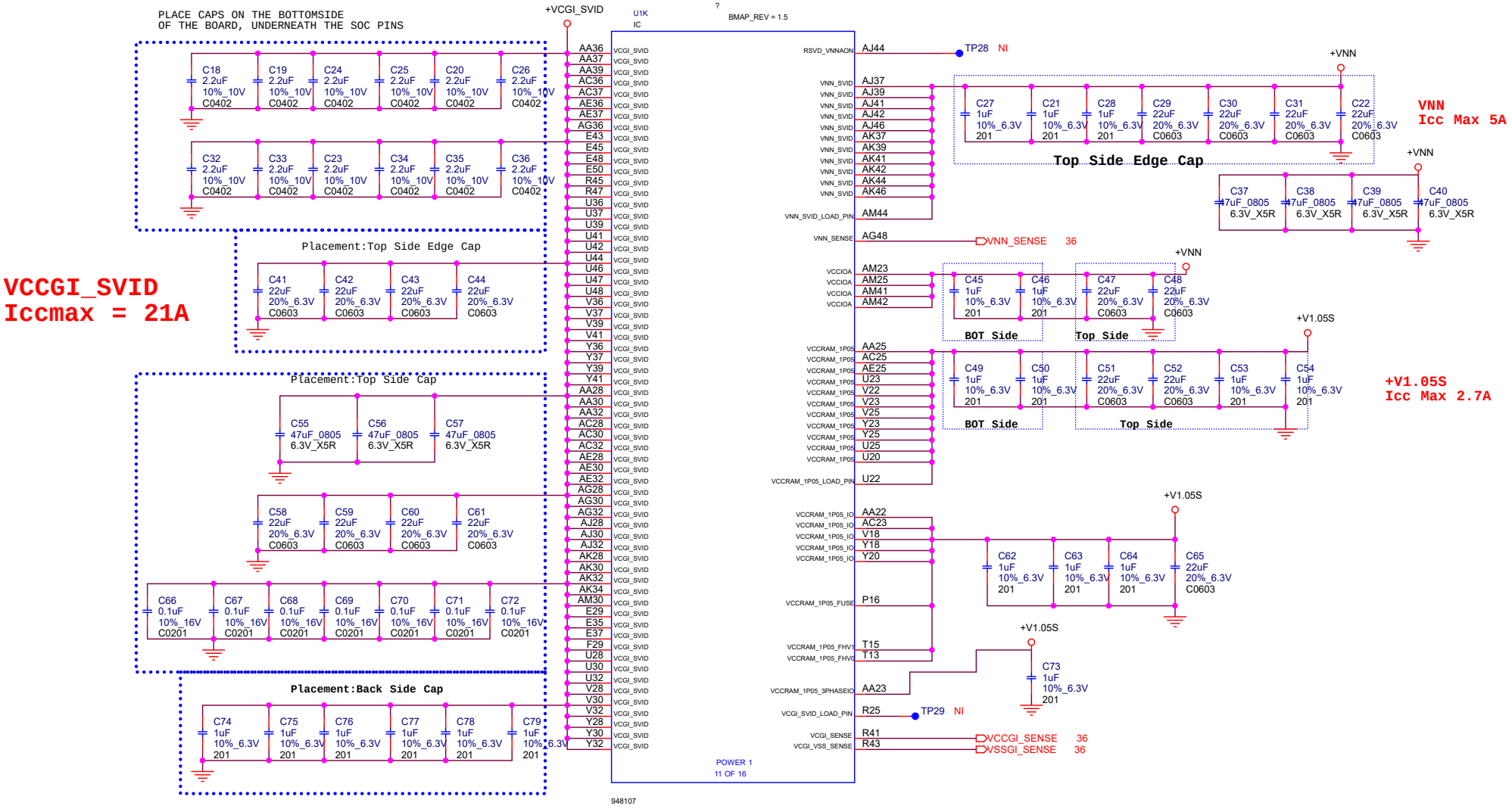
SOC_MISC			
Size: C	Project Name: RSY1	Engineer: Andrew	Rev: 1.0
Date: Thursday, May 03, 2018		Sheet 9 of 40	

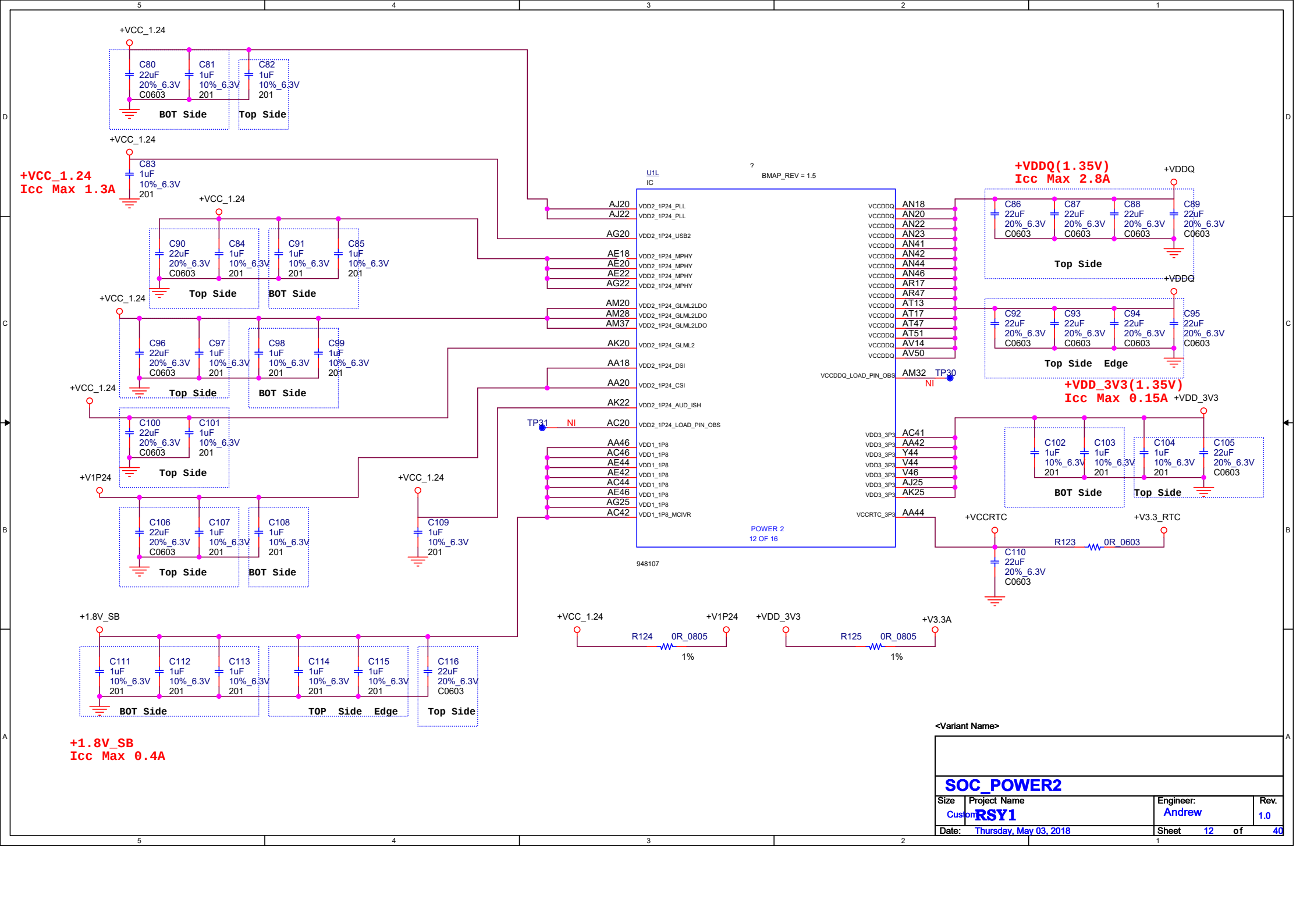


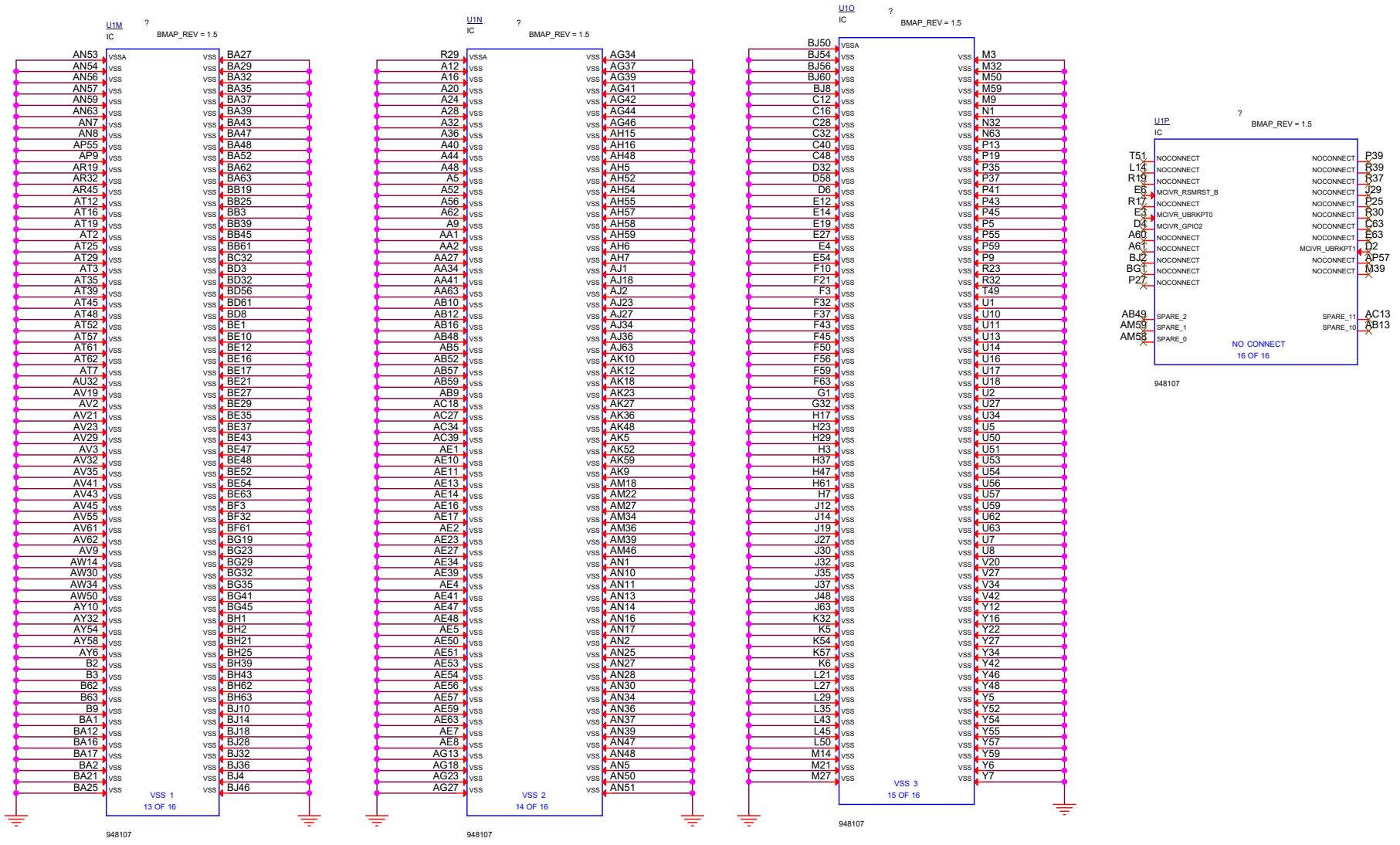
<Variant Name>

SOC_RCOMP/XDP

Size	Project Name	Engineer:	Rev.
A	RSY1	Andrew	1.0
Date:	Thursday, May 03, 2018	Sheet 10 of 40	


PLACE CAPS ON THE BOTTOMSIDE
OF THE BOARD, UNDERNEATH THE SOC PINS
VCCGI_SVID
Iccmax = 21A
+VCGI_SVID
U1K
IC
BMAP_REV = 1.5
Placement:Top Side Edge Cap
Placement:Top Side Cap
Placement:Back Side Cap
C18 2.2uF 10%_10V C0402
C19 2.2uF 10%_10V C0402
C24 2.2uF 10%_10V C0402
C25 2.2uF 10%_10V C0402
C20 2.2uF 10%_10V C0402
C26 2.2uF 10%_10V C0402
C32 2.2uF 10%_10V C0402
C33 2.2uF 10%_10V C0402
C23 2.2uF 10%_10V C0402
C34 2.2uF 10%_10V C0402
C35 2.2uF 10%_10V C0402
C36 2.2uF 10%_10V C0402
C41 22uF 20%_6.3V C0603
C42 22uF 20%_6.3V C0603
C43 22uF 20%_6.3V C0603
C44 22uF 20%_6.3V C0603
C55 47uF_0805 6.3V_X5R
C56 47uF_0805 6.3V_X5R
C57 47uF_0805 6.3V_X5R
C58 22uF 20%_6.3V C0603
C59 22uF 20%_6.3V C0603
C60 22uF 20%_6.3V C0603
C61 22uF 20%_6.3V C0603
C66 0.1uF 10%_16V C0201
C67 0.1uF 10%_16V C0201
C68 0.1uF 10%_16V C0201
C69 0.1uF 10%_16V C0201
C70 0.1uF 10%_16V C0201
C71 0.1uF 10%_16V C0201
C72 0.1uF 10%_16V C0201
C74 1uF 10%_6.3V 201
C75 1uF 10%_6.3V 201
C76 1uF 10%_6.3V 201
C77 1uF 10%_6.3V 201
C78 1uF 10%_6.3V 201
C79 1uF 10%_6.3V 201
AA36 AA37 AA39 AC36 AC37 AE36 AE37 AG36 E43 E45 E48 E50 R45 R47 U36 U37 U39 U41 U42 U44 U46 U47 U48 V36 V37 V39 V41 Y36 Y37 Y39 Y41 AA28 AA30 AA32 AC28 AC30 AC32 AE28 AE30 AE32 AG28 AG30 AG32 AJ28 AJ30 AJ32 AK28 AK30 AK32 AK34 AM30 E29 E35 E37 F29 U28 U30 U32 V28 V30 V32 Y28 Y30 Y32
VCGI_SVID
POWER 1
11 OF 16
948107
RSVD_VNNAON AJ44
TP28 NI
VNN_SVID AJ37 AJ39 AJ41 AJ42 AJ46 AK37 AK39 AK41 AK42 AK44 AK46
VNN_SVID_LOAD_PIN AM44
VNN_SENSE AG48
VNN_SENSE 36
+VNN
C27 1uF 10%_6.3V 201
C21 1uF 10%_6.3V 201
C28 1uF 10%_6.3V 201
C29 22uF 20%_6.3V C0603
C30 22uF 20%_6.3V C0603
C31 22uF 20%_6.3V C0603
C22 22uF 20%_6.3V C0603
Top Side Edge Cap
VNN
Icc Max 5A
C37 47uF_0805 6.3V_X5R
C38 47uF_0805 6.3V_X5R
C39 47uF_0805 6.3V_X5R
C40 47uF_0805 6.3V_X5R
VCCIOA AM23 AM25 AM41 AM42
C45 1uF 10%_6.3V 201
C46 1uF 10%_6.3V 201
C47 22uF 20%_6.3V C0603
C48 22uF 20%_6.3V C0603
BOT Side
Top Side
+V1.05S
VCCRAM_1P05 AA25 AC25 AE25 U23 V22 V23 V25 Y23 Y25 U25 U20
VCCRAM_1P05_LOAD_PIN U22
C49 1uF 10%_6.3V 201
C50 1uF 10%_6.3V 201
C51 22uF 20%_6.3V C0603
C52 22uF 20%_6.3V C0603
C53 1uF 10%_6.3V 201
C54 1uF 10%_6.3V 201
+V1.05S
Icc Max 2.7A
VCCRAM_1P05_IO AA22 AC23 V18 Y18 Y20
VCCRAM_1P05_FUSE P16
C62 1uF 10%_6.3V 201
C63 1uF 10%_6.3V 201
C64 1uF 10%_6.3V 201
C65 22uF 20%_6.3V C0603
VCCRAM_1P05_FHV1 T15
VCCRAM_1P05_FHV0 T13
VCCRAM_1P05_3PHASEIO AA23
C73 1uF 10%_6.3V 201
VCGI_SVID_LOAD_PIN R25
TP29 NI
VCGI_SENSE R41
VCGI_VSS_SENSE R43
VCCGI_SENSE 36
VSSGI_SENSE 36
<Variant Name>
SOC_POWER1
Size B
Project Name RSY1
Engineer: Andrew
Rev. 1.0
Date: Thursday, May 03, 2018
Sheet 11 of 40


+VCC_1.24
C80 22uF 20%_6.3V C0603
C81 1uF 10%_6.3V 201
C82 1uF 10%_6.3V 201
BOT Side
Top Side
+VCC_1.24
Icc Max 1.3A
C83 1uF 10%_6.3V 201
+VCC_1.24
C90 22uF 20%_6.3V C0603
C84 1uF 10%_6.3V 201
C91 1uF 10%_6.3V 201
C85 1uF 10%_6.3V 201
Top Side
BOT Side
+VCC_1.24
C96 22uF 20%_6.3V C0603
C97 1uF 10%_6.3V 201
C98 1uF 10%_6.3V 201
C99 1uF 10%_6.3V 201
Top Side
BOT Side
+VCC_1.24
C100 22uF 20%_6.3V C0603
C101 1uF 10%_6.3V 201
Top Side
+V1P24
C106 22uF 20%_6.3V C0603
C107 1uF 10%_6.3V 201
C108 1uF 10%_6.3V 201
Top Side
BOT Side
+VCC_1.24
C109 1uF 10%_6.3V 201
+1.8V_SB
C111 1uF 10%_6.3V 201
C112 1uF 10%_6.3V 201
C113 1uF 10%_6.3V 201
C114 1uF 10%_6.3V 201
C115 1uF 10%_6.3V 201
C116 22uF 20%_6.3V C0603
BOT Side
TOP Side Edge
Top Side
+1.8V_SB
Icc Max 0.4A
U1L
IC
BMAP_REV = 1.5
AJ20 VDD2_1P24_PLL
AJ22 VDD2_1P24_PLL
AG20 VDD2_1P24_USB2
AE18 VDD2_1P24_MPHY
AE20 VDD2_1P24_MPHY
AE22 VDD2_1P24_MPHY
AG22 VDD2_1P24_MPHY
AM20 VDD2_1P24_GLML2LDO
AM28 VDD2_1P24_GLML2LDO
AM37 VDD2_1P24_GLML2LDO
AK20 VDD2_1P24_GLML2
AA18 VDD2_1P24_DSI
AA20 VDD2_1P24_CSI
AK22 VDD2_1P24_AUD_ISH
TP31 NI AC20 VDD2_1P24_LOAD_PIN_OBS
AA46 VDD1_1P8
AC46 VDD1_1P8
AE44 VDD1_1P8
AE42 VDD1_1P8
AC44 VDD1_1P8
AE46 VDD1_1P8
AG25 VDD1_1P8
AC42 VDD1_1P8_MCIVR
POWER 2
12 OF 16
948107
VCCDDQ AN18
VCCDDQ AN20
VCCDDQ AN22
VCCDDQ AN23
VCCDDQ AN41
VCCDDQ AN42
VCCDDQ AN44
VCCDDQ AN46
VCCDDQ AR17
VCCDDQ AR47
VCCDDQ AT13
VCCDDQ AT17
VCCDDQ AT47
VCCDDQ AT51
VCCDDQ AV14
VCCDDQ AV50
VCCDDQ_LOAD_PIN_OBS AM32 TP30 NI
+VDDQ(1.35V)
Icc Max 2.8A
+VDDQ
C86 22uF 20%_6.3V C0603
C87 22uF 20%_6.3V C0603
C88 22uF 20%_6.3V C0603
C89 22uF 20%_6.3V C0603
Top Side
+VDDQ
C92 22uF 20%_6.3V C0603
C93 22uF 20%_6.3V C0603
C94 22uF 20%_6.3V C0603
C95 22uF 20%_6.3V C0603
Top Side Edge
+VDD_3V3(1.35V)
Icc Max 0.15A
+VDD_3V3
VDD3_3P3 AC41
VDD3_3P3 AA42
VDD3_3P3 Y44
VDD3_3P3 V44
VDD3_3P3 V46
VDD3_3P3 AJ25
VDD3_3P3 AK25
VCCRTC_3P3 AA44
C102 1uF 10%_6.3V 201
C103 1uF 10%_6.3V 201
C104 1uF 10%_6.3V 201
C105 22uF 20%_6.3V C0603
BOT Side
Top Side
+VCCRTC
+V3.3_RTC
R123 0R_0603
C110 22uF 20%_6.3V C0603
+VCC_1.24
+V1P24
R124 0R_0805 1%
+VDD_3V3
+V3.3A
R125 0R_0805 1%
<Variant Name>
SOC_POWER2
Size Custom
Project Name RSY1
Engineer: Andrew
Rev. 1.0
Date: Thursday, May 03, 2018
Sheet 12 of 40



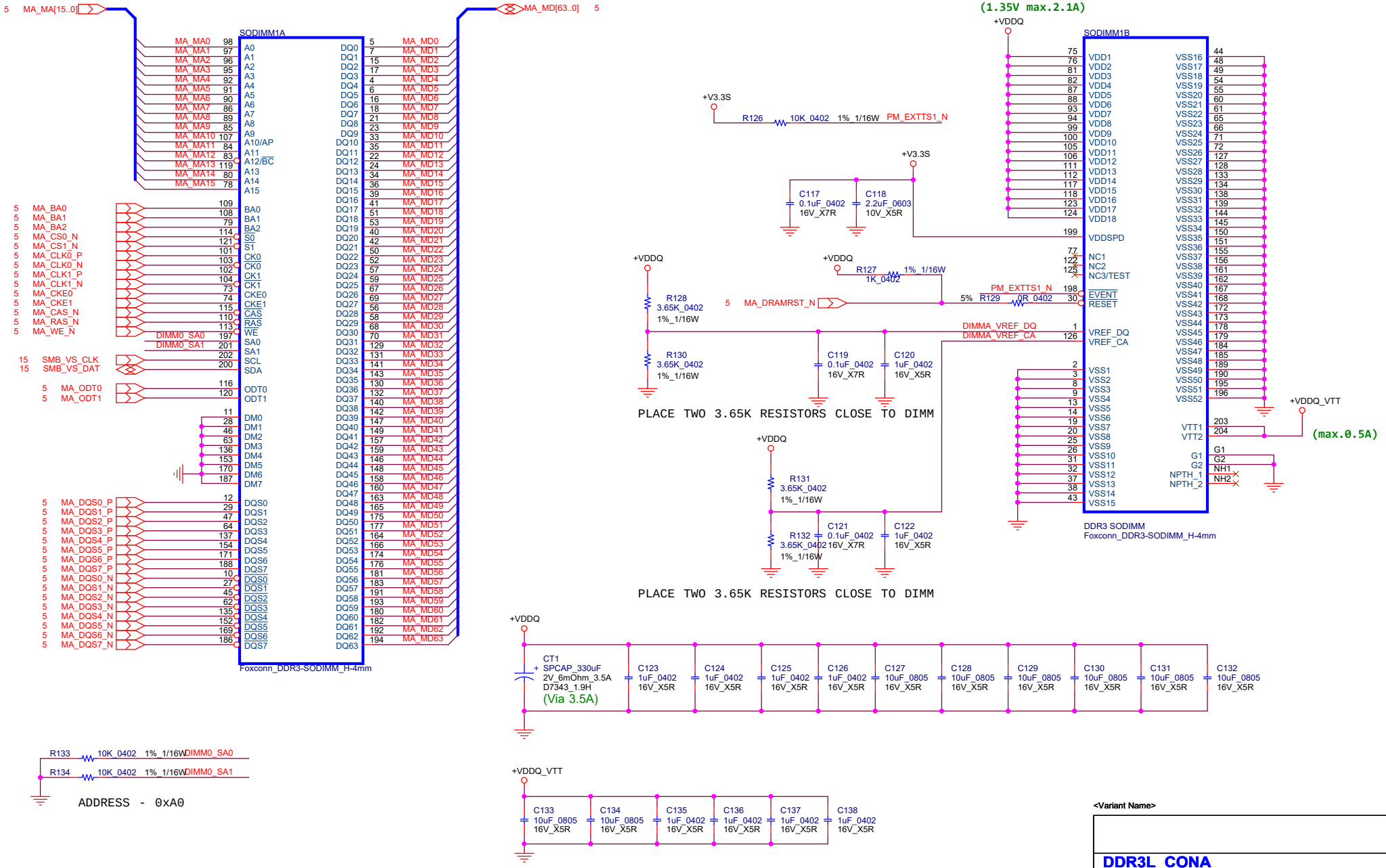
<Variant Name>

SOC_GND

Size	Project Name	Engineer:	Rev.
B	RSY1	Andrew	1.0
Date: Thursday, May 03, 2018		Sheet 13 of 40	

STANDARD-TYPE DDR3 SO-DIMM_A1

H=4mm

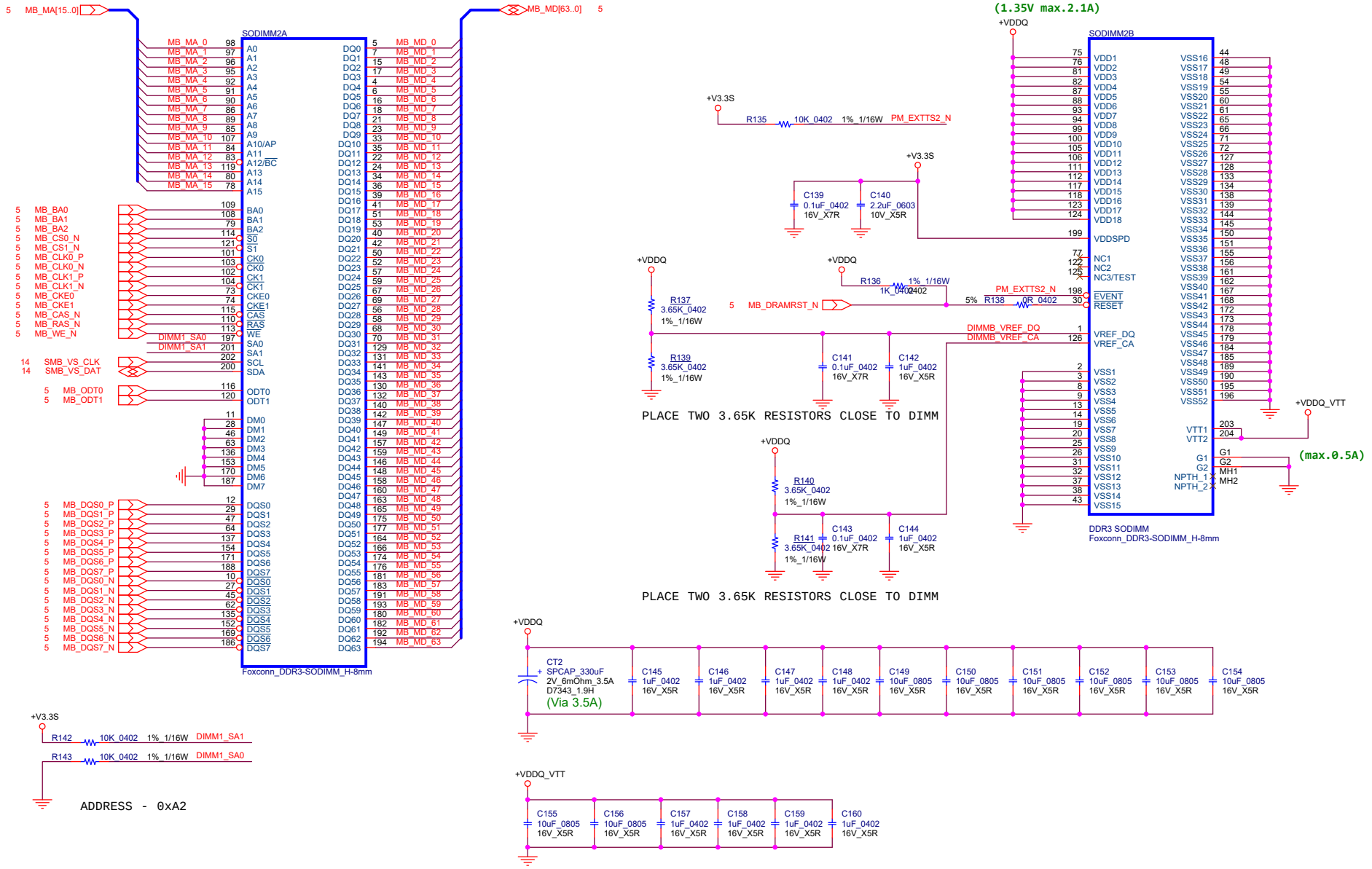


<Variant Name>

DDR3L_CONA			
Size: Custom	Project Name: RSY1	Engineer: Andrew	Rev: 1.0
Date: Thursday, May 03, 2018		Sheet 14 of 40	

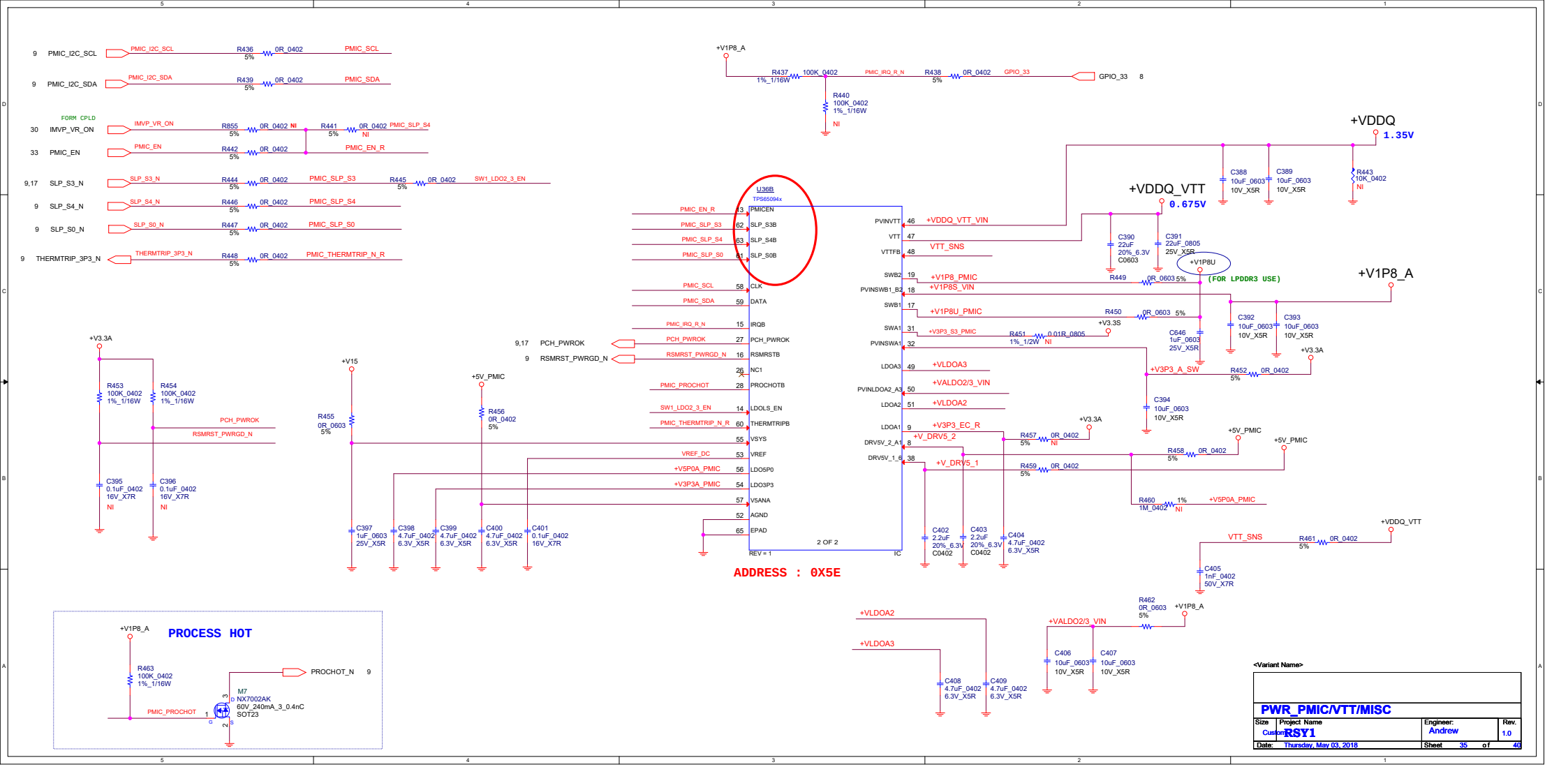
STANDARD-TYPE DDR3 SO-DIMM_B1

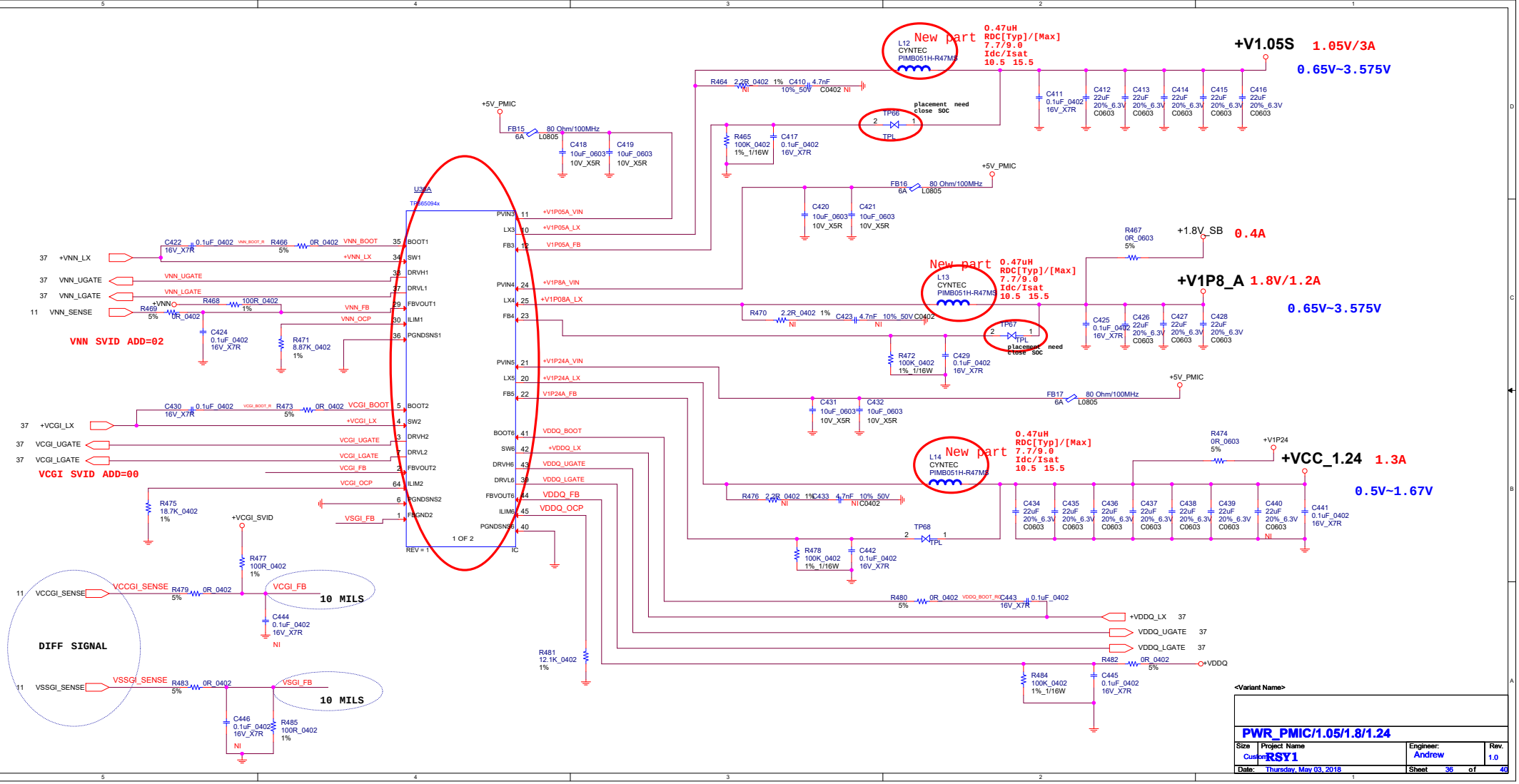
H=8mm



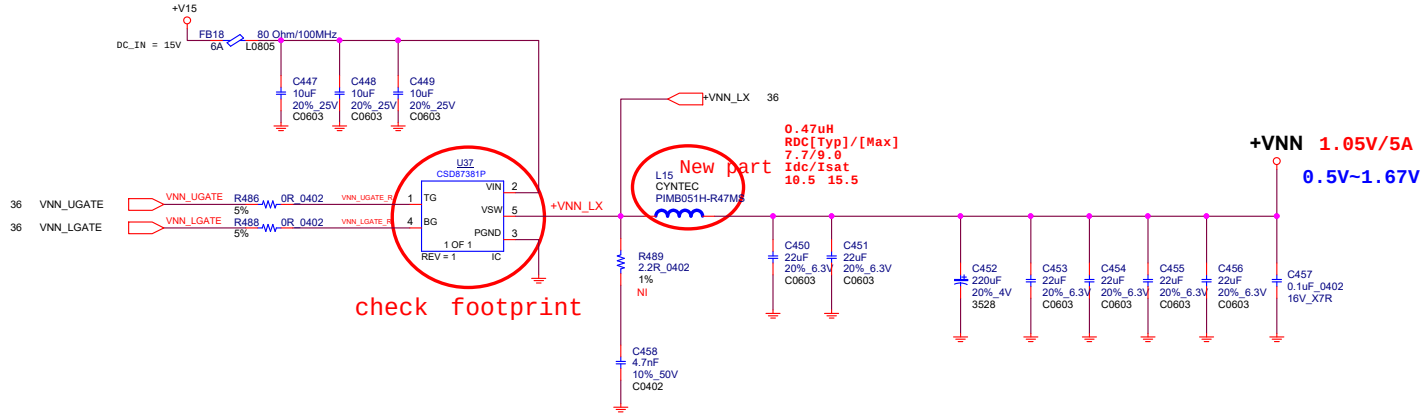
<Variant Name>

DDR3L_CONB			
Size: Custom	Project Name: RSY1	Engineer: Andrew	Rev: 1.0
Date: Thursday, May 03, 2018		Sheet 15 of 40	

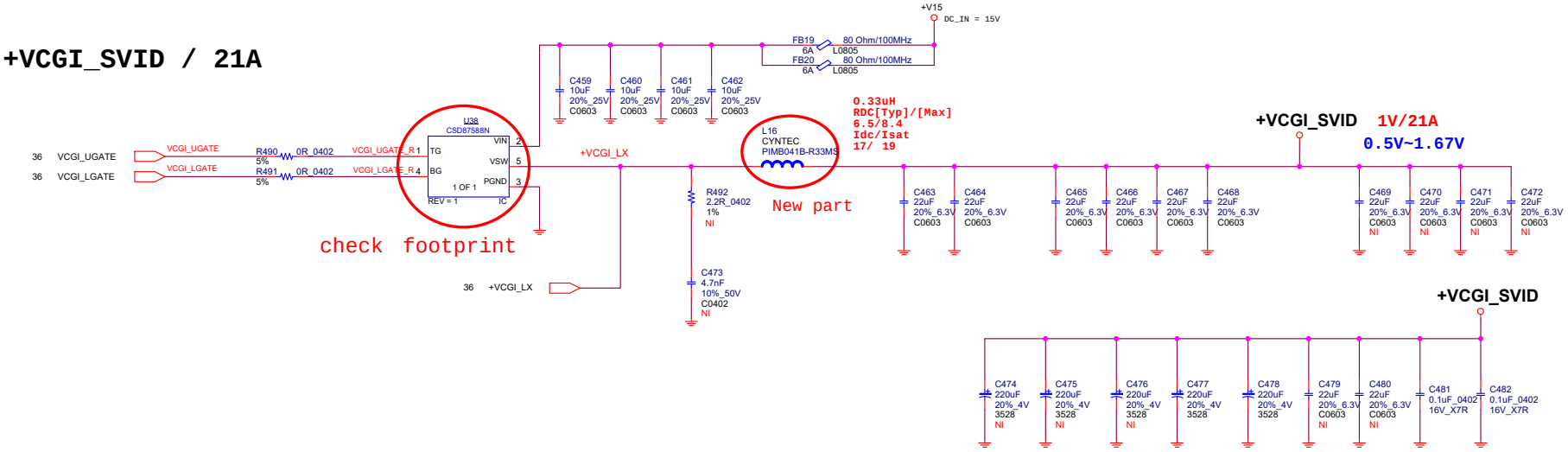

9 PMIC_I2C_SCL
PMIC_I2C_SCL
R436 0R_0402 5%
PMIC_SCL
9 PMIC_I2C_SDA
PMIC_I2C_SDA
R439 0R_0402 5%
PMIC_SDA
FORM CPLD
30 IMVP_VR_ON
IMVP_VR_ON
R855 0R_0402 NI 5%
R441 0R_0402 NI 5%
PMIC_SLP_S4
33 PMIC_EN
PMIC_EN
R442 0R_0402 5%
PMIC_EN_R
9,17 SLP_S3_N
SLP_S3_N
R444 0R_0402 5%
PMIC_SLP_S3
R445 0R_0402 5%
SW1_LDO2_3_EN
9 SLP_S4_N
SLP_S4_N
R446 0R_0402 5%
PMIC_SLP_S4
9 SLP_S0_N
SLP_S0_N
R447 0R_0402 5%
PMIC_SLP_S0
9 THERMTRIP_3P3_N
THERMTRIP_3P3_N
R448 0R_0402 5%
PMIC_THERMTRIP_N_R
+V1P8_A
R437 100K_0402 1%_1/16W
PMIC_IRQ_R_N
R438 0R_0402 5%
GPIO_33
GPIO_33 8
R440 100K_0402 1%_1/16W NI
U36B
TPS65094x
PMIC_EN_R 13 PMICEN
PMIC_SLP_S3 62 SLP_S3B
PMIC_SLP_S4 63 SLP_S4B
PMIC_SLP_S0 61 SLP_S0B
PMIC_SCL 58 CLK
PMIC_SDA 59 DATA
PMIC_IRQ_R_N 15 IRQB
9,17 PCH_PWROK
PCH_PWROK 27 PCH_PWROK
9 RSMRST_PWRGD_N
RSMRST_PWRGD_N 16 RSMRSTB
26 NC1
PMIC_PROCHOT 28 PROCHOTB
SW1_LDO2_3_EN 14 LDOLS_EN
PMIC_THERMTRIP_N_R 60 THERMTRIPB
55 VSYS
VREF_DC 53 VREF
+V5P0A_PMIC 56 LDO5P0
+V3P3A_PMIC 54 LDO3P3
57 VSANA
52 AGND
65 EPAD
REV = 1
2 OF 2
IC
PVINVTT 46 +VDDQ_VTT_VIN
VTT 47
VTTFB 48 VTT_SNS
SWB2 19 +V1P8_PMIC
PVINSWB1_B2 18 +V1P8S_VIN
SWB1 17 +V1P8U_PMIC
SWA1 31 +V3P3_S3_PMIC
PVINSWA1 32
LDOA3 49 +VLDOA3
PVINLDOA2_A3 50 +VALDO2/3_VIN
LDOA2 51 +VLDOA2
LDOA1 9 +V3P3_EC_R
DRV5V_2_A1 8 +V_DRV5_2
DRV5V_1_B1 38 +V_DRV5_1
+VDDQ
1.35V
+VDDQ_VTT
0.675V
C388 10uF_0603 10V_X5R
C389 10uF_0603 10V_X5R
R443 10K_0402 NI
C390 22uF 20% 6.3V C0603
C391 22uF_0805 25V_X5R
+V1P8U
(FOR LPDDR3 USE)
R449 0R_0603 5%
+V1P8_A
R450 0R_0603 5%
+V3.3S
C646 1uF_0603 25V_X5R
C392 10uF_0603 10V_X5R
C393 10uF_0603 10V_X5R
+V3.3A
R451 0.01R_0805 1%_1/2W NI
+V3P3_A_SW
R452 0R_0402 5%
C394 10uF_0603 10V_X5R
R457 0R_0402 5%
+V3.3A
R458 0R_0402 5%
+5V_PMIC
R459 0R_0402 5%
+5V_PMIC
R460 1M_0402 1% NI
+V5P0A_PMIC
C402 2.2uF 20% 6.3V C0402
C403 2.2uF 20% 6.3V C0402
C404 4.7uF_0402 6.3V_X5R
VTT_SNS
R461 0R_0402 5%
+VDDQ_VTT
C405 1nF_0402 50V_X7R
+V3.3A
R453 100K_0402 1%_1/16W
R454 100K_0402 1%_1/16W
PCH_PWROK
RSMRST_PWRGD_N
C395 0.1uF_0402 16V_X7R NI
C396 0.1uF_0402 16V_X7R NI
+V15
R455 0R_0603 5%
+5V_PMIC
R456 0R_0402 5%
C397 1uF_0603 25V_X5R
C398 4.7uF_0402 6.3V_X5R
C399 4.7uF_0402 6.3V_X5R
C400 4.7uF_0402 6.3V_X5R
C401 0.1uF_0402 16V_X7R
ADDRESS : 0X5E
+VLDOA2
+VLDOA3
C408 4.7uF_0402 6.3V_X5R
C409 4.7uF_0402 6.3V_X5R
+VALDO2/3_VIN
C406 10uF_0603 10V_X5R
C407 10uF_0603 10V_X5R
R462 0R_0603 5%
+V1P8_A
PROCESS HOT
+V1P8_A
R463 100K_0402 1%_1/16W
PROCHOT_N 9
PMIC_PROCHOT
M7
NX7002AK
60V_240mA_3_0.4nC
SOT23
<Variant Name>
PWR_PMIC/VTT/MISC
Size
Project Name
RSY1
Engineer:
Andrew
Rev.
1.0
Date: Thursday, May 03, 2018
Sheet 35 of 40


New part
0.47uH
RDC[Typ]/[Max]
7.7/9.0
Idc/Isat
10.5 15.5
L12
CYNTEC
PIMB051H-R47MS
+V1.05S 1.05V/3A
0.65V~3.575V
+V1P8_A 1.8V/1.2A
0.65V~3.575V
+1.8V_SB 0.4A
+V1P24
+VCC_1.24 1.3A
0.5V~1.67V
+5V_PMIC
VNN SVID ADD=02
VCGI SVID ADD=00
DIFF SIGNAL
10 MILS
placement need close SOC
1 OF 2
REV = 1
PWR_PMIC/1.05/1.8/1.24
Project Name
RSY1
Engineer:
Andrew
Rev.
1.0
Thursday, May 03, 2018
Sheet 36 of 40

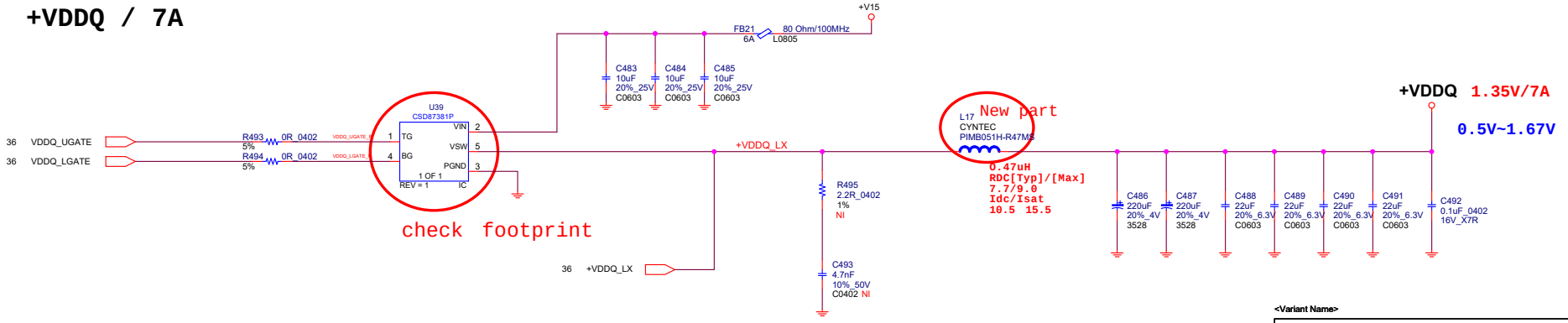
+VNN / 5A



+VCGI_SVID / 21A



+VDDQ / 7A



<Variant Name>

PWR_PMIC/VNN/VDDQ/VCGI

Size	Project Name	Engineer:	Rev.
Custom	RSY1	Andrew	1.0
Date: Thursday, May 03, 2018		Sheet 37 of 40	