

A A

B B

C C

D D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.83mil		
4	Dielectricl	FR-4	55.53mil	4.8	
5	Bottom Layer	Copper	2.83mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 8 MIL  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 24 MIL  
 MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENEPIG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

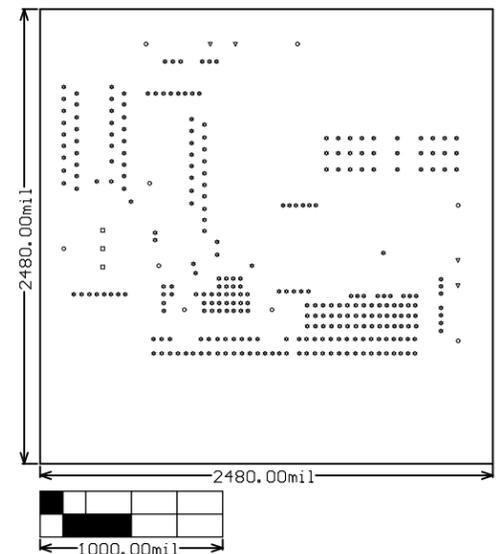
**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
✳	285	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
□	3	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
▽	4	50.00mil (1.270mm)	PTH	Round	Top Layer - Bottom Layer	
○	9	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
	301 Total					



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: BSR040	REV: A	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: Ryan Hu	LAYOUT BY: Ryan Hu
LAYER NAME = 060504-01	TID #: N/A	GENERATED : 3/18/2019 9:09:33 PM	TEXAS INSTRUMENTS		SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472
PLOT NAME = Fabrication Drawing						